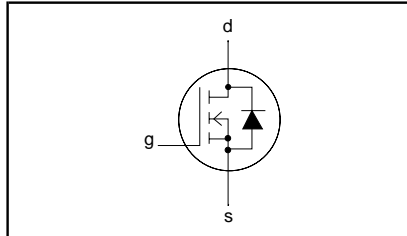


**SiliconMAX****N-channel logic level TrenchMOS™ transistor PSMN004-25B, PSMN004-25P****FEATURES**

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

**SYMBOL****QUICK REFERENCE DATA**

$V_{DSS} = 25 \text{ V}$
$I_D = 75 \text{ A}$
$R_{DS(ON)} \leq 4.3 \text{ m}\Omega (V_{GS} = 10 \text{ V})$
$R_{DS(ON)} \leq 5 \text{ m}\Omega (V_{GS} = 5 \text{ V})$

**GENERAL DESCRIPTION**

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

**Applications:-**

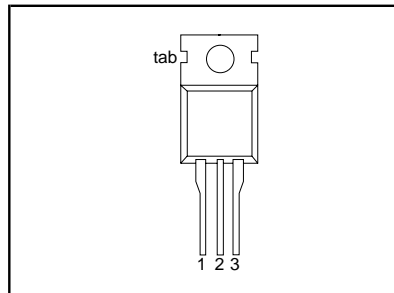
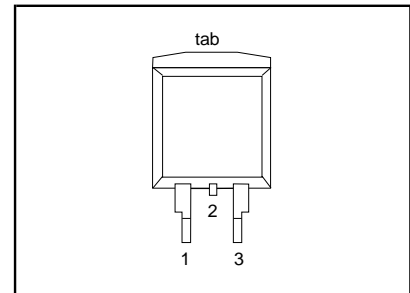
- d.c. to d.c. converters
- switched mode power supplies

The PSMN004-25P is supplied in the SOT78 (TO220AB) conventional leaded package.

The PSMN004-25B is supplied in the SOT404 surface mounting package.

**PINNING**

PIN	DESCRIPTION
1	gate
2	drain <sup>1</sup>
3	source
tab	drain

**SOT78 (TO220AB)****SOT404 (D<sup>2</sup>PAK)****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$	-	25	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	25	V
$V_{GS}$	Continuous gate-source voltage		-	$\pm 15$	V
$V_{GSM}$	Peak pulsed gate-source voltage	$T_j \leq 150 \text{ }^\circ\text{C}$	-	$\pm 20$	V
$I_D$	Continuous drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$ $T_{mb} = 100 \text{ }^\circ\text{C}$ ; $V_{GS} = 5 \text{ V}$	-	$75^2$	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	240	A
$P_D$	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	230	W
$T_j, T_{stg}$	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

<sup>1</sup> It is not possible to make connection to pin:2 of the SOT404 package

<sup>2</sup> maximum continuous current limited by package

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**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	0.65	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, vertical in still air SOT404 package, pcb mounted, minimum footprint	-	60	-	K/W
			-	50	-	K/W

**AVALANCHE ENERGY LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{AS}$	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 75\text{ A}$ ; $t_p = 100\ \mu\text{s}$ ; $T_j$ prior to avalanche = $25^\circ\text{C}$ ; $V_{DD} \leq 15\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 5\text{ V}$	-	120	mJ
$I_{AS}$	Non-repetitive avalanche current		-	75	A

**ELECTRICAL CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.25\text{ mA}$ ; $T_j = -55^\circ\text{C}$	25 22	-	-	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ ; $I_D = 1\text{ mA}$ ; $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.5	1.5	2	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ $V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 175^\circ\text{C}$	-	3.5	4.3	m $\Omega$
$I_{GSS}$	Gate-source leakage current	$V_{GS} = \pm 10\text{ V}$ ; $V_{DS} = 0\text{ V}$ ;	-	0.02	100	nA
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 25\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 175^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$Q_{g(tot)}$	Total gate charge	$I_D = 75\text{ A}$ ; $V_{DD} = 15\text{ V}$ ; $V_{GS} = 5\text{ V}$	-	97	-	nC
$Q_{gs}$	Gate-source charge		-	20	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	39	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ ; $R_D = 1.2\ \Omega$	-	45	-	ns
$t_r$	Turn-on rise time	$V_{GS} = 5\text{ V}$ ; $R_G = 5.6\ \Omega$	-	220	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	435	-	ns
$t_f$	Turn-off fall time		-	320	-	ns
$L_d$	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $f = 1\text{ MHz}$	-	6000	-	pF
$C_{oss}$	Output capacitance		-	1700	-	pF
$C_{rss}$	Feedback capacitance		-	1400	-	pF

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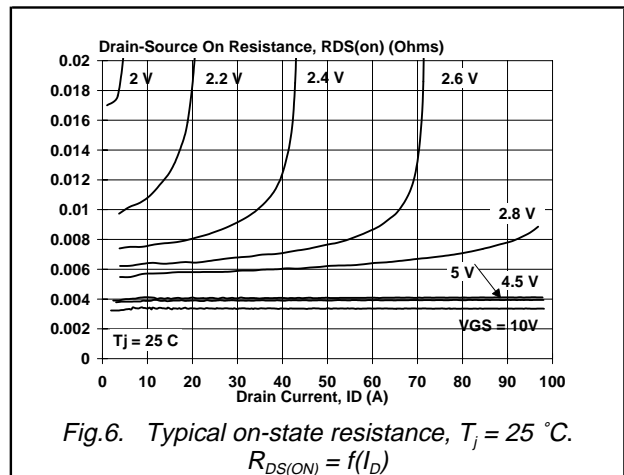
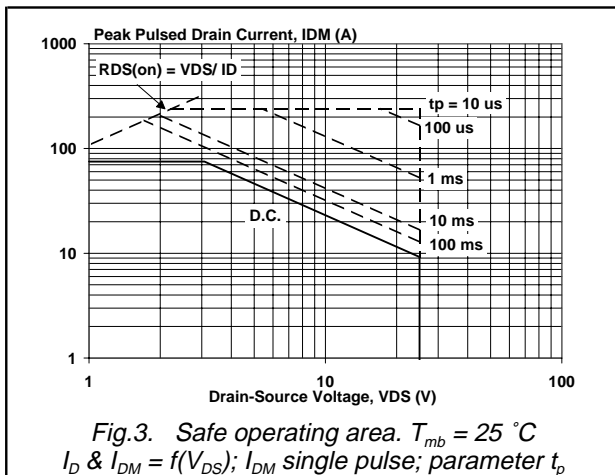
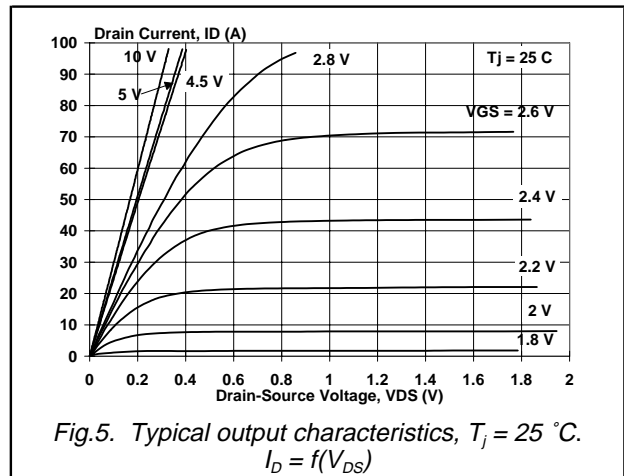
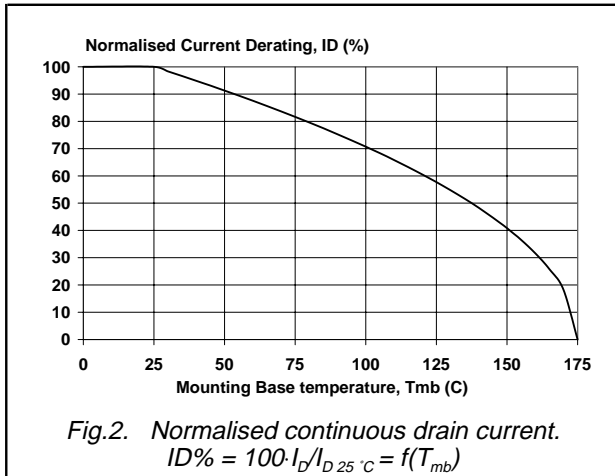
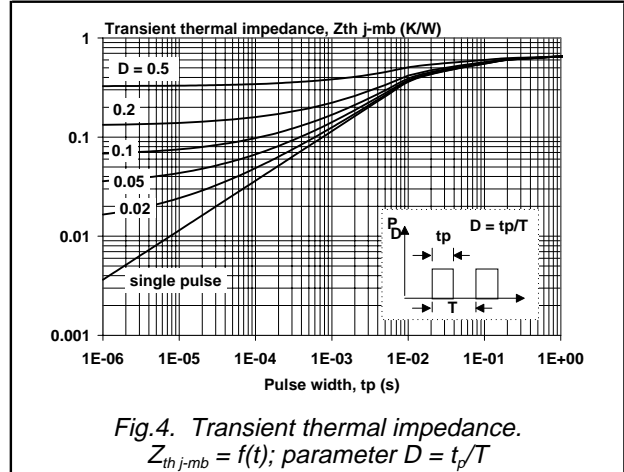
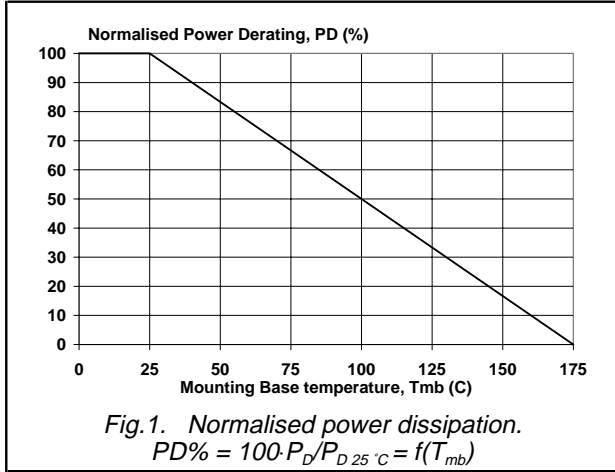
**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS** $T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_S$	Continuous source current (body diode)		-	-	75	A
$I_{SM}$	Pulsed source current (body diode)		-	-	240	A
$V_{SD}$	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
		$I_F = 75\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	-	
$t_{rr}$	Reverse recovery time	$I_F = 20\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s};$	-	400	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 25\text{ V}$	-	1	-	$\mu\text{C}$

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## N-channel logic level TrenchMOS™ transistor

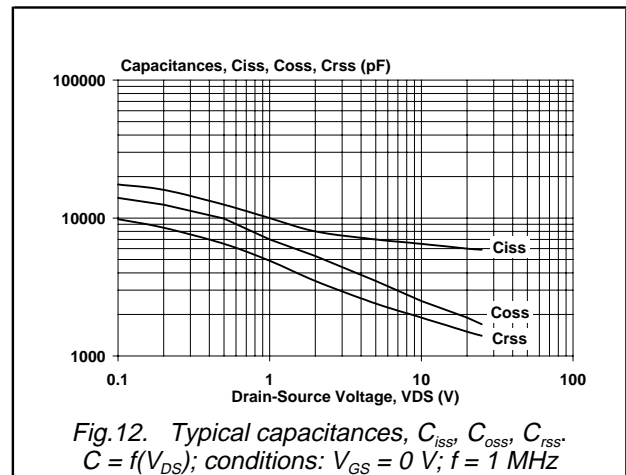
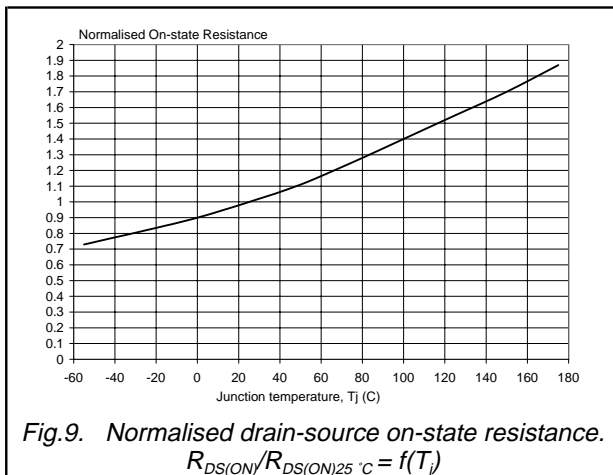
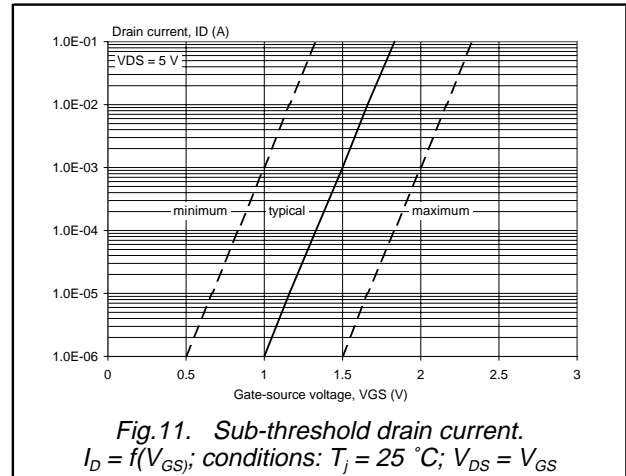
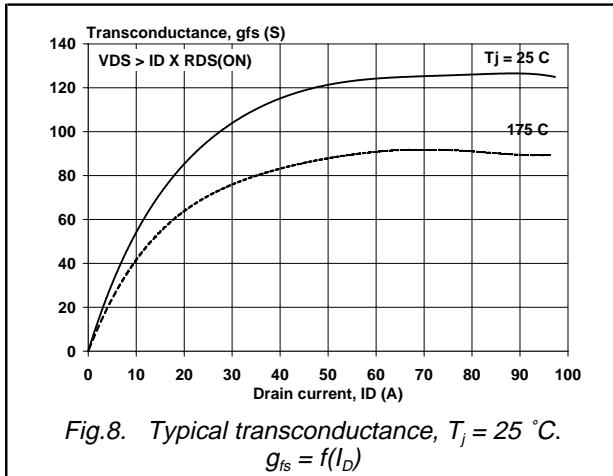
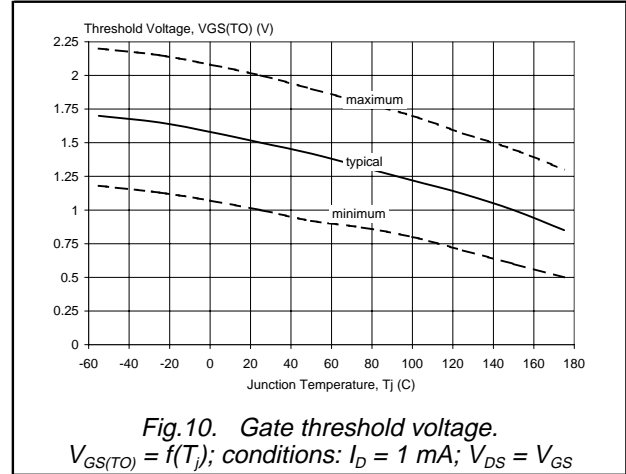
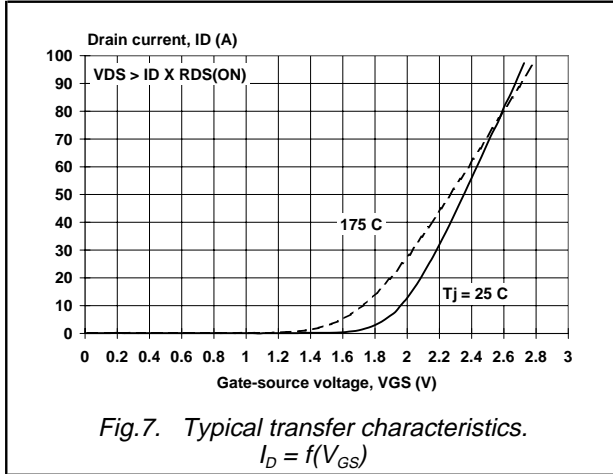
## PSMN004-25B, PSMN004-25P



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N-channel logic level TrenchMOS™ transistor

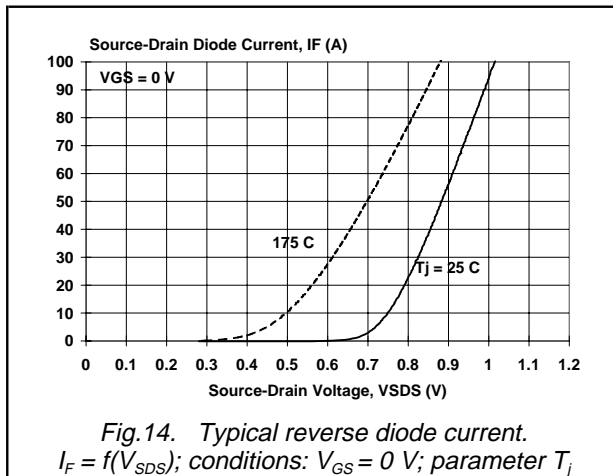
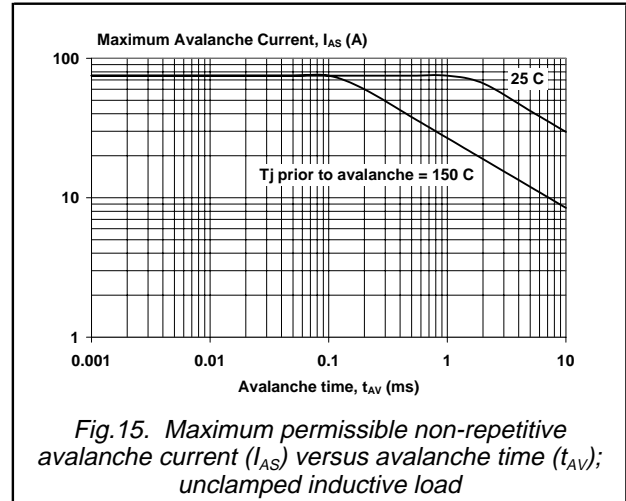
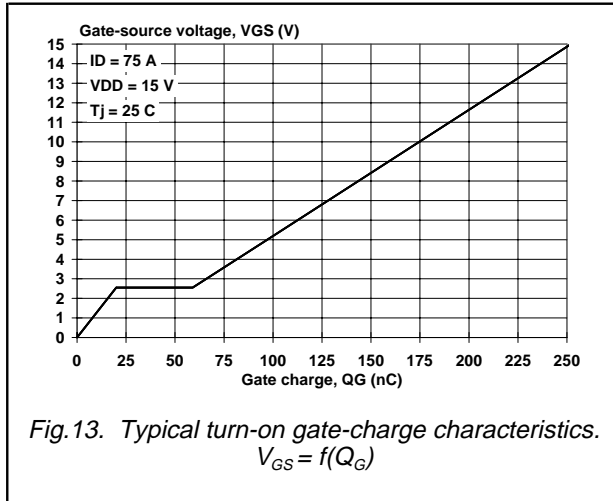
PSMN004-25B, PSMN004-25P





N-channel logic level TrenchMOS™ transistor

PSMN004-25B, PSMN004-25P





N-channel logic level TrenchMOS™ transistor

PSMN004-25B, PSMN004-25P

**MECHANICAL DATA**

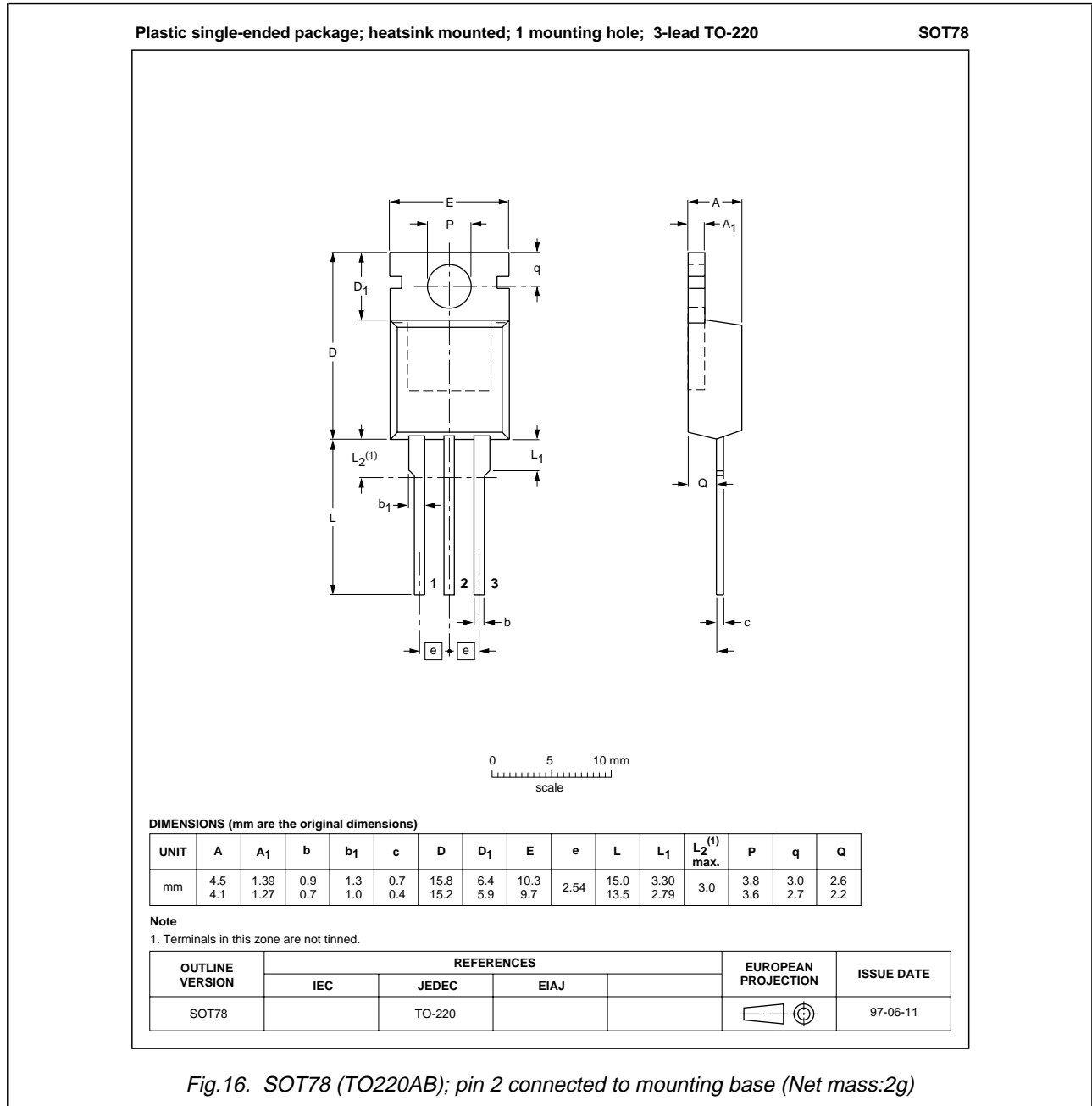


Fig. 16. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

**Notes**

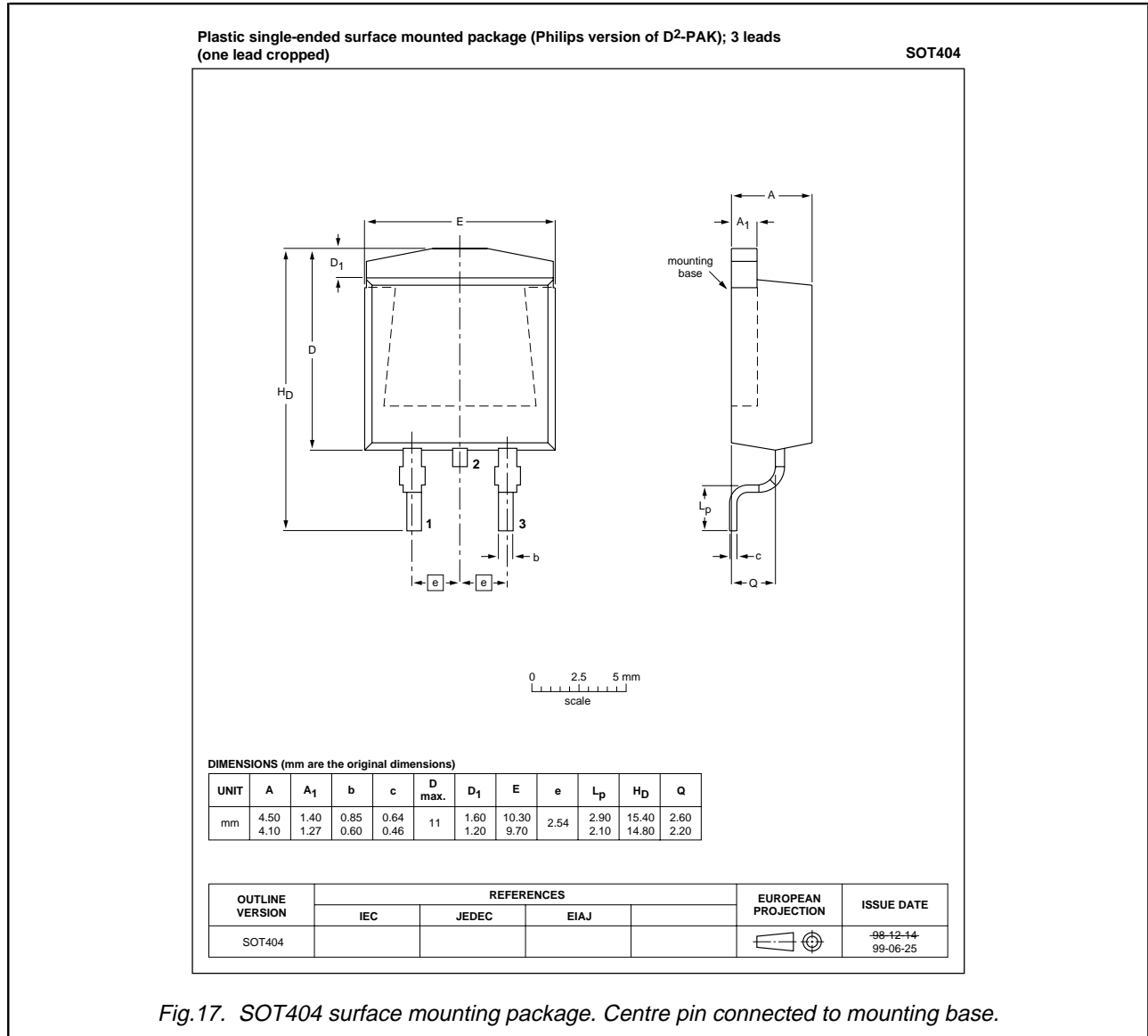
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".



N-channel logic level TrenchMOS™ transistor

PSMN004-25B, PSMN004-25P

**MECHANICAL DATA**



**Notes**

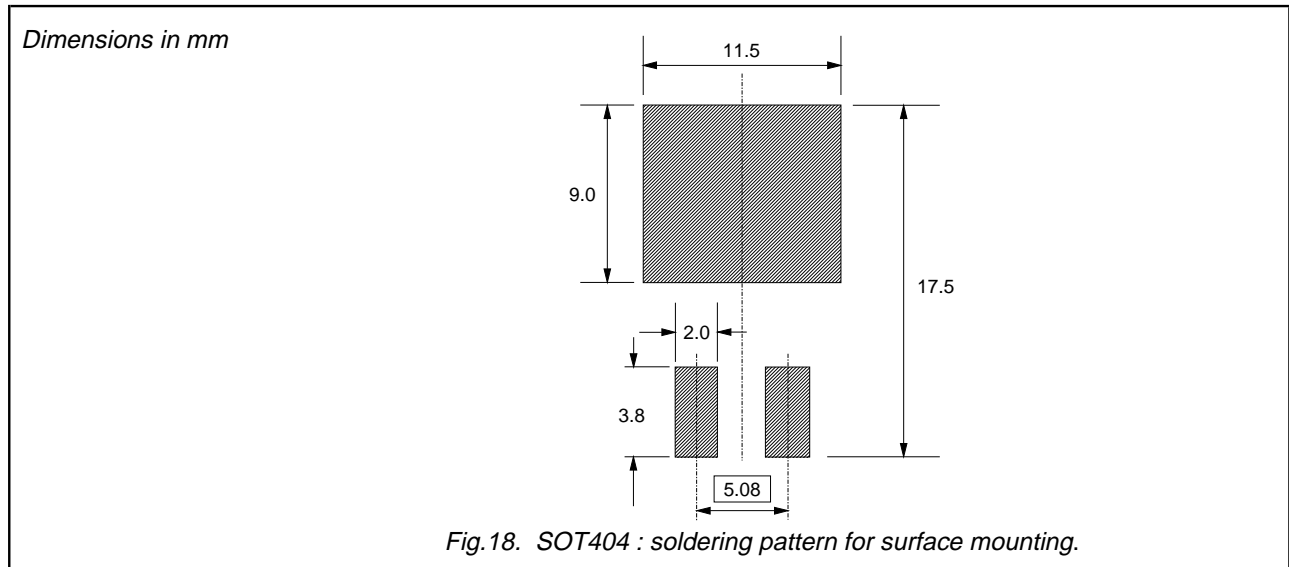
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".



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**MOUNTING INSTRUCTIONS****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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