SC2612E
500kHz Step-Down DC/DC Converter

Description

The SC2612E is a voltage mode switcher designed for low cost, “point of use” voltage conversion. SC2612E is available with fixed switching frequencies of 500kHz.

The SC2612E has soft start and enable functions and is short circuit protected. The output of the switcher may be set anywhere between 0.8V and 75% of Vin. Short circuit protection is disabled during start-up to allow the output capacitors time to fully charge.

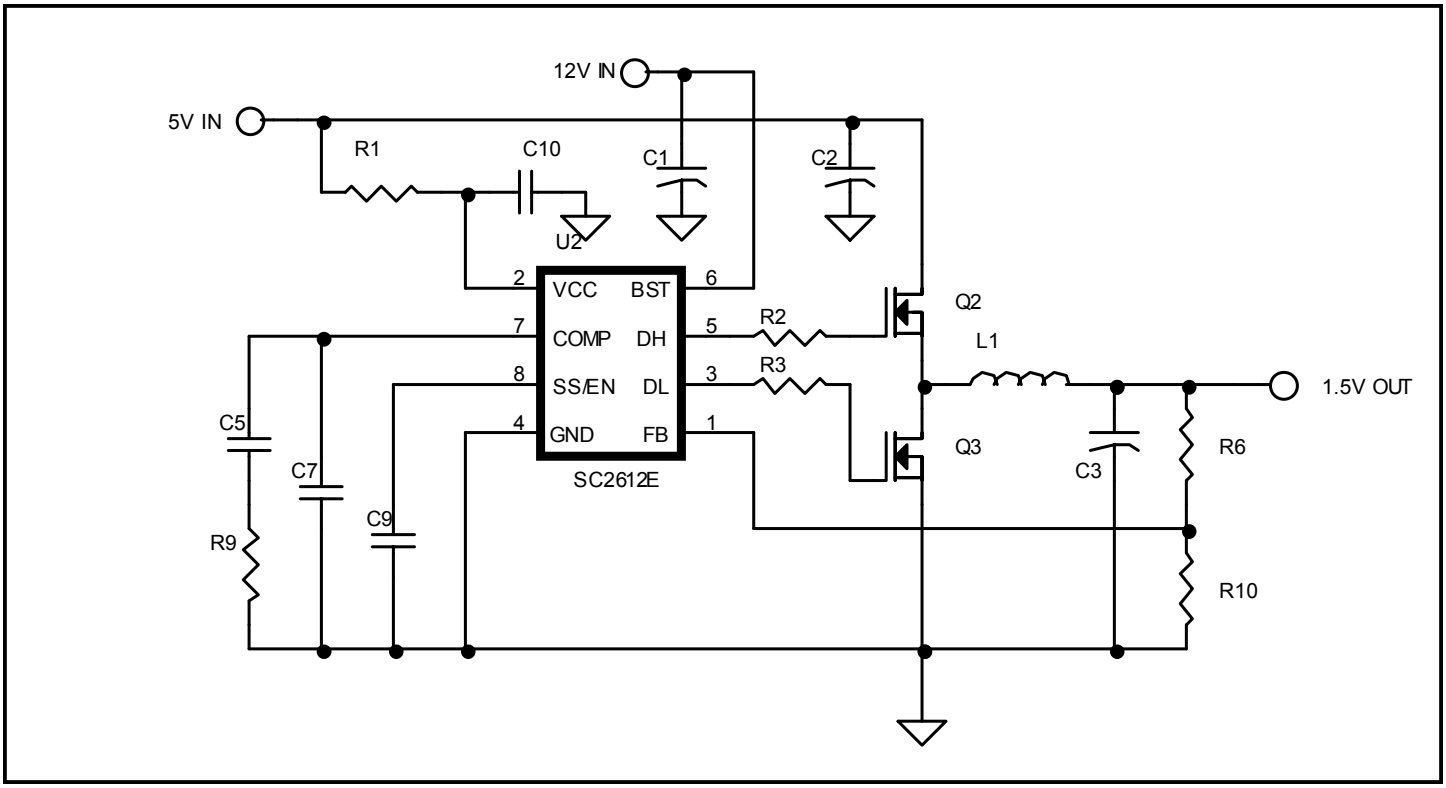
Features

- Operating frequency of 500kHz
- Input supply of 4.5V to 15V
- 0.5A Drive current for up to 10A output
- Output voltages down to 0.8V
- Overcurrent protection and soft start
- SO-8 package

Applications

- Graphics IC Power supplies
- Embedded, low cost, high efficiency converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
VCC Supply Voltage	V_{CC}	18	V
Boost Pin Voltage	V_{BST}	20	V
DL to GND (1), DH to GND (1)	V_{DLO}, V_{DHI}	-1 to +20	V
DH to GND Negative Pulse (t_{pulse} < 10ns)	V_{DH_PULSE}	-4.5	V
DL to GND Negative Pulse (t_{pulse} < 20ns)	V_{DL_PULSE}	-4.5	V
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature	T_J	125	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temperature (Soldering) 10s	T_{LEAD}	300	°C
Thermal Resistance Junction to Ambient (2)	θ_{JA}	113	°C/W
Thermal Resistance Junction to Case	θ_{JC}	42	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: V_{CC} = 4.5V to 12V; V_{FB} = V_O; BST = Vcc+5V; T_A = 0 to 70°C

Parameter	Symbol	Conditions		Min	Typ	Max	Units
VCC Supply Voltage	V_{CC}			4.5		15	V
VCC Quiescent Current	I_{QVCC}	V_{CC} = 5.0V, V_{BST} = 12.0V, SS/EN = 0V			5	10	mA
BST Supply Voltage	V_{BST}			4.5		18	V
BST Quiescent Current	I_{QBST}	V_{CC} = 5.0V, V_{BST} = 12.0V, SS/EN = 0V				5	mA
VCC Under Voltage Lockout	UV_{VCC}			3.8	4.15	4.5	V
BST Under Voltage Lockout	UV_{BST}			3.15	3.5	3.85	V
Output Voltage	V_{OS}	I_O = 10mA; V_{FB} = V_{OS}, T_A = 25°C		792	800	808	mV
Overcurrent trip voltage	V_{ITS}			0.4		0.7	V
Load Regulation		I_O = 0.2A to 4A			1		%
Line Regulation					±0.5		%
Oscillator Frequency	f_{OSC}			400	500	600	kHz
Oscillator Max Duty Cycle	δ_{MAX}			80			%
SS/EN Shutdown Voltage	V_{SS}			0.3		0.8	V
SS/EN Charge current	I_{SS}	Vss = 0.8V			25		µA
Peak DH Sink/Source Current		BST - DH = 4.5V,	DH - GND = 3.3V DH - GND = 1.5V	0.5 50			A mA
Peak DL Sink/Source Current		BST - DL = 4.5V,	DL - GND = 3.3V DL - GND = 1.5V	0.5 50			A mA

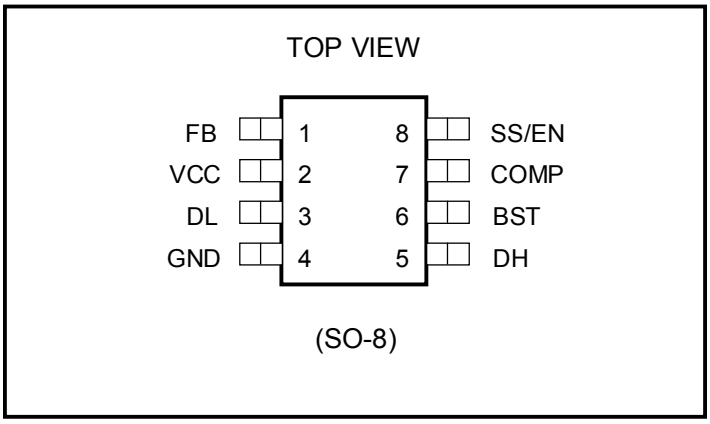
Electrical Characteristics

Unless specified: V_{CC} = 4.5V to 12V; V_{FB} = V_O; BST = Vcc+5V; T_A = 0 to 70°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Error Amplifier Transconductance (3)	gm			0.8		mS
Error Amplifier Gain (3)	A_{EA}	R_{COMP} = open		45		dB
Error Amplifier Source/Sink Current				±60		µA
Modulator Gain (3)	A_M	V_{CC} = 5V		19		dB
Dead Time				50		ns

Notes:
(1) See Gate Resistor selection recommendations.
(2) 1square inch of FR4, double sided, 1oz. minimum copper weight.
(3) Guaranteed by design, not tested in production.

Pin Configuration



Ordering Information

Part Numbers (1)	Frequency	Package
SC2612ESTRT (2)	500kHz	SO-8

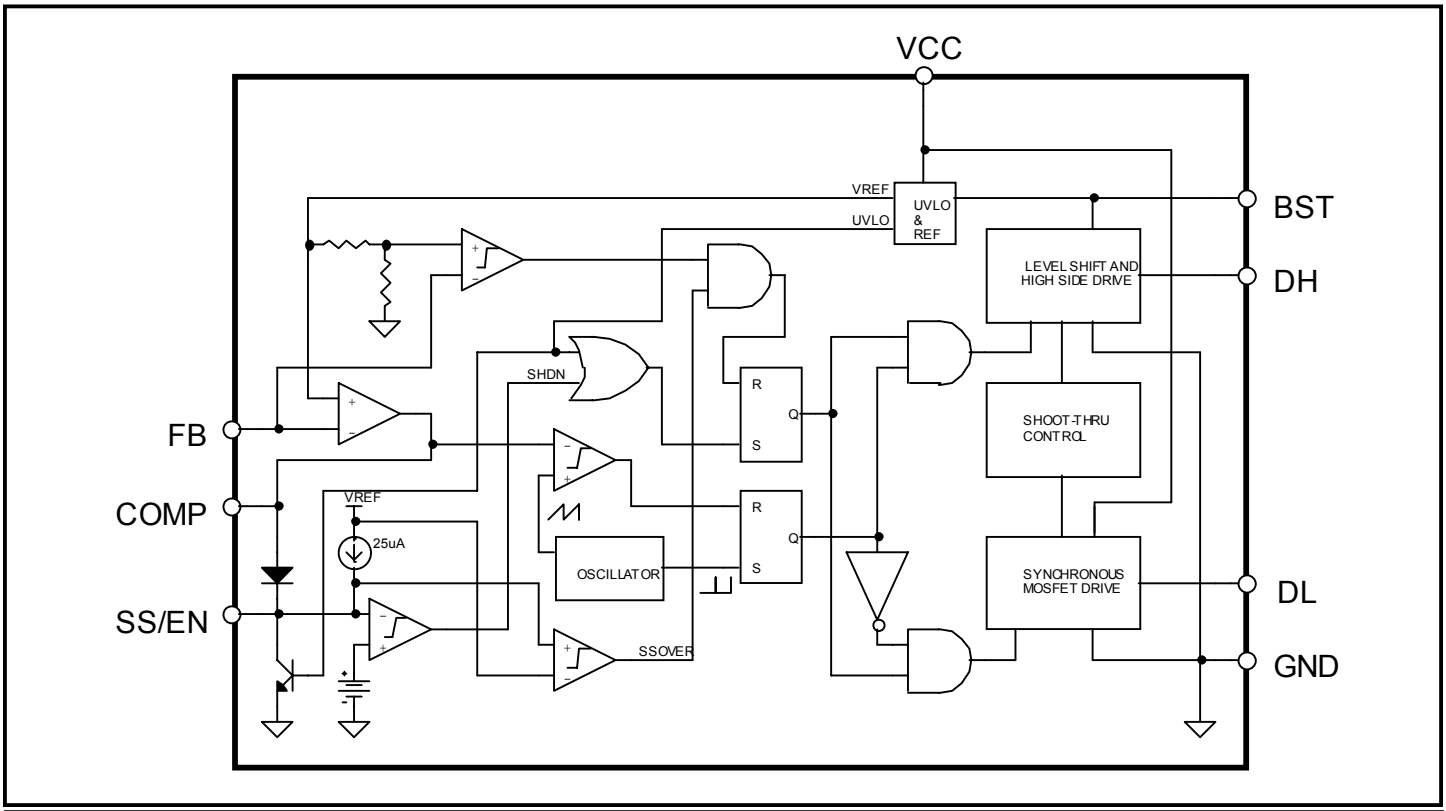
Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Switcher section feeedback input.
2	VCC	Chip Supply Input Voltage.
3	DL	Switcher Low side FET drive output.
4	GND	Analog and Power Ground, connect directly to ground plane, see layout guidelines.
5	DH	Switcher High side FET drive output.
6	BST	Supply voltage for FET drives.
7	COMP	Output of the Switcher section voltage error amplifier.
8	SS/EN	Soft start and enable pin, controls the switcher output voltage ramp rate.

Block Diagram



Theory of Operation

The SC2612E is a step down DC/DC controller designed for minimum cost and size without sacrificing accuracy and protection. Overcurrent protection is implemented by a simple undervoltage detection scheme and is disabled until soft start has been completed to eliminate false trips due to output capacitor charging. The SS/EN pin is held low, as are the DH and DL pins, until the undervoltage lockout points are exceeded. Once the VCC and BST pins both rise above their undervoltage lockout points, the SS capacitor begins to charge, controlling the duty cycle of the switcher, and therefore slowly ramping up the switcher output voltage. Once the SS capacitor is charged, the current limit circuitry is enabled. If a short circuit is applied , the output will be pulled down below it's trip point and shut down. The device may be restarted by either cycling power, or momentarily pulling SS/EN low.

Component Selection

OUTPUT INDUCTOR - A good starting point for output filter component selection is to choose an inductor value that will give an inductor ripple current of approximately 20% of max. output current.
Inductor ripple current is given by:-

$$I_{LRIPPLE} = \frac{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_{OSC}}$$

So choose inductor value from:-

$$L = \frac{5 \cdot V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{I_O \cdot f_{OSC}}$$

OUTPUT CAPACITOR(S) - The output capacitors should be selected to meet output ripple and transient response criteria. Output ripple voltage is caused by the inductor ripple current flowing in the output capacitor's ESR (There is also a component due to the inductor ripple current charging and discharging the output capacitor itself, but this component is usually small and can often be ignored). Given a maximum output voltage ripple requirement, ESR is given by:-

$$R_{ESR} < \frac{V_O \cdot V_{RIPPLE} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_{OSC}}$$

Output voltage transient excursions are a function of load current transient levels, input and output voltages and inductor and capacitor values.
Capacitance and R_{ESR} values to meet a required transient condition can be calculated from:-

$$R_{ESR} < \frac{V_T}{I_T}$$

$$C > \frac{L \cdot I_T^2}{2 \cdot V_T \cdot V_A}$$

where

$V_A = V_{IN} - V_O$ for negative transients (load application)

and

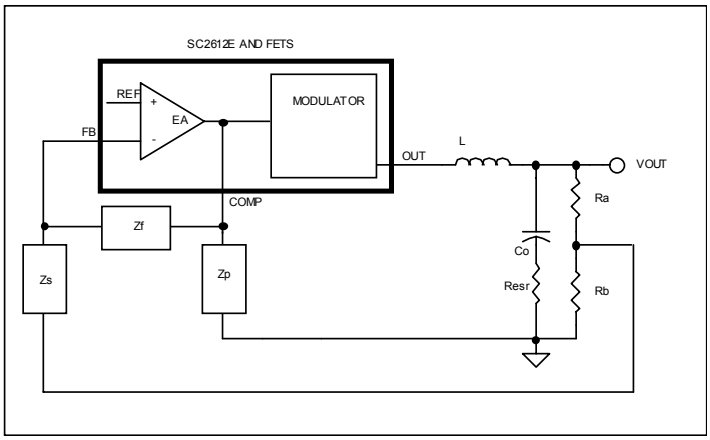
$V_A = V_O$ for positive transients (load release)

values for positive and negative transients must be calculated seperately and the worst case value chosen. For Capacitor values, the calculated value should be doubled to allow for duty cycle limitation and voltage drop issues.

COMPENSATION COMPONENTS - Once the filter components have been determined, the compensation components can be calculated. The goal of compensation is to modify the frequency response characteristics of the error amplifier to ensure that the closed loop feedback system has the highest gain and bandwidth possible while maintaining stability.

A simplified stability criteria states that the open loop gain of the converter should fall through 0dB at 20dB/decade at a frequency no higher than 20-25% of the switching frequency.

This objective is most simply met by generating asymptotic bode plots of the small signal response of the various sections of the converter.



It is convenient to split the converter into two sections, the Error amp and compensation components being one section and the Modulator, output filter and divider being the other.

First calculate the DC Filter+Modulator+Divider gain

The DC filter gain is always 0dB, the Modulator gain is 19dB at 5V in and is proportional to Vin, so modulator gain at any input voltage is.

$$G_{MOD} = 19 + 20 \cdot \mathrm{Log}\left(\frac{V_{IN}}{5}\right)$$

the divider gain is given by

$$G_{DIV} = 20 \cdot \mathrm{Log}\left(\frac{R_8}{R_5 + R_8}\right)$$

So the total Filter+Modulator+Divider DC Gain is

$$G_{FMD} = 19 + 20 \cdot \mathrm{Log}\left(\frac{V_{IN}}{5}\right) + 20 \cdot \mathrm{Log}\left(\frac{R_B}{R_A + R_B}\right)$$

Calculate the filter double pole frequency (Fp(lc))

$$\mathrm{Fp(lc)} = \frac{1}{2\pi\sqrt{\mathrm{LCo}}}$$

and calculate ESR Zero frequency (Fz(esr))

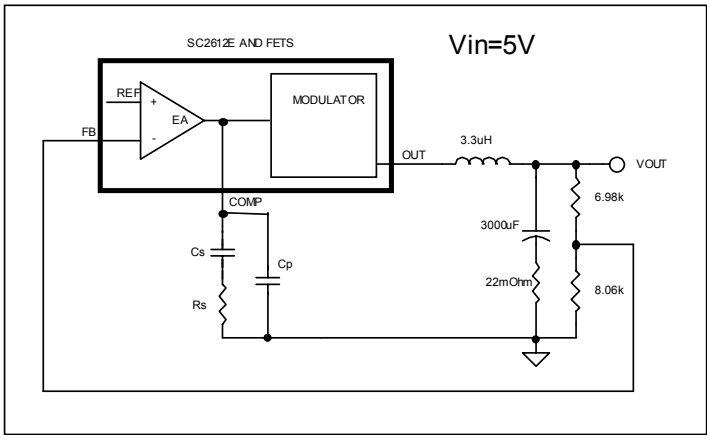
$$\mathrm{Fz(esr)} = \frac{1}{2\pi \cdot \mathrm{Co} \cdot \mathrm{Resr}}$$

Choose an open loop crossover frequency (Fco) no higher than 20% of the switching frequency (Fs).

The proximity of Fz(esr) to the crossover frequency Fco determines the type of compensation required, if Fz(esr)>Fco/4, use type 3 compensation, otherwise use type 2. Type 1 compensation is not appropriate and is not discussed here.

Type 2 Example

As an example of type 2 compensation, we will use the Evaluation board schematic.



The total Filter+Modulator+Divider DC Gain is

$$G_{FMD} = 19 + 20 \cdot \mathrm{Log}\left(\frac{5}{5}\right) + 20 \cdot \mathrm{Log}\left(\frac{8.06}{6.98 + 8.06}\right) = 13.6\mathrm{dB}$$

This is drawn as the line A-B in Fig2

$$\mathrm{Fp(lc)} = \frac{1}{2\pi\sqrt{\mathrm{LCo}}} = \frac{1}{2\pi\sqrt{3.3 \cdot 10^{-6} \cdot 3000 \cdot 10^{-6}}} \approx 1.6\mathrm{kHz}$$

This is point B in Fig2.

$$\mathrm{Fz(esr)} = \frac{1}{2\pi \cdot 3000 \cdot 10^{-6} \cdot 22 \cdot 10^{-3}} = 2.4\mathrm{kHz}$$

This is point C in Fig2., the line joining B-C slopes at -40dB/decade, the line joining C-D slopes at -20dB/decade.

For 500kHz switching frequency, crossover is designed for 100kHz.

Since Fz(esr)<<Fco/4 Type 2 compensation is appropriate.

Having plotted the line ABCD, and confirmed the type of compensation necessary, compensation component values can be determined.

At Fco, the line ABCD shows a gain of -27.5dB and a slope of -20dB/decade. In order for the total open loop gain to be 0dB with a -20dB/decade slope at this frequency, the compensated error amp gain at Fco must be +27.5dB with a 0dB slope. This is the line FG on the plot below.

Since open loop DC gain should be as high as possible to minimize errors, a zero is placed at F and to minimize high frequency gain and switching interference a pole is placed at G.

The zero at F should be no higher than Fco/4 and the pole at G no lower than 4*Fco. The equations to set the gain and the pole and zero locations are:

$$Rs = \frac{10^{\frac{A}{20}}}{gm} \quad \text{where A = gain at Fco (in dB)}$$

$$Cs = \frac{1}{2\pi \cdot Fz1 \cdot Rs}$$

$$Cp = \frac{1}{2\pi \cdot Fp1 \cdot Rs}$$

For this example, this results in the following values.

$$Rs = \frac{10^{\frac{27.5}{20}}}{0.8} = 29.6k\Omega \approx 30k\Omega$$

$$Cs \approx \frac{1}{6 \cdot 25 \cdot 10^3 \cdot 30 \cdot 10^3} = 0.22nF$$

$$Cp \approx \frac{1}{6 \cdot 400 \cdot 10^3 \cdot 30 \cdot 10^3} = 14pF \text{ (unecessary due to EA rolloff)}$$

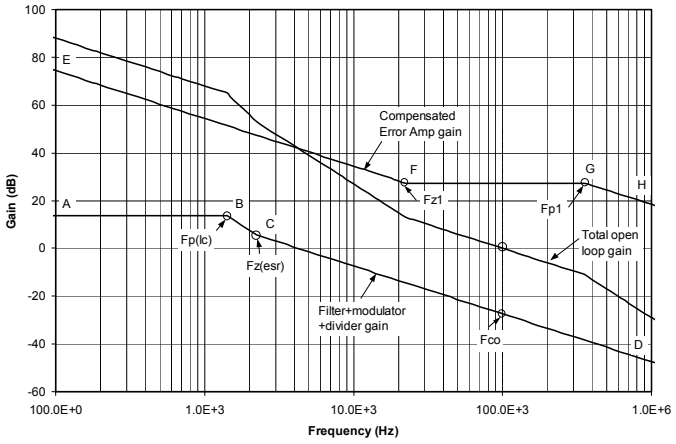
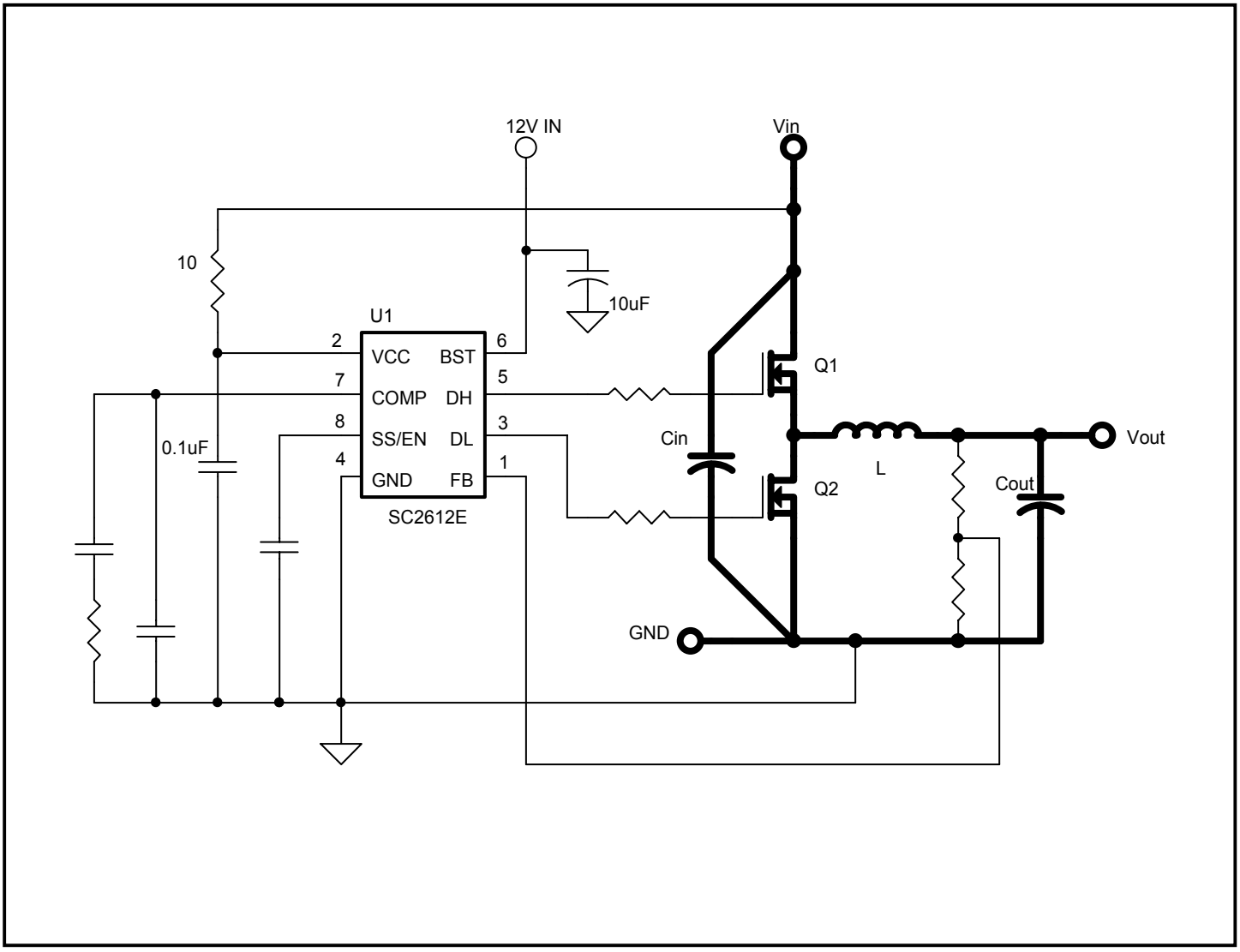


Fig2: Type 2 Error Amplifier Compensation

Layout Guidelines

Careful attention to layout requirements are necessary for successful implementation of the SC2612E PWM controller. High currents switching at high frequency are present in the application and their effect on ground plane voltage differentials must be understood and minimized.
1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.
2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.
3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the output capacitors should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.

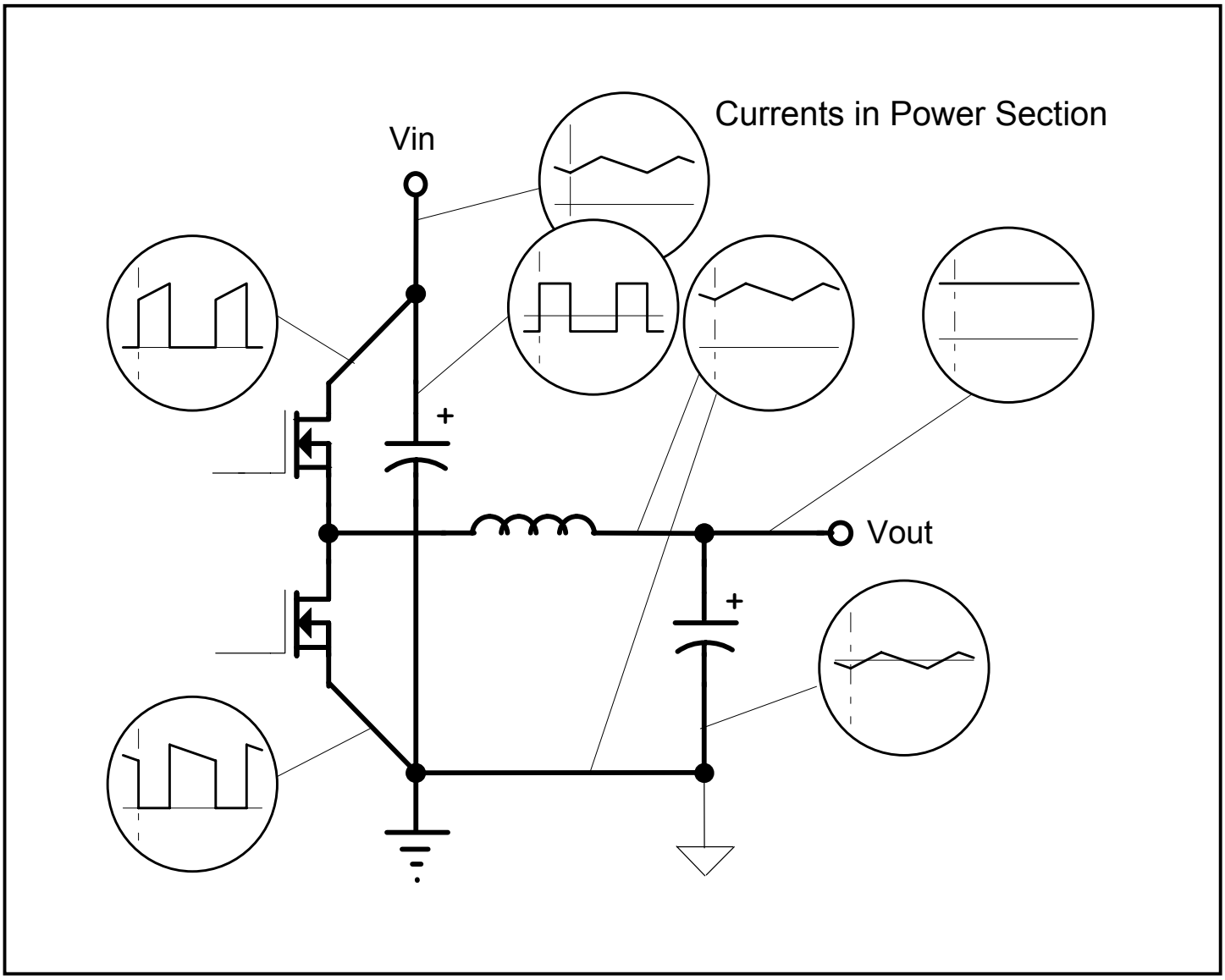


Layout Guidelines (Cont.)

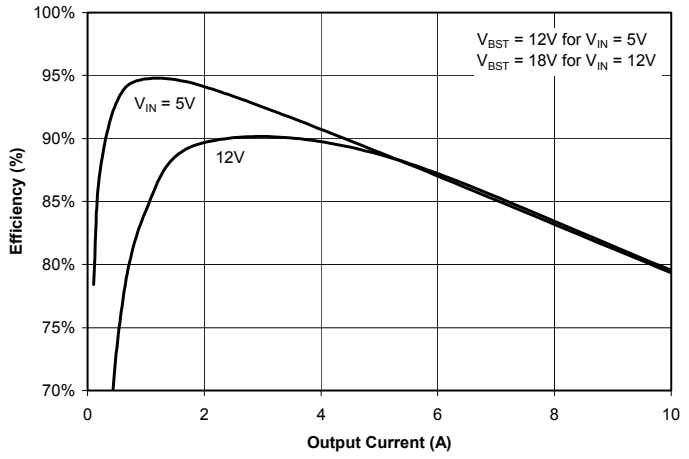
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC2612E is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. PGNDH and PGNDL should be returned to the ground plane close to the package. The AGND pin should be connected to the ground side of (one of) the output capacitor(s). If this is not possible, the AGND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should AGND be returned to a ground inside the Cin, Q1, Q2 loop.

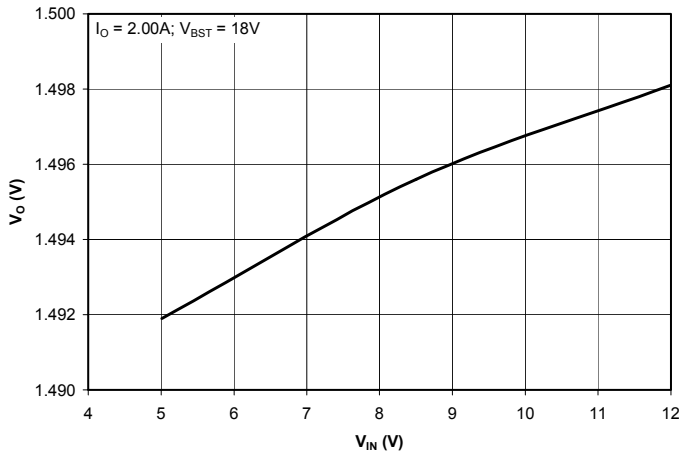
6) Vcc for the SC2612E should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to AGND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.



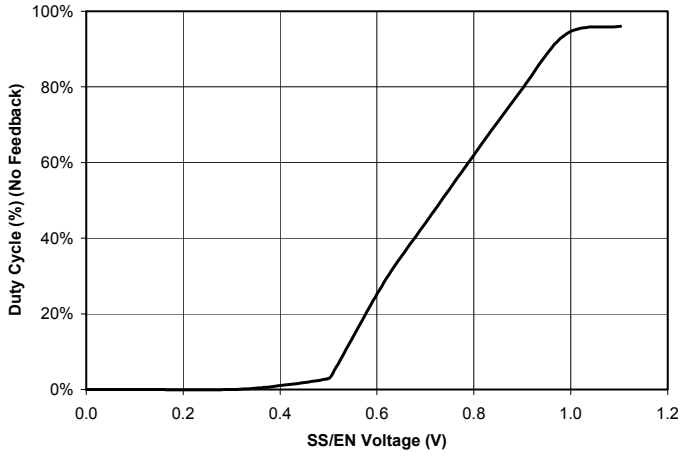
Typical Characteristics



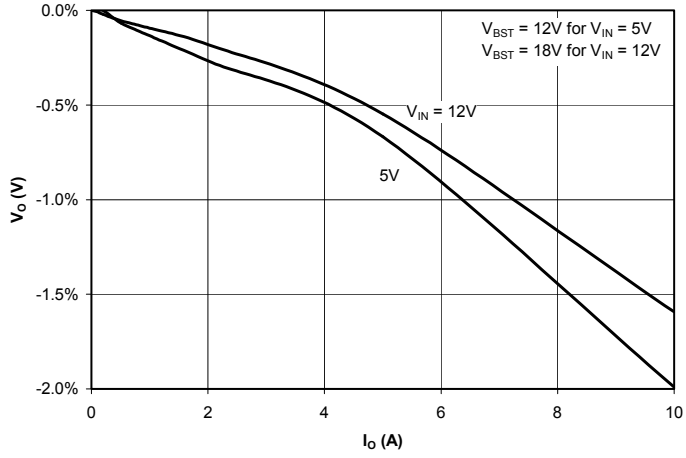
Typical Efficiency



Typical Line Regulation

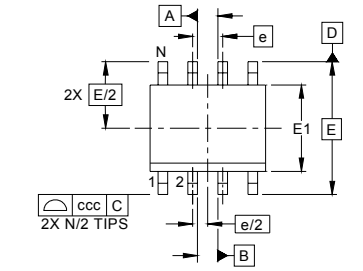


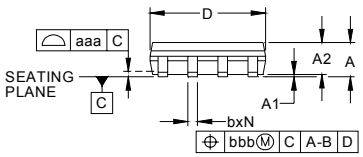
SS/EN Control of duty cycle

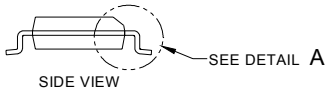


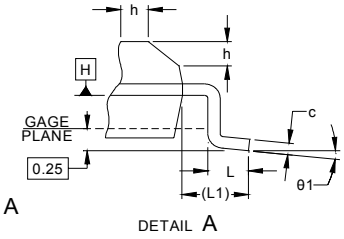
Typical Load Regulation

Outline Drawing - SOIC-8







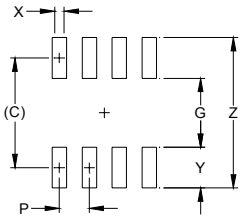


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SOIC-8



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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