UFX7000

USB 3.0 Super-Speed Graphics Controller with VGA, HDMI/DVI, and Digital RGB Interfaces

PRODUCT FEATURES

Data Brief

Highlights

- Single-Chip Super-Speed USB 3.0 Graphics Adapter
- USB 3.0 and 2.0 Device Controllers with Integrated USB 3.0 and 2.0 PHYs
- High Efficiency USB Graphics Adapter
- HDMI/DVI Display Connectivity via Integrated HDMI/DVI Controller/PHY
- VGA Display Connectivity via Integrated Video DAC
- Support for External Display Interface IC's via Digital RGB Interface
- High Performance DDR2 SDRAM Controller with Integrated DDR2 PHY

Target Applications

- USB to Video Adapters
- Docking Stations, USB Port Replicators
- Thin Clients
- USB Monitors and Projectors
- Embedded Systems

Features

- USB 3.0 and 2.0 Device Controllers
  - Fully compliant with Universal Serial Bus Specification Revision 3.0
  - Operates in SS (5 Gbps) and HS (480 Mbps) modes
  - Supports Control, Bulk-Out, and Interrupt-In endpoints
  - Supports vendor specific commands
  - Integrated USB 3.0 and 2.0 PHYs
  - Integrated USB termination pull-up/pull-down resistors
  - Short circuit protection of USB differential signals
- USB Graphics Adapter
  - Integrated HDMI/DVI Controller and PHY
    - Complies with DVI specification v1.0
    - Complies with HDMI specification v1.3
    - S/PDIF and I^2S inputs for HDMI audio (2-channel uncompressed PCM)
    - Master I^2C interface for DDC connection
  - Integrated Triple 10-bit Video DAC with VGA output
  - Digital RGB Interface
    - 12/15-bit double data rate digital RGB
    - 24-bit single data rate digital RGB
  - Supports up to 2048x1152 (QWXGA) with 32-bit color
  - 8-bit and 16-bit color support
  - Supports display cloning and extending
  - Standard and wide screen aspect ratios
  - Complies with VESA auto display identification
  - Gamma correction
  - Color Look-Up Table (CLUT)
  - Triple-buffered animations
  - Graphics Engine
    - Optimized algorithms for static and dynamic content
    - I^2C controller
- DDR2 SDRAM Controller
  - 16-bit data bus, 13-bit address bus
  - JEDEC DDR2 compliant (JESD79-2E)
  - Integrated DDR2 SDRAM PHY
- Power
  - Reduced power operating modes
  - Supports bus-powered and self-powered operation
- Miscellaneous Features
  - Optional EEPROM controller
  - IEEE 1149.1 (JTAG) boundary scan TAP controller
- Software
  - Microsoft Windows® XP/Vista/7 drivers
- Packaging & Environmental
  - 225-ball LFBGA, lead-free RoHS compliant package
  - Commercial temperature range (0°C to +70°C)

Order Number:

UFX7000-VE for 225-Ball LFBGA lead-free RoHS compliant package (0 to +70°C temp range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The UFX7000 is a high performance USB 3.0 graphics adapter with multiple graphics interfaces. The UFX7000 is an ideal solution for extending a PC workspace to an additional monitor without the need for an additional internal graphics card. With applications ranging from docking stations, USB port replicators, USB monitors/projectors, and embedded systems, the UFX7000 is targeted as a high performance, low cost USB-to-graphics solution.

The UFX7000 contains integrated USB 3.0 and 2.0 Device Controllers, USB 3.0 and 2.0 PHYs, a USB Bulk-Out Controller, Control Endpoint, Interrupt-In Endpoint, DDR2 SDRAM Controller/PHY, Graphics Engine, HDMI/DVI Controller/PHY, Video DAC, TAP Controller, EEPROM Controller, and I^2C Controller. Figure 1 details an internal block diagram of the UFX7000.

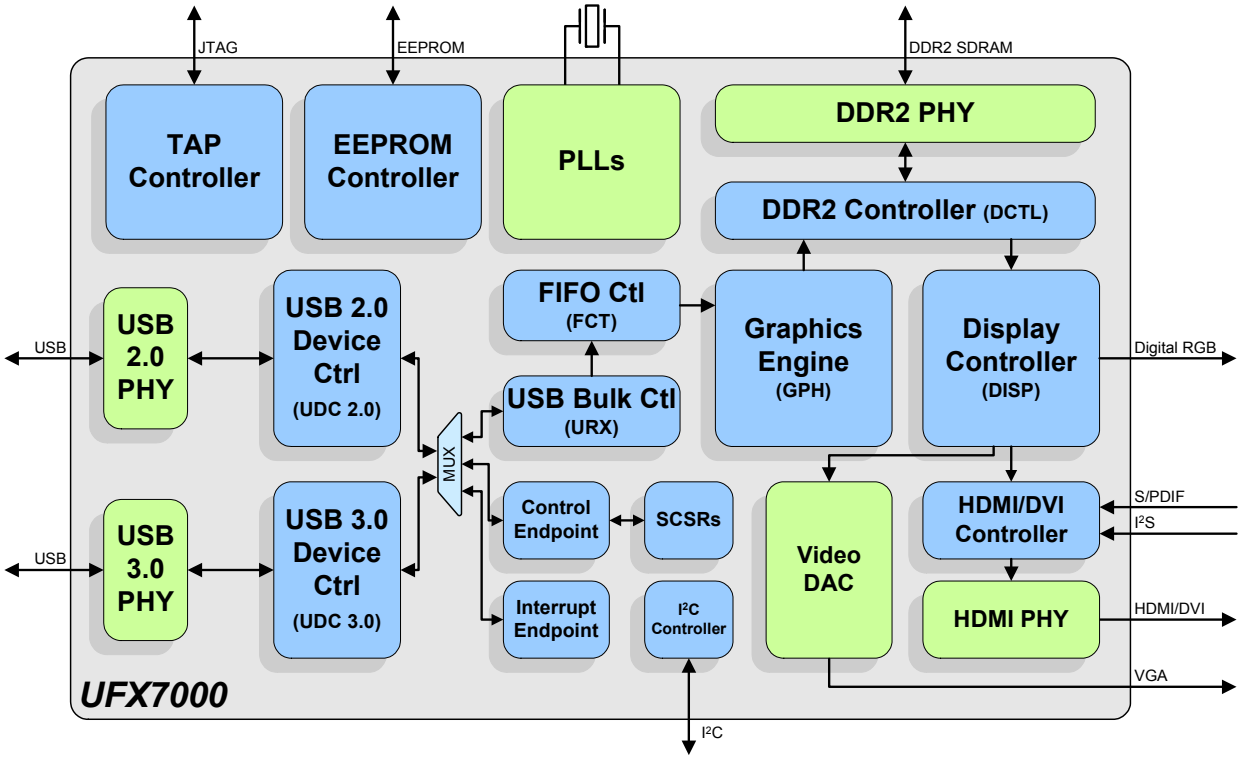


Figure 1 Internal Block Diagram

USB DEVICE CONTROLLER

The USB Device Controller is fully compliant with the USB 3.0 Specification, enabling the device to operate in Super-Speed (5 Gbps) or Hi-Speed (480 Mbps) mode. Integrated USB 3.0 and 2.0 PHYs are provided on the USB port.

The controller implements three USB endpoints: Control, Bulk-Out, and Interrupt-In. The Bulk-Out endpoint allows for uncompressed or compressed graphics data reception from the USB port. The USB Bulk-Out Controller collects the graphics information and transfers it to the Graphics Engine. Implementation of vendor-specific commands allows for access to the device System Control and Status Registers (SCSRs).

USB GRAPHICS ADAPTER

The USB Graphics Adapter consists of the following main blocks: the Graphics Engine, Display Controller, HDMI/DVI Controller/PHY, Video DAC, and the Digital RGB Interface. Together, these blocks support high definition resolutions of up to 2048x1152 (QWXGA) with 32-bit true color in both standard and wide screen aspect ratios. The HDMI/DVI interface is compliant with the HDMI v1.3 and DVI v1.0 specifications and supports 2-channel uncompressed PCM audio via a S/PDIF or I^2S input. The Display Controller also supports 8-bit and 16-bit color, gamma correction, Color Look-Up Table (CLUT) and triple-buffered animation. The DDC2B/EDID VESA standard is supported, allowing the host OS and device drivers to query the monitor's frequency, resolution, and other features for true plug-and-play and intelligent mode setting capabilities.

Once the graphics data has been received via the USB Bulk-Out Controller, it is sent to the Graphics Engine. If the data is compressed, the Graphics Engine decompresses it via algorithms that have been optimized for speed and quality. The device's decompression algorithms have been designed to work seamlessly with the compression algorithms utilized in the software device drivers.

The graphics data is then transferred to the SDRAM via the DDR2 SDRAM Controller. The Display Controller generates all display and interface timing signals, retrieves the graphics data from the DDR2 SDRAM, and sends it to the HDMI/DVI Controller/PHY, Video DAC, or Digital RGB Interface.

The Digital RGB Interface may be used to connect external display interface IC's (e.g., DisplayPort, etc.) via the provided RGB data channel busses and control signals. The Digital RGB Interface supports two modes of operation: 24-bit single data rate mode and 12/15-bit double data rate mode. 24-bit mode is single edge triggered and utilizes the full 24-bit data bus width. The 12/15-bit mode is triggered on both clock edges and utilizes 12/15-bits of the data bus width.

DDR2 SDRAM INTERFACE

The UFX7000 provides a full JEDEC compliant (JESD79-2E) DDR2 SDRAM Controller and PHY for interfacing to external DDR2 SDRAM. The DDR2 SDRAM interface is comprised of JEDEC standard 1.8V I/O signals grouped into control signals, a 16-bit data bus, and a 13-bit address bus.

The DDR2 SDRAM Controller transfers the graphics data in and out of external SDRAM through the DDR2 SDRAM PHY. External SDRAM is used as storage for the graphics and acts a a buffer between the Graphics Engine and Display Controller.

PERIPHERALS

The UFX7000 also contains an EEPROM Controller, I^2C Controller, and TAP Controller.

The EEPROM Controller allows connection to an external EEPROM for automatic loading of static configuration data upon power-on, pin reset, or software reset. The EEPROM can be configured to load USB descriptors and USB device configuration.

The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

Package Outline

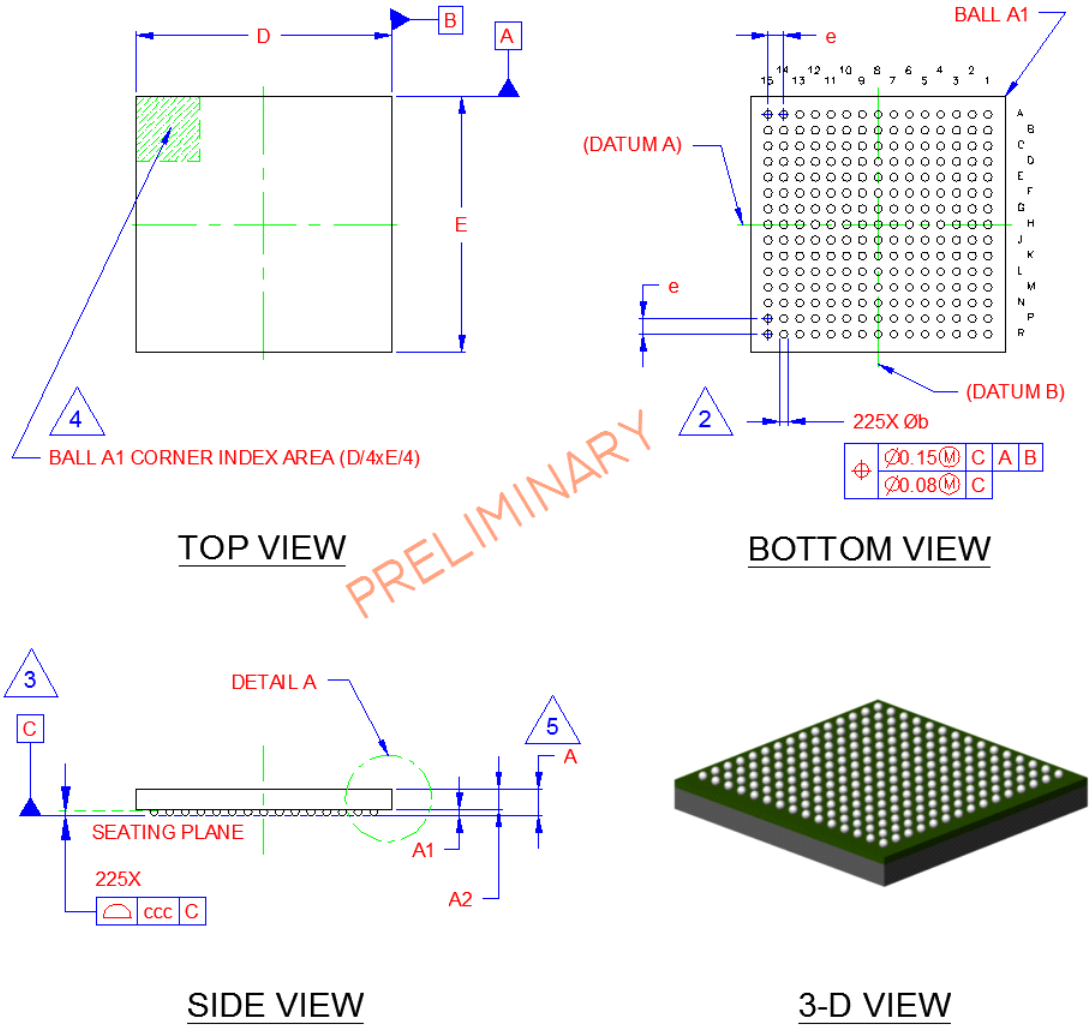


Figure 2 225-Ball LFBGA Package

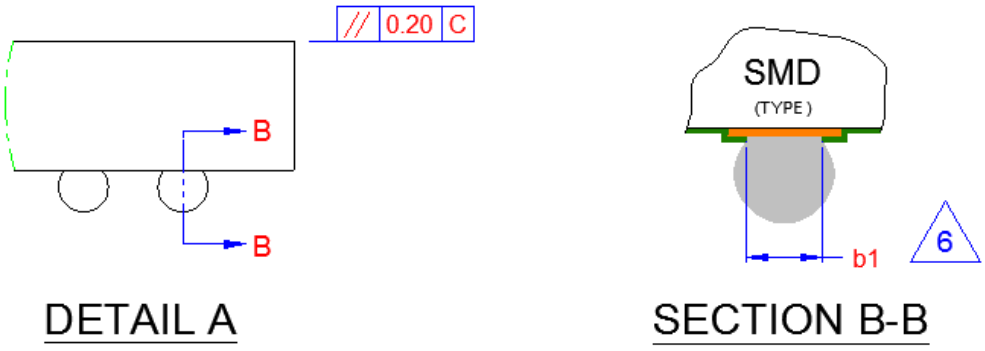


Figure 3 225-Ball LFBGA Package Ball Detail

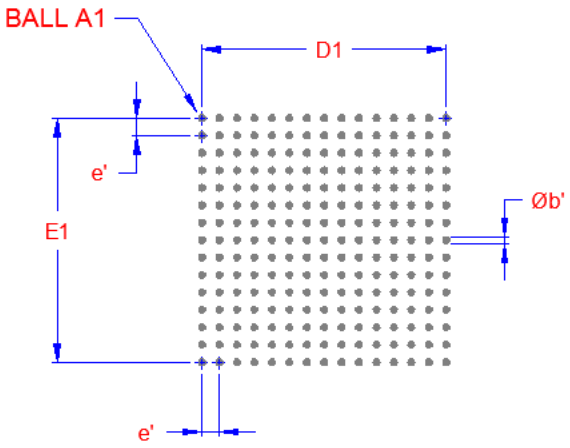
PRODUCT PREVIEW

Table 1 225-Ball LFBGA Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	-	1.30	1.40	Overall Package Height
A1	0.25	-	0.40	Standoff
A2	0.65	0.96	-	Package Body Thickness
D/E	12.90	13.00	13.10	Overall Package Size
b	0.40	0.45	0.50	Ball Diameter
b1	0.35	0.40	0.45	Package Ball Solderable Surface
e		0.80 BSC		Ball Pitch
ccc	-	-	0.20	Coplanarity

Notes:

1. All dimensions are in millimeters.
2. Dimension “b” is measured at the maximum ball diameter, parallel to primary datum “C”.
3. Primary datum “C” (seating plane) is defined by the spherical crowns of the contact balls.
4. The ball A1 identifier may vary, but is always located within the zone indicated.
5. Dimension “A” does not include attached external features, such as heat sink or chip capacitors.
6. The package ball solderable surface may be a Solder-Mask-Defined (SMD) or Non-Solder-Mask-Defined (NSMD) type. For NSMD type designs, exposed copper traces are permitted outside the “b1” pad area.



PCB LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1/E1		11.20 BSC	
b'	0.35	0.40	-
e'		0.80 BSC	

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

Figure 4 Recommended PCB Land Pattern

PRODUCT PREVIEW