19-2016; Rev 1; 4/05

MAXIM

Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

General Description

The MAX4245/MAX4246/MAX4247 family of low-cost op amps offer rail-to-rail inputs and outputs, draw only 320µA of quiescent current, and operate from a single +2.5V to +5.5V supply. For additional power conservation, the MAX4245/MAX4247 offer a low-power shutdown mode that reduces supply current to 50nA, and puts the amplifiers' outputs in a high-impedance state. These devices are unity-gain stable with a 1MHz gain-bandwidth product driving capacitive loads up to 470pF.

The MAX4245/MAX4246/MAX4247 family is specified from -40°C to +125°C, making them suitable for use in a variety of harsh environments, such as automotive applications. The MAX4245 single amplifier is available in ultra-small 6-pin SC70 and space-saving 6-pin SOT23 packages. The MAX4246 dual amplifier is available in 8-pin SOT23, SO, and µMAX® packages. The MAX4247 dual amplifier comes in a tiny 10-pin µMAX package.

Features

- ♦ **Rail-to-Rail Input and Output Voltage Swing**
- ♦ **50nA (max) Shutdown Mode (MAX4245/MAX4247)**
- ♦ **320µA (typ) Quiescent Current Per Amplifier**
- ♦ **Single +2.5V to +5.5V Supply Voltage Range**
- ♦ **110dB Open-Loop Gain with 2kΩ Load**
- ♦ **0.01% THD with 100kΩ Load**
- ♦ **Unity-Gain Stable up to C_{LOAD} = 470pF**
- ♦ **No Phase Inversion for Overdriven Inputs**
- ♦ **Available in Space-Saving Packages**
  6-Pin SC70 or 6-Pin SOT23 (MAX4245)
  8-Pin SOT23/SO or 8-Pin µMAX (MAX4246)
  10-Pin µMAX (MAX4247)

Applications

Portable Communications

Single-Supply Zero-Crossing Detectors

Instruments and Terminals

Electronic Ignition Modules

Infrared Receivers

Sensor-Signal Detection

Ordering Information

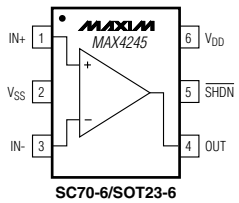
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4245AXT-T	-40°C to +125°C	6 SC70-6	AAZ
MAX4245AUT-T	-40°C to +125°C	6 SOT23-6	AAUB
MAX4246AKA-T	-40°C to +125°C	8 SOT23-8	AAIN
MAX4246ASA	-40°C to +125°C	8 SO	—
MAX4246AUA	-40°C to +125°C	8 µMAX	—
MAX4247AUB	-40°C to +125°C	10 µMAX	—

Selector Guide

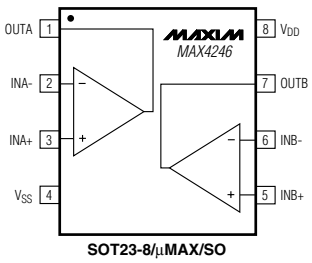
PART	AMPLIFIERS PER PACKAGE	SHUTDOWN MODE
MAX4245AXT-T	1	Yes
MAX4245AUT-T	1	Yes
MAX4246AKA-T	2	No
MAX4246ASA	2	No
MAX4246AUA	2	No
MAX4247AUB	2	Yes

Pin Configurations

TOP VIEW



SC70-6/SOT23-6



SOT23-8/µMAX/SO

Pin Configurations continued at end of data sheet.

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Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{DD} to V_{SS}) .....-0.3V to +6V
All Other Pins .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Output Short-Circuit Duration
(OUT shorted to V_{SS} or V_{DD})..... Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....695mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
8-Pin SOT23 (derate 9.1mW/°C above +70°C).....727mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L connected from OUT to V_{DD} / 2, $\overline{SHDN\_}$ = V_{DD} (MAX4245/MAX4247 only), **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test		2.5		5.5	V
Supply Current (Per Amplifier)	I_{DD}	V_{DD} = +2.7V			320	650	µA
		V_{DD} = +5.5V			375	700	
Supply Current in Shutdown	$I_{\overline{SHDN\_}}$	$\overline{SHDN\_}$ = V_{SS} (Note 2)			0.05	0.5	µA
Input Offset Voltage	V_{OS}	V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V			±0.4	±1.5	mV
Input Bias Current	I_B	V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V			±10	±50	nA
Input Offset Current	I_{OS}	V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V			±1	±6	nA
Input Resistance	R_{IN}	$\lvert V_{IN+} - V_{IN-} \rvert$ ≤ 10mV			4000		kΩ
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		V_{SS} - 0.1		V_{DD} + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V		65	80		dB
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{DD} ≤ 5.5V		75	90		dB
Large-Signal Voltage Gain	A_V	V_{SS} + 0.05V ≤ V_{OUT} ≤ V_{DD} - 0.05V, R_L = 100kΩ			120		dB
		V_{SS} + 0.2V ≤ V_{OUT} ≤ V_{DD} - 0.2V, R_L = 2kΩ		95	110		
Output Voltage Swing High	V_{OH}	Specified as V_{DD} - V_{OUT}	R_L = 100kΩ		1		mV
			R_L = 2kΩ		35	60	
Output Voltage Swing Low	V_{OL}	Specified as V_{OUT} - V_{SS}	R_L = 100kΩ		1		mV
			R_L = 2kΩ		30	60	
Output Short-Circuit Current	$I_{OUT(SC)}$	V_{DD} = +5.0V	Sourcing		11		mA
			Sinking		30		
Output Leakage Current in Shutdown	$I_{OUT(SH)}$	Device in Shutdown Mode ($\overline{SHDN\_}$ = V_{SS}), V_{SS} ≤ V_{OUT} ≤ V_{DD} (Note 2)			±0.01	±0.5	µA
$\overline{SHDN\_}$ Logic Low	V_{IL}	(Note 2)				0.3 x V_{DD}	V
$\overline{SHDN\_}$ Logic High	V_{IH}	(Note 2)		0.7 x V_{DD}			V
$\overline{SHDN\_}$ Input Current	I_L/I_H	V_{SS} ≤ $\overline{SHDN\_}$ ≤ V_{DD} (Note 2)			0.5	50	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L connected from OUT to V_{DD} / 2, $\overline{SHDN\_}$ = V_{DD} (MAX4245/MAX4247 only), **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBW			1.0		MHz
Phase Margin	ϕ_M			70		degrees
Gain Margin	G_M			20		dB
Slew Rate	SR			0.4		V/µs
Input Voltage-Noise Density	e_n	f = 10kHz		52		nV/√Hz
Input Current-Noise Density	i_n	f = 10kHz		0.1		pA/√Hz
Capacitive-Load Stability	C_{LOAD}	A_V = 1 (Note 3)			470	pF
Shutdown Delay Time	$t_{(SH)}$	(Note 2)		3		µs
Enable Delay Time	$t_{(EN)}$	(Note 2)		4		µs
Power-On Time	t_{ON}			4		µs
Input Capacitance	C_{IN}			2.5		pF
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = 2Vp-p, A_V = +1, V_{DD} = +5.0V, Load = 100kΩ to V_{DD}/2		0.01		%
Settling Time to 0.01%	t_S	V_{OUT} = 4V step, V_{DD} = +5.0V, A_V = +1		10		µs

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L connected from OUT to V_{DD} / 2, $\overline{SHDN\_}$ = V_{DD} (MAX4245/MAX4247 only), **T_A = -40°C to +125°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Inferred from PSRR test	2.5		5.5	V
Supply Current (Per Amplifier)	I_{DD}	V_{DD} = +2.7V			800	µA
Supply Current in Shutdown	$I_{\overline{SHDN\_}}$	$\overline{SHDN\_}$ = V_{SS} (Note 2)			1	µA
Input Offset Voltage	V_{OS}	V_{SS} ≤ V_{CM} ≤ V_{DD} (Note 4)			±3.0	mV
Input Offset Voltage Drift	TCV_{OS}	V_{SS} ≤ V_{CM} ≤ V_{DD} (Note 4)		±2		µV/°C
Input Bias Current	I_B	V_{SS} ≤ V_{CM} ≤ V_{DD} (Note 4)			±100	nA
Input Offset Current	I_{OS}	V_{SS} ≤ V_{CM} ≤ V_{DD} (Note 4)			±10	nA
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test (Note 4)	V_{SS}		V_{DD}	V
Common-Mode Rejection Ratio	CMRR	V_{SS} ≤ V_{CM} ≤ V_{DD} (Note 4)	60			dB
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{DD} ≤ 5.5V	70			dB
Large-Signal Voltage Gain	A_V	V_{SS} + 0.2V ≤ V_{OUT} ≤ V_{DD} - 0.2V, R_L = 2kΩ	85			dB
Output Voltage Swing High	V_{OH}	Specified as V_{DD} - V_{OUT}, R_L = 2kΩ			90	mV
Output Voltage Swing Low	V_{OL}	Specified as V_{OUT} - V_{SS}, R_L = 2kΩ			90	mV
Output Leakage Current in Shutdown	$I_{OUT(SH)}$	Device in Shutdown Mode ($\overline{SHDN\_}$ = V_{SS}), V_{SS} ≤ V_{OUT} ≤ V_{DD} (Note 3)			±1.0	µA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V, V_{SS} = 0V, V_{CM} = 0V, V_{OUT} = V_{DD} / 2, R_L connected from OUT to V_{DD} / 2, $\overline{SHDN\_}$ = V_{DD} (MAX4245/MAX4247 only), **T_A = -40°C to +125°C**, unless otherwise noted.) (Note 1)

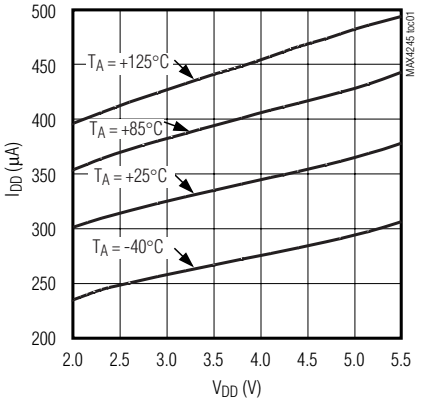
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN\_}$ Logic Low	V_{IL}	(Note 2)			0.3 × V_{DD}	V
$\overline{SHDN\_}$ Logic High	V_{IH}	(Note 2)	0.7 × V_{DD}			V
$\overline{SHDN\_}$ Input Current	I_L/I_H	V_{SS} ≤ $\overline{SHDN\_}$ ≤ V_{DD} (Notes 2, 3)			100	nA

Note 1: Specifications are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Shutdown mode is only available in MAX4245 and MAX4247.
Note 3: Guaranteed by design, not production tested.
Note 4: For -40°C to +85°C, Input Common-Mode Range is V_{SS} - 0.1V ≤ V_{CM} ≤ V_{DD} + 0.1V.

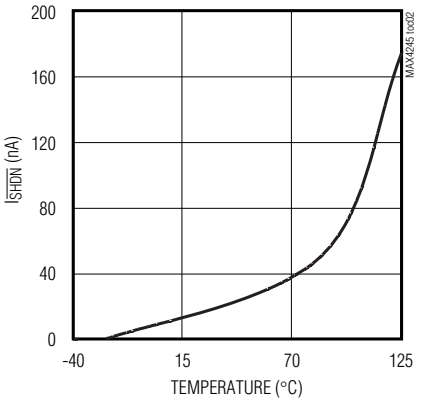
Typical Operating Characteristics

(V_{DD} = 2.7V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD} / 2, no load, T_A = +25°C, unless otherwise noted.)

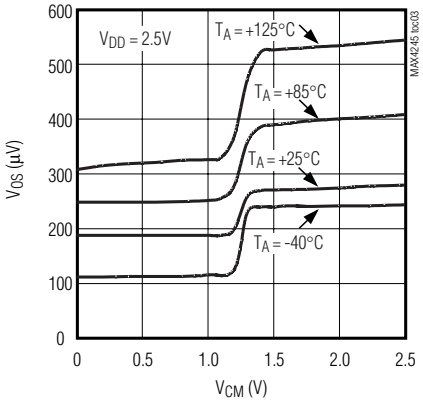
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



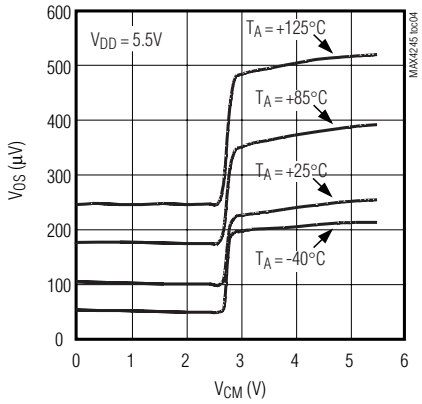
MAX4245/MAX4247 SHUTDOWN SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



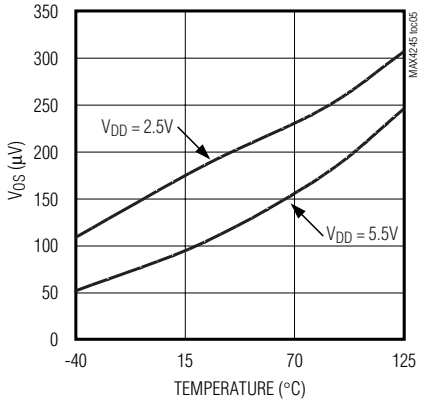
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



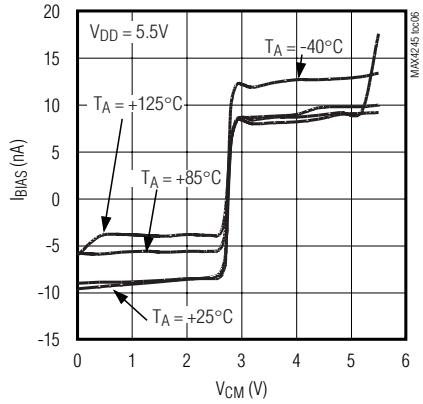
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



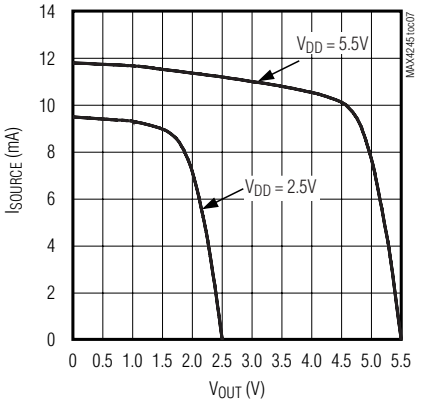
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



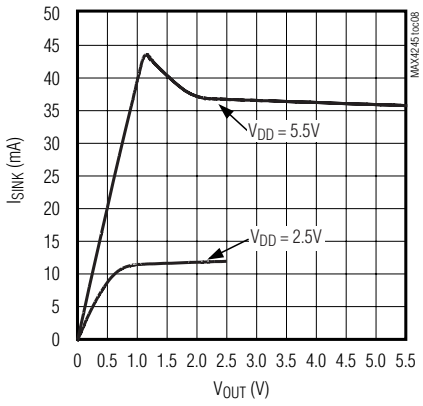
Typical Operating Characteristics (continued)

(V_{DD} = 2.7V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD} / 2, no load, T_A = +25°C, unless otherwise noted.)

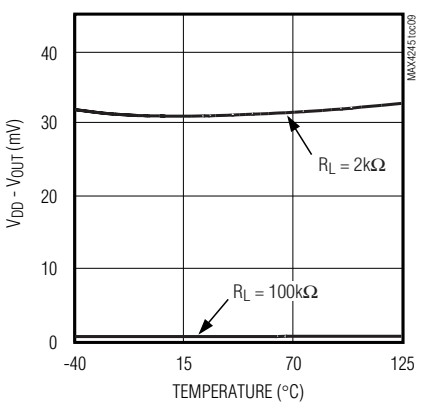
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



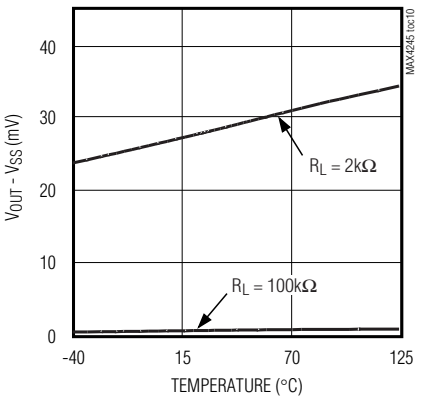
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



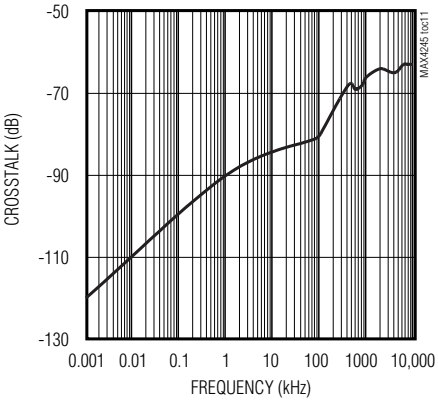
OUTPUT SWING HIGH vs. TEMPERATURE



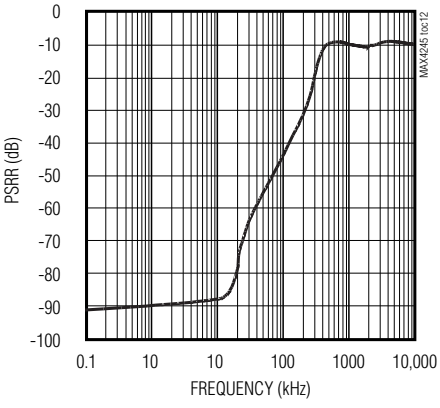
OUTPUT SWING LOW vs. TEMPERATURE



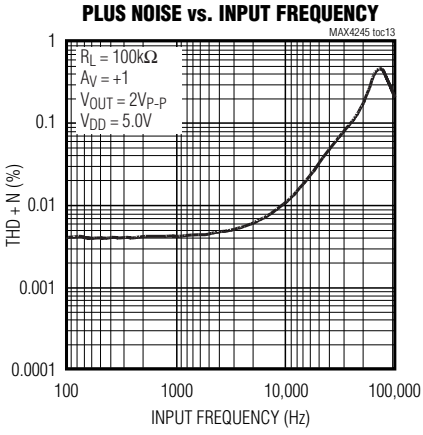
CROSSTALK vs. FREQUENCY



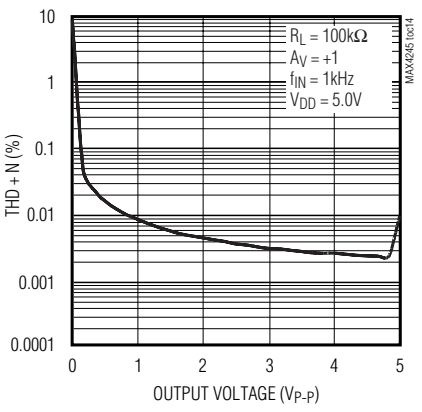
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



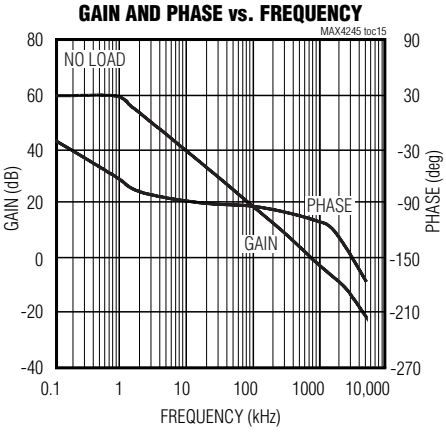
TOTAL HARMONIC DISTORTION PLUS NOISE vs. INPUT FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. AMPLITUDE



GAIN AND PHASE vs. FREQUENCY

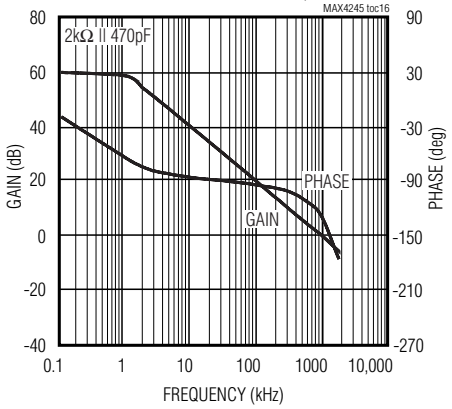


Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

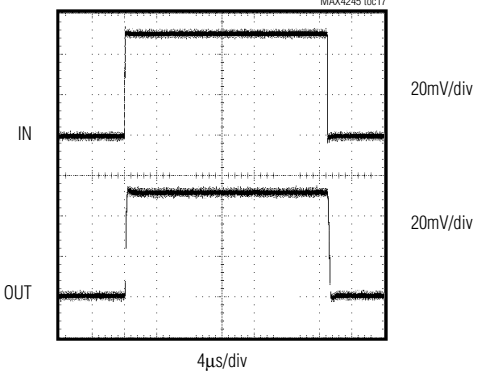
Typical Operating Characteristics (continued)

(V_{DD} = 2.7V, V_{SS} = V_{CM} = 0V, V_{OUT} = V_{DD} / 2, no load, T_A = +25°C, unless otherwise noted.)

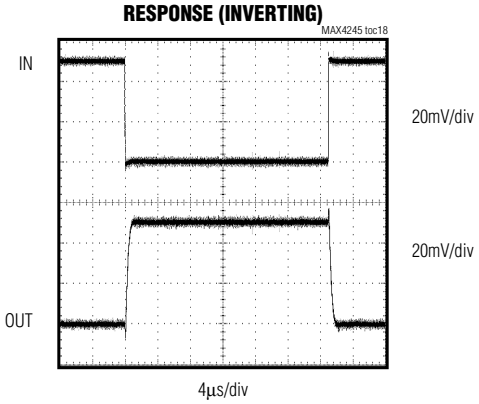
GAIN AND PHASE vs. FREQUENCY



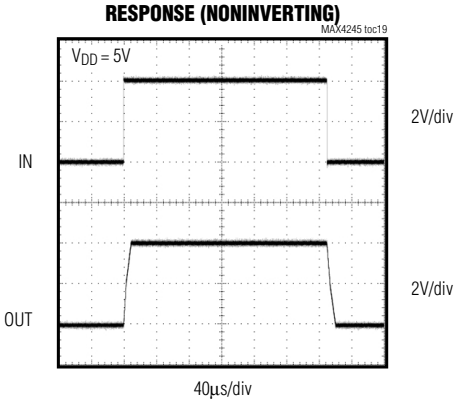
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



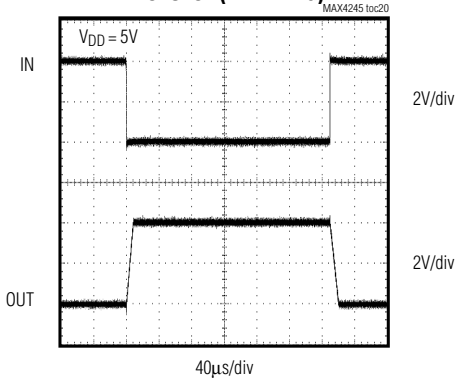
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

PIN			NAME	FUNCTION
MAX4245	MAX4246	MAX4247		
1	—	—	IN+	Noninverting Input
2	4	4	V_{SS}	Ground or Negative Supply
3	—	—	IN-	Inverting Input
4	—	—	OUT	Amplifier Output
5	—	—	$\overline{SHDN}$	Shutdown
6	8	10	V_{DD}	Positive Supply
—	1	1	OUTA	Amplifier Output Channel A
—	2	2	INA-	Inverting Input Channel A
—	3	3	INA+	Noninverting Input Channel A
—	5	7	INB+	Noninverting Input Channel B
—	6	8	INB-	Inverting Input Channel B
—	7	9	OUTB	Amplifier Output Channel B
—	—	5	$\overline{SHDNA}$	Shutdown Channel A
—	—	6	$\overline{SHDNB}$	Shutdown Channel B

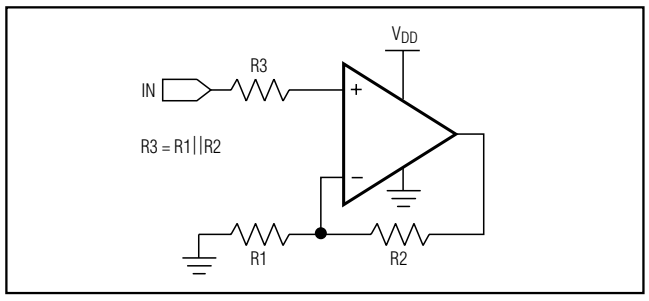


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

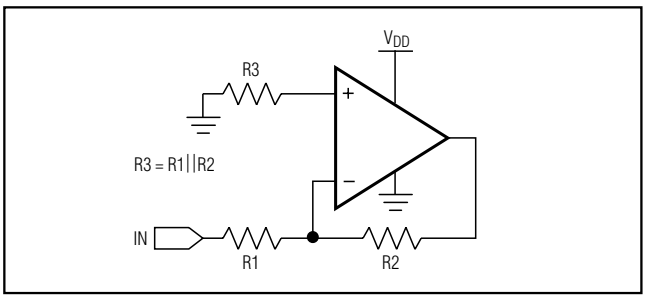


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

Detailed Description

Rail-to-Rail Input Stage

The MAX4245/MAX4246/MAX4247 have rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of composite NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between V_{DD} and V_{SS}. The input offset voltage is typically ±400µV. Low-operating supply voltage, low supply current and rail-to-rail outputs make this family of operational amplifiers an excellent choice for precision or general-purpose, low-voltage, battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedance (Figures 1a and 1b).

The combination of high-source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that can produce an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

The MAX4245/MAX4246/MAX4247 family's inputs are protected from large differential input voltages by internal 5.3kΩ series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential-input voltages much less than 2.1V (triple-diode drop),

Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

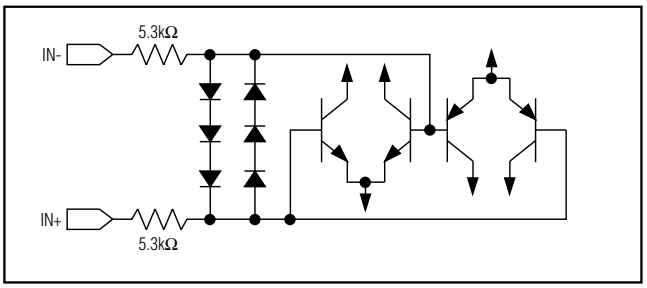


Figure 2. Input Protection Circuit

input resistance is typically 4MΩ. For differential voltages greater than 2.1V, input resistance is around 10.6kΩ, and the input bias current can be approximated by the following equation:

$$I_B = (V_{DIFF} - 2.1V) / 10.6k\Omega$$

In the region where the differential input voltage approaches 2.1V, the input resistance decreases exponentially from 4MΩ to 10.6kΩ as the diodes begin to conduct. It follows that the bias current increases with the same curve.

In unity-gain configuration, high slew-rate input signals may capacitively couple to the output through the triple-diode stacks.

Rail-to-Rail Output Stage

The MAX4245/MAX4246/MAX4247 can drive a 2kΩ load and still typically swing within 35mV of the supply rails. Figure 3 shows the output voltage swing of the MAX4245 configured with A_V = -1V/V.

Applications Information

Power-Supply Considerations

The MAX4245/MAX4246/MAX4247 operate from a single +2.5V to +5.5V supply (or dual ±1.25V to ±2.75V supplies) and consume only 320µA of supply current per amplifier. A 90dB power-supply rejection ratio allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

Power-Up

The MAX4245/MAX4246/MAX4247 output typically settles within 4µs after power-up. Figure 4 shows the output voltage on power-up and power-down.

Shutdown Mode

The MAX4245/MAX4247 feature a low-power shutdown mode. When $\overline{SHDN\_}$ is pulled low, the supply current drops to 50nA per amplifier, the amplifier is disabled, and the output enters a high-impedance state. Pulling $\overline{SHDN\_}$ high enables the amplifier. Figure 5 shows the MAX4245/MAX4247's shutdown waveform.

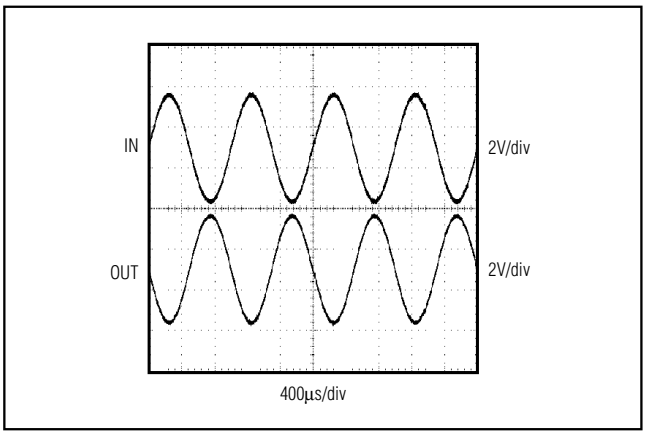


Figure 3. Rail-to-Rail Input/Output Voltage Range

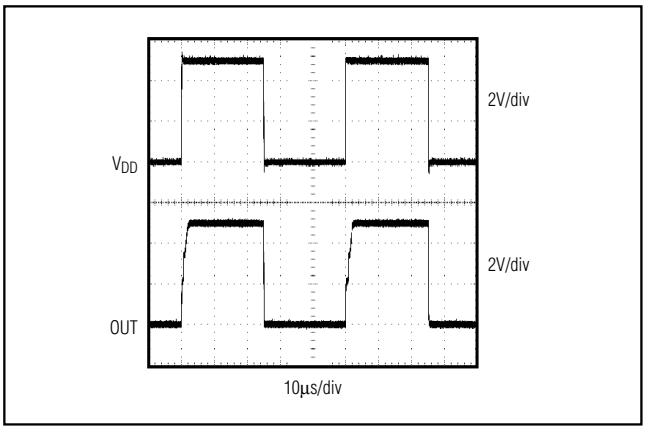


Figure 4. Power-Up/Power-Down Waveform

Due to the output leakage currents of three-state devices and the small internal pullup current for $\overline{SHDN\_}$, do not let the $\overline{SHDN\_}$ float. Floating $\overline{SHDN\_}$ may result in indeterminate logic levels, and could adversely affect op amp operation. The logic threshold for $\overline{SHDN\_}$ is referred to V_{SS}. When using dual supplies, pull $\overline{SHDN\_}$ to V_{SS}, not GND, to shut down the op amp.

Driving Capacitive Loads

The MAX4245/MAX4246/MAX4247 are unity-gain stable for loads up to 470pF. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load

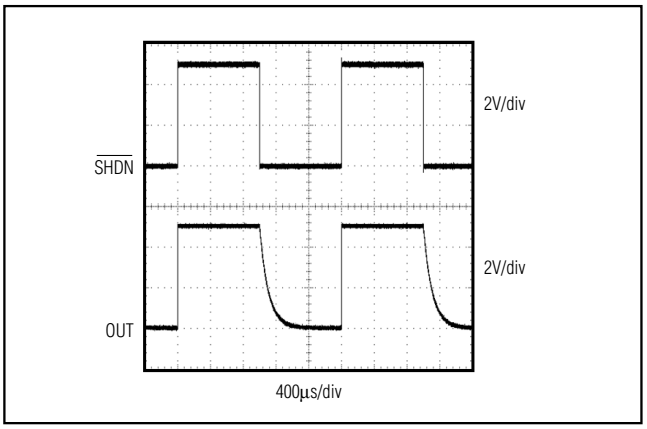


Figure 5. Shutdown Waveform

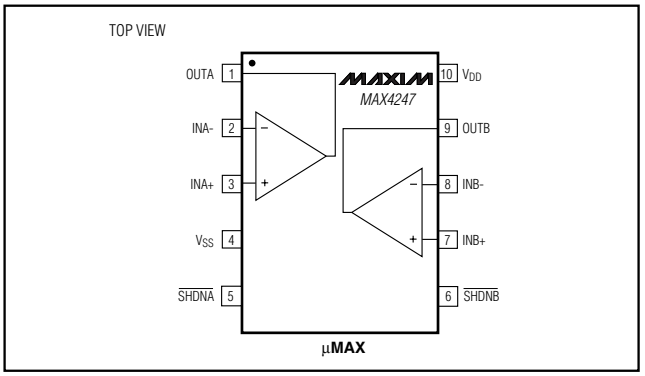
(Figures 6a, 6b, 6c). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

Power-Supply Bypassing and Layout

The MAX4245/MAX4246/MAX4247 family operates from either a single +2.5V to +5.5V supply or dual ±1.25V to ±2.75V supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to V_{SS} (in this case GND). For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components when possible.

Pin Configurations (continued)



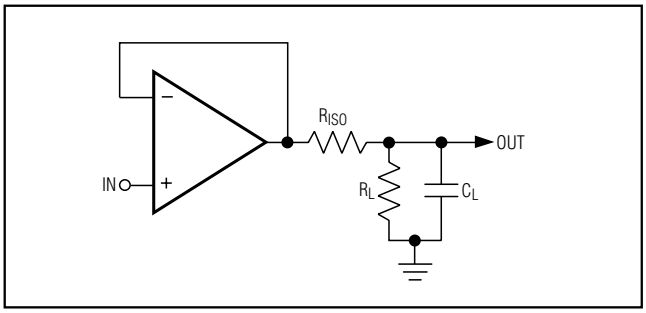


Figure 6a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

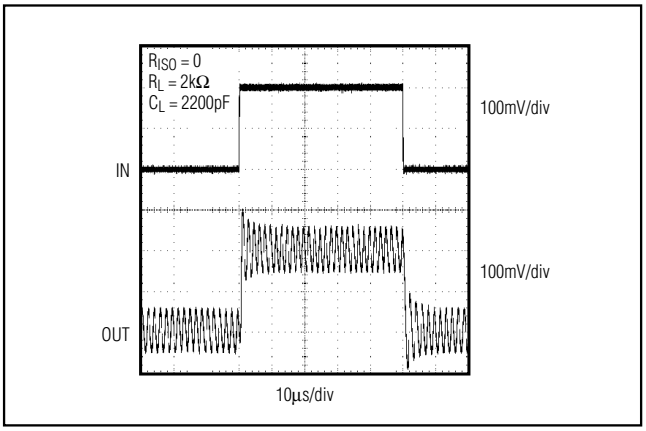


Figure 6b. Pulse Response Without Isolating Resistor

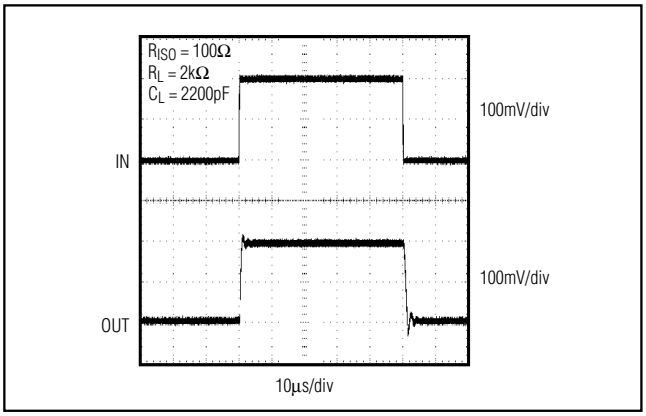


Figure 6c. Pulse Response With Isolating Resistor

Chip Information

MAX4245 TRANSISTOR COUNT: 207

MAX4246/MAX4247 TRANSISTOR COUNT: 414

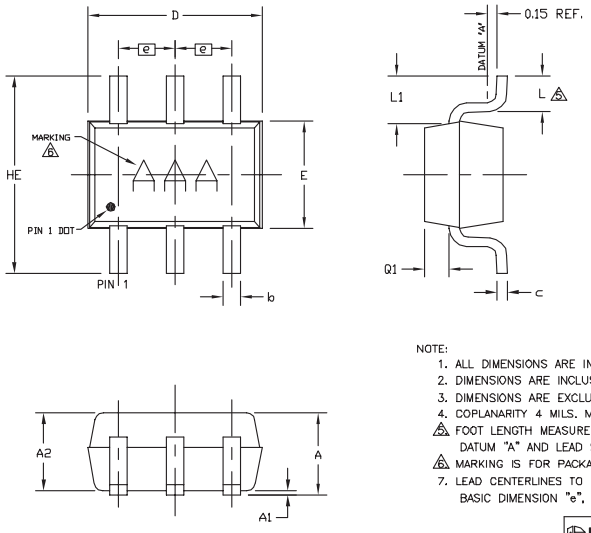
PROCESS: BiCMOS

Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SC70, 6L.EPS



COMMON DIMENSIONS		
SYMBOL	MIN	MAX
A	0.80	1.10
A1	0.00	0.10
A2	0.80	1.00
b	0.15	0.30
c	0.10	0.18
D	1.80	2.20
e	0.65 BSC.	
E	1.15	1.35
HE	1.80	2.40
L	0.10	0.41
L1	0.425 TYP.	
Q1	0.10	0.40

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

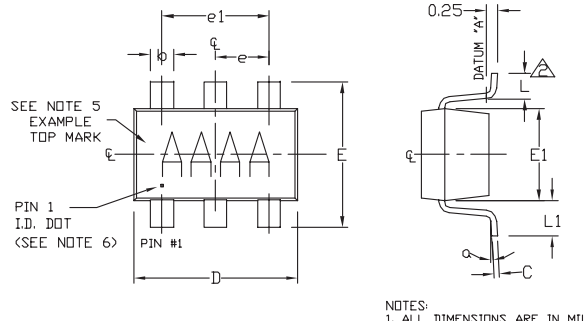
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L SC70

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0077	C	1/1

-DRAWING NOT TO SCALE-

6LSOT.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF.	
e1	1.90 BSC.	
e	0.95 BSC.	
α	0°	10°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

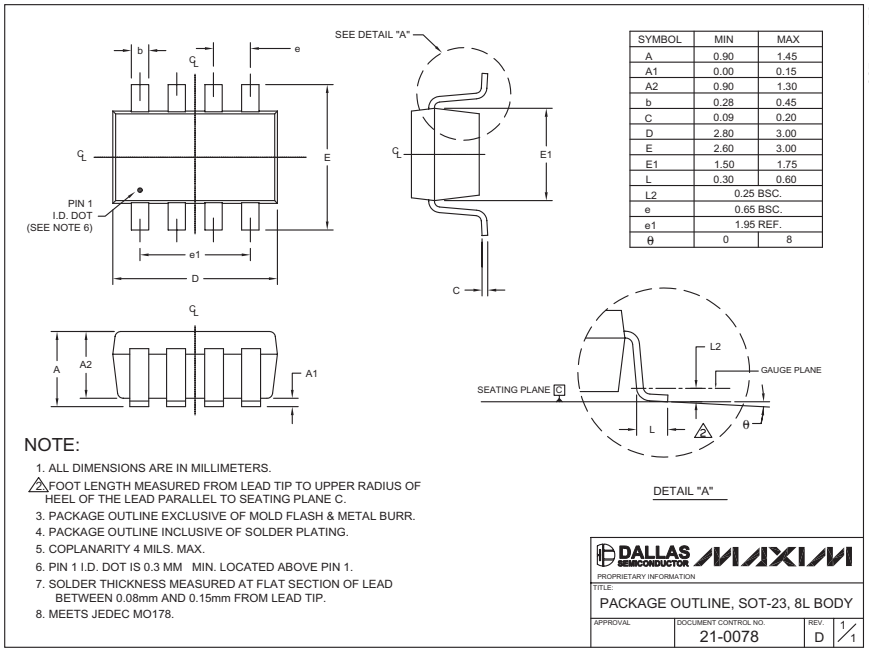
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	G	1/1

-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0	8

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

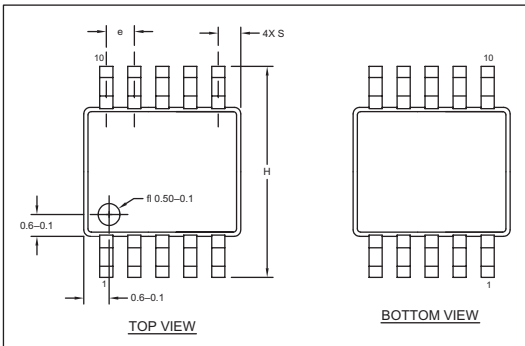
DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

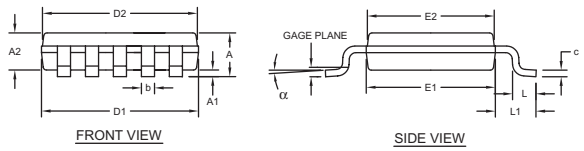
TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	D	1/1

10LUMAX.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

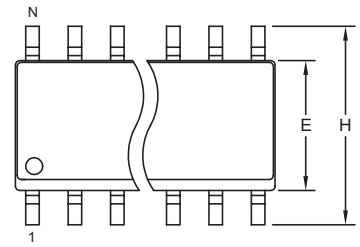
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

Ultra-Small, Rail-to-Rail I/O with Disable, Single-/Dual-Supply, Low-Power Op Amps

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SOICN .EPS

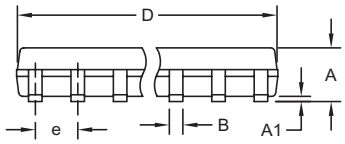


TOP VIEW

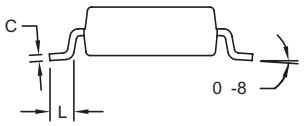
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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