

FQB25N33 330V N-Channel MOSFET

Features

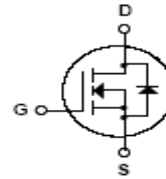
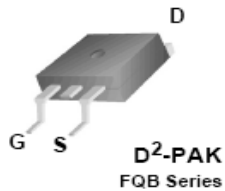
- 25A, 330V, $R_{DS(on)} = 0.23\Omega @ V_{GS} = 10V$
- Low gate charge (typical 58nC)
- Low Crss (typical 40pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Qualified to AEC Q101
- RoHS Compliant



General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimized on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



Absolute Maximum Ratings

Symbol	Parameter	FQB25N33	Units
V_{DSS}	Drain-Source Voltage	330	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	25	A
	- Continuous ($T_C = 100^\circ\text{C}$)	16.0	A
I_{DM}	Drain Current - Pulsed (Note 1)	100	A
V_{GSS}	Gate -Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (Note 2)	370	mJ
I_{AR}	Avalanche Current (Note 1)	25	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	37	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.1	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	250	W
	- Derate above 25°C	2.0	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8 from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQB25N33	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient *	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB25N33	FQB25N33	D2-PAK	330mm	24mm	800

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	330	--	--	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	--	0.34	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 330\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 264\text{V}, T_C = 125^\circ\text{C}$	--	--	1 10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{V}, V_{DS} = 0\text{V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 12.5\text{A}$	--	0.18	0.23	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{V}, I_D = 12.5\text{A}$, (Note 4)	--	1	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	--	1510	2010	pF
C_{oss}	Output Capacitance		--	290	385	pF
C_{rss}	Reverse Transfer Capacitance		--	40	60	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 165\text{V}, I_D = 25\text{A}$ $R_{GS} = 25\Omega$ (Note 4, 5)	--	20	35	ns
t_r	Turn-On Rise Time		--	100	160	ns
$t_{d(off)}$	Turn-Off Delay Time		--	90	145	ns
t_f	Turn-Off Fall Time		--	70	110	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{DS} = 297\text{V}, I_D = 25\text{A}$, $V_{GS} = 15\text{V}$, (Note 4, 5)	--	58	75	nC
Q_{gs}	Gate to Source Gate Charge		--	11.2	--	nC
Q_{gd}	Gate to Drain Charge		--	21	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	25	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	100	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0, I_S = 25\text{A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0, I_S = 25\text{A}$,	--	275	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	--	3.6	--	μC

Notes:

- 1: Repetitive Rating : Pulse width Limited by maximum junction temperature
- 2: $L = 1.79\text{mH}, I_{AS} = 25\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 25\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq B_{VDSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
- 5: Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

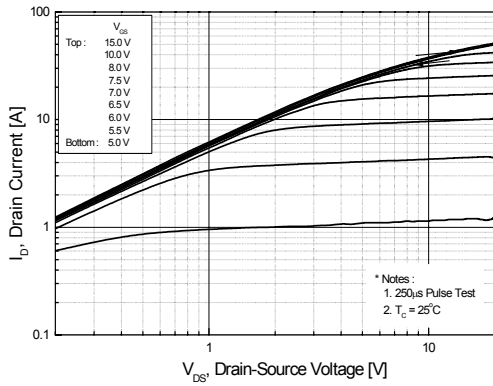


Figure 2. Transfer Characteristics

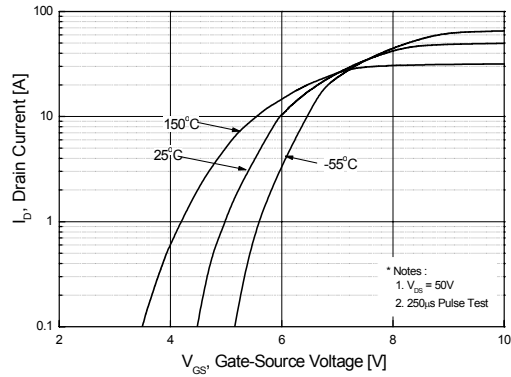


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

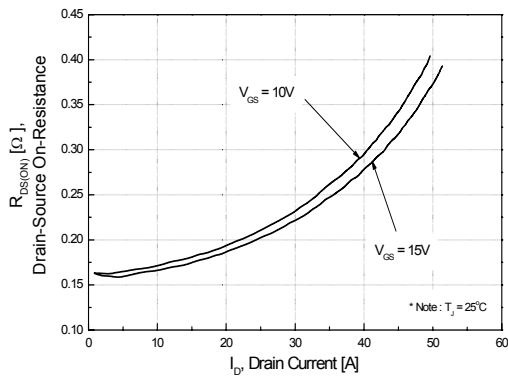


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

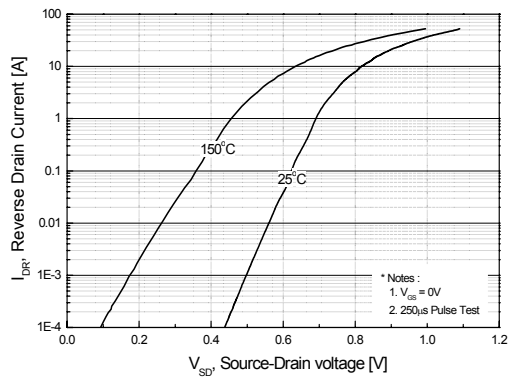


Figure 5. Capacitance Characteristics

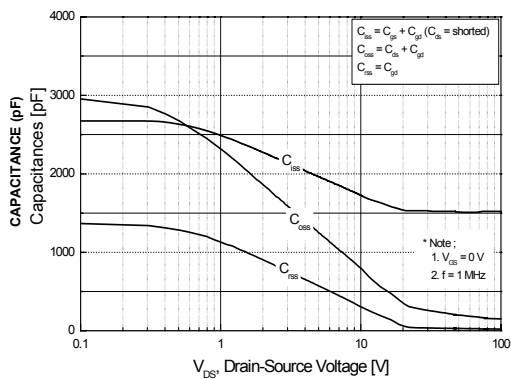
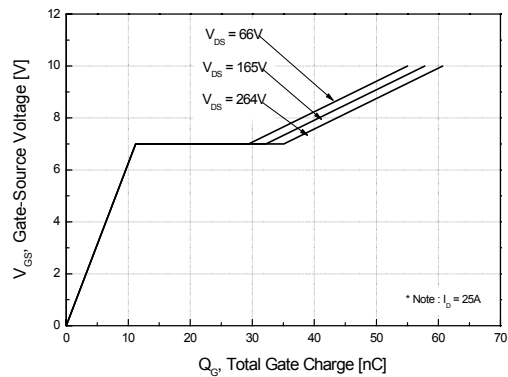


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

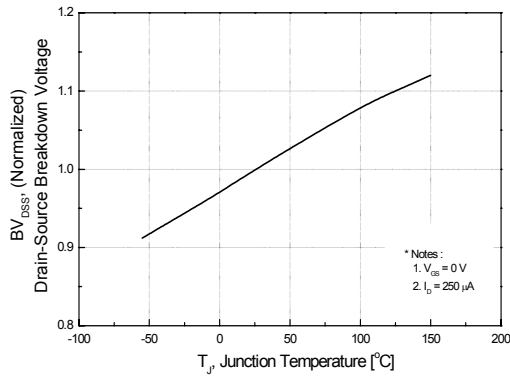


Figure 8. On-Resistance Variation vs. Temperature

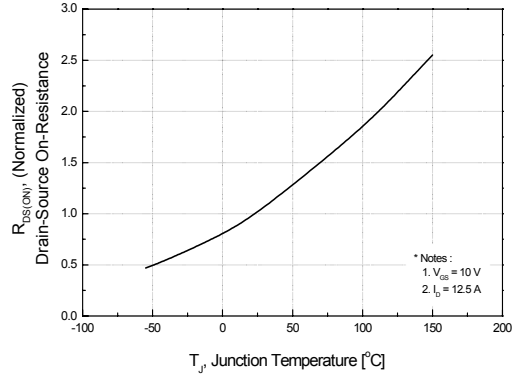


Figure 9. Maximum Safe Operating Area

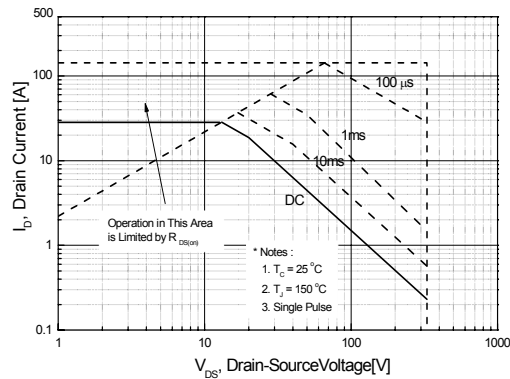


Figure 10. Maximum Drain Current vs. Case Temperature

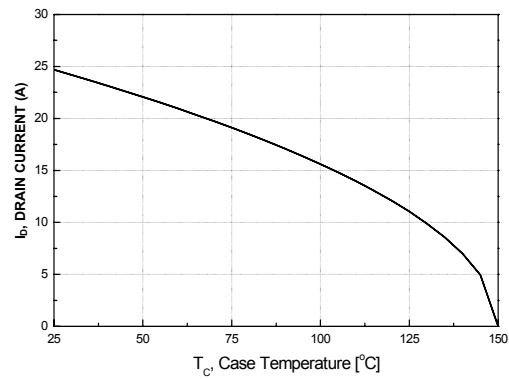
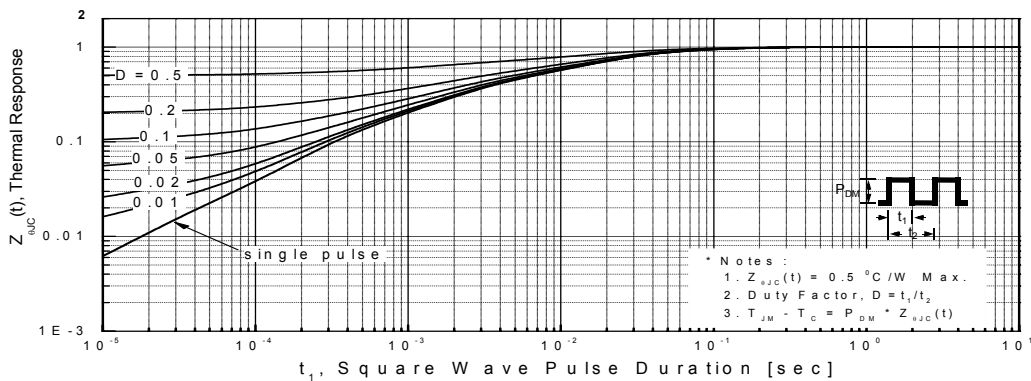
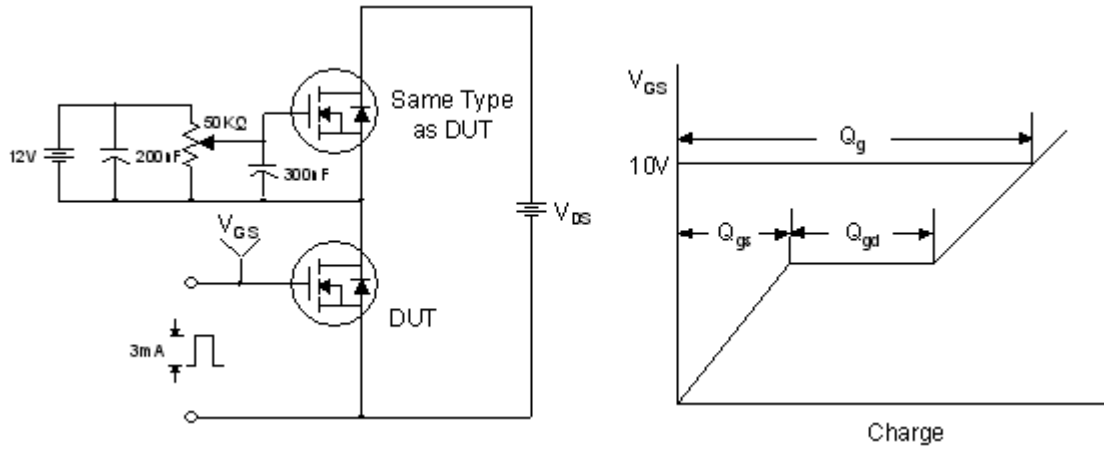


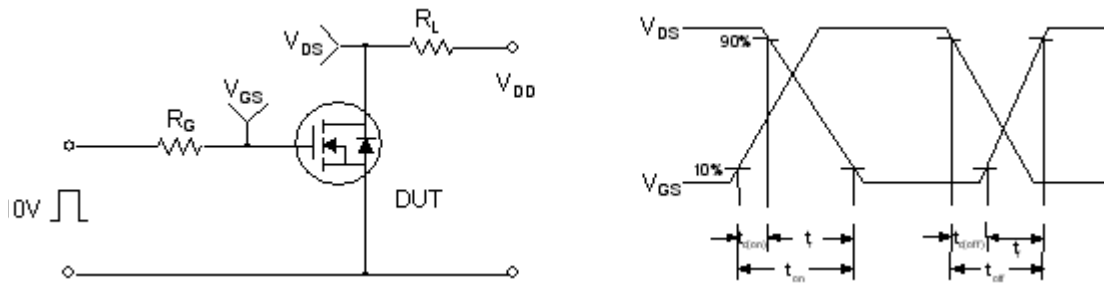
Figure 11. Transient Thermal Response Curve



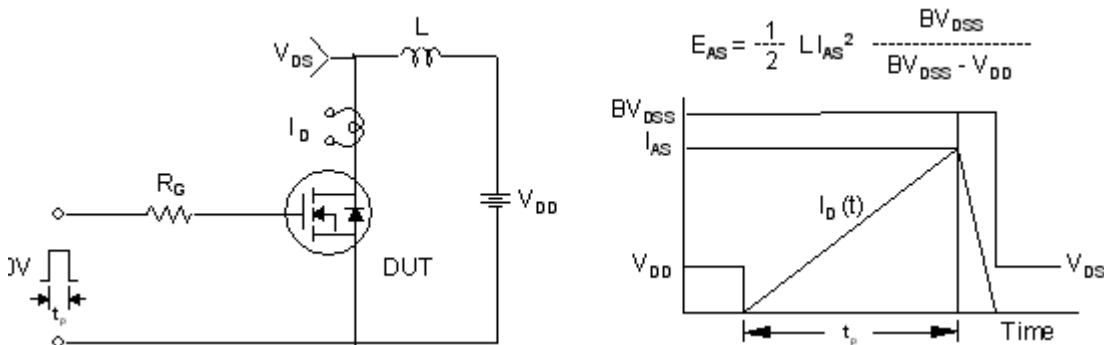
Gate Charge Test Circuit & Waveform



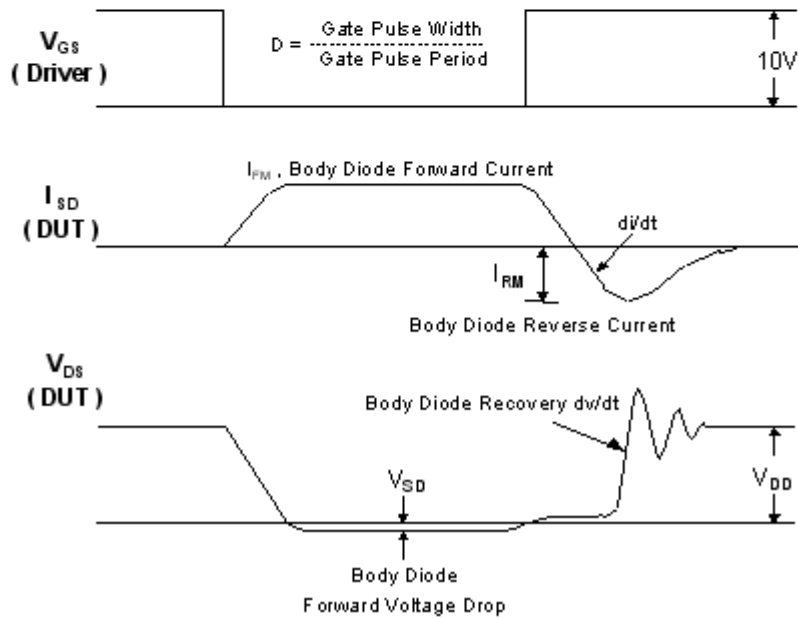
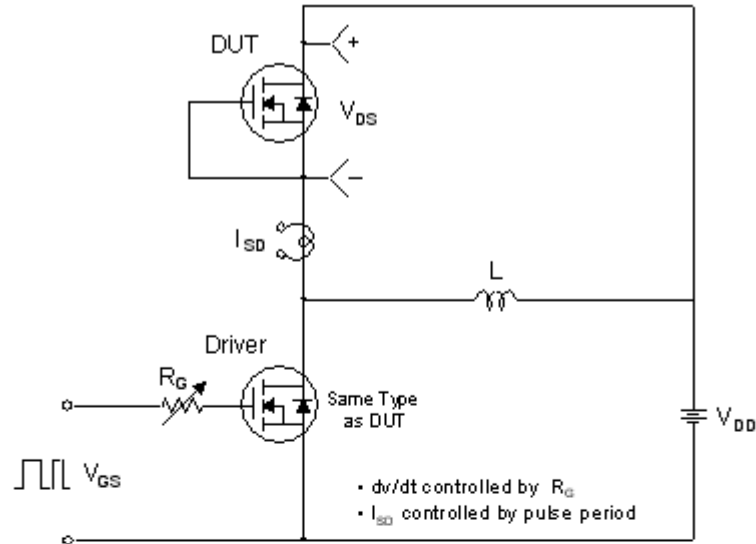
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

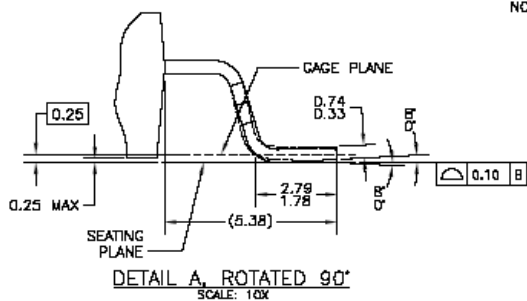
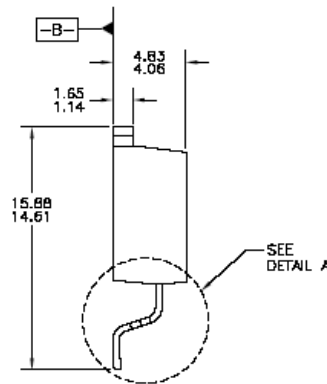
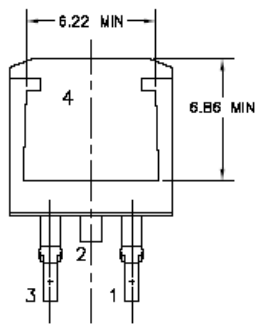
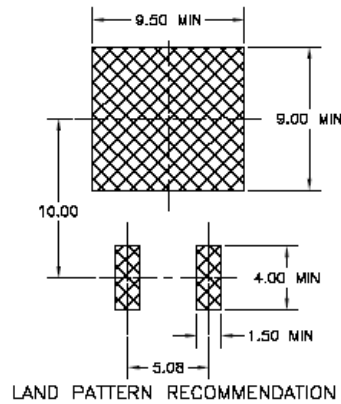
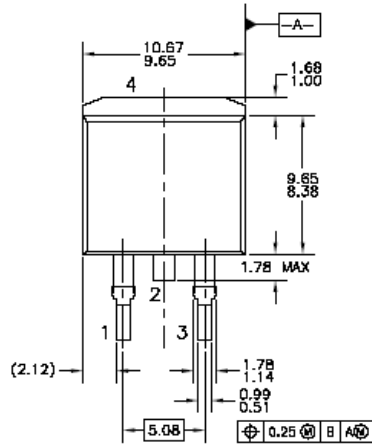


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

D2-PAK



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.
 - C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M - 1982.
 - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
 - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

T02B3AD2REVD

Dimensions in Millimeters

Ultrafast Recovery Power Rectifier

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