



# MX23L51220

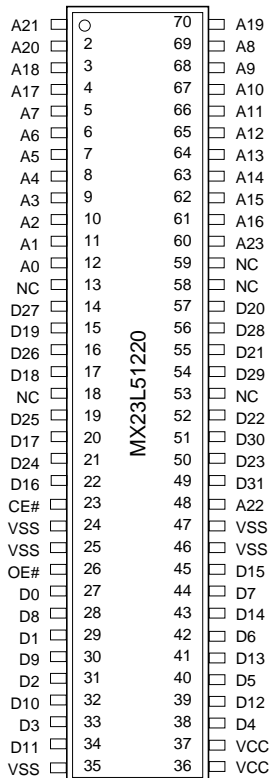
## 512M-BIT (16M x 32) MASKROM WITH PAGE MODE (SSOP ONLY) (for socket solution only)

### FEATURES

- Bit organization
  - 16M x 32 (double word mode) only
- Fast access time
  - Random access: 90ns (max.)
  - Page access: 30ns (max.)
- Page size
  - 8 double words per page
- Current
  - Operating: 80mA (max.) @ 5MHz
  - Standby: 30uA (max.)
- Supply voltage : 3.3V ±10%
- Package
  - 70 pin SSOP
- Temperature
  - 0~70° C

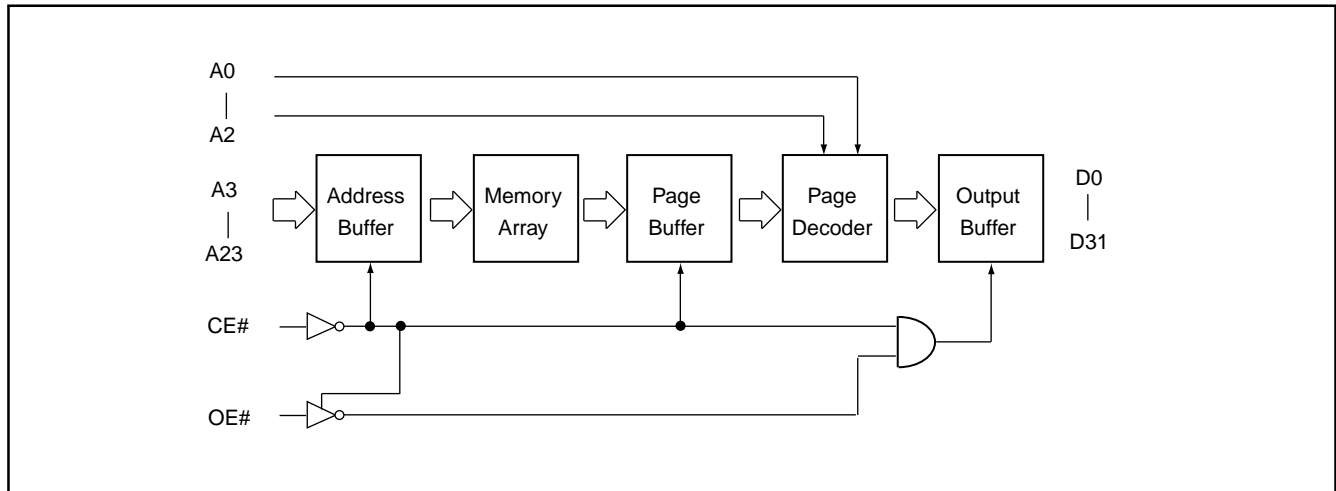
### PIN CONFIGURATION

#### 70 PIN SSOP



### PIN DESCRIPTION

Symbol	Pin Function
A0~A23	Address Inputs
D0~D31	Data Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection (pin 18 and 53 must be floating, not connected to VCC or GND)

**BLOCK DIAGRAM**

**MODE SELECTION**

CE#	OE#	D0~D31	Mode	Power
H	X	High Z	-	Stand-by
L	H	High Z	-	Active
L	L	D0~D31	Double Word	Active

**ORDER INFORMATION**

Part No.	Access Time	Package
MX23L51220MC-90	90ns	70 pin SSOP
MX23L51220MC-10	100ns	70 pin SSOP

**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	V <sub>IN</sub>	-0.3V to 3.9V
Ambient Operating Temperature	T <sub>opr</sub>	0°C to 70°C
Storage Temperature	T <sub>stg</sub>	-65°C to 125°C

**DC CHARACTERISTICS** ( $T_a = 0^\circ\text{C} \sim 70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

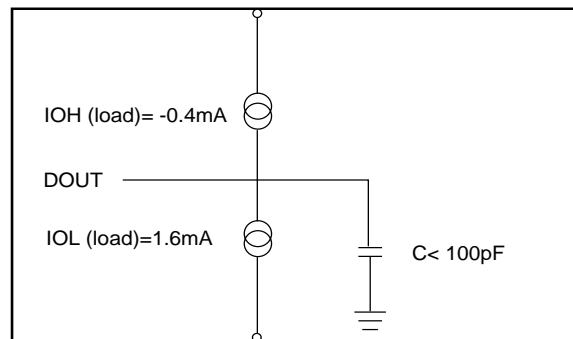
Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2xVCC	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC	-	80mA	f=5MHz, all output open CE#=VIL(Chip Enable) OE#=VIH(Output Disabled)
Standby Current (TTL)	ISTB1	-	1mA	CE# = VIH
Standby Current (CMOS)	ISTB2	-	30uA	CE# > VCC-0.2V
Input Capacitance	CIN	-	20pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

**AC CHARACTERISTICS** ( $T_a = 0^\circ\text{C} \sim 70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Item	Symbol	23L51220-90		23L51220-10	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	90ns	-	100ns	-
Address Access Time	tAA	-	90ns	-	100ns
Chip Enable Access Time	tCE	-	90ns	-	100ns
Page Mode Access Time	tPA	-	30ns	-	30ns
Output Enable Time	tOE	-	30ns	-	30ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

**AC Test Conditions**

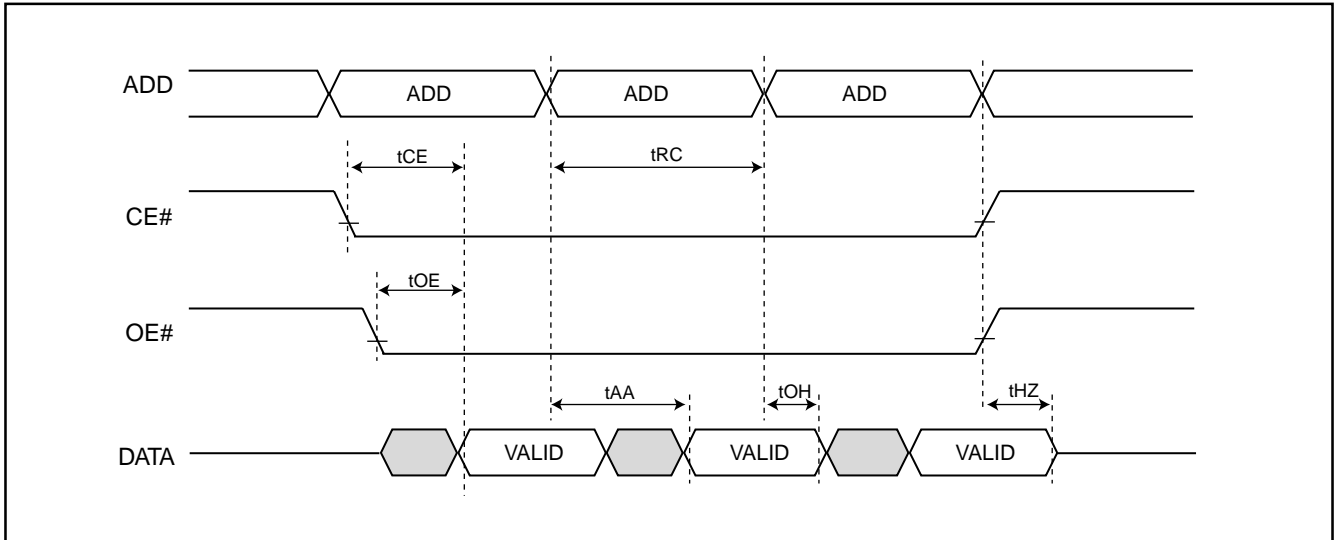
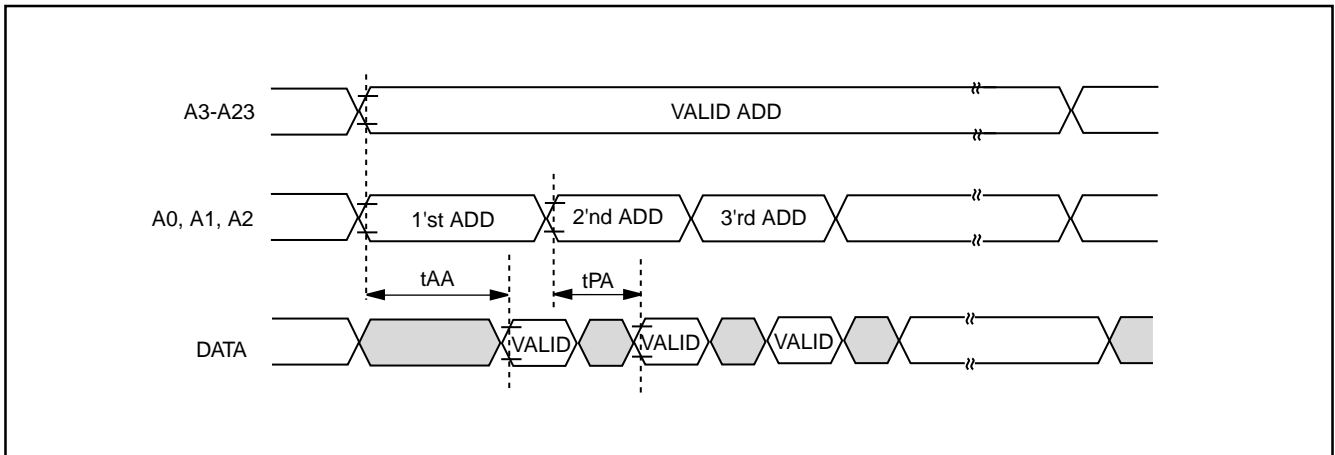
Input Pulse Levels	0.4V~ 2.8V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure

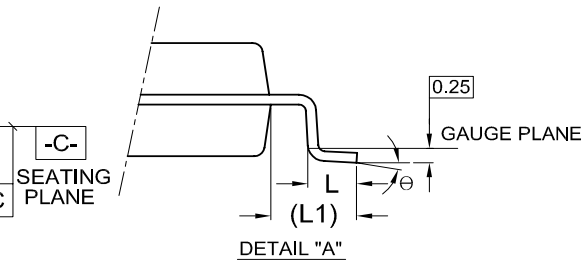
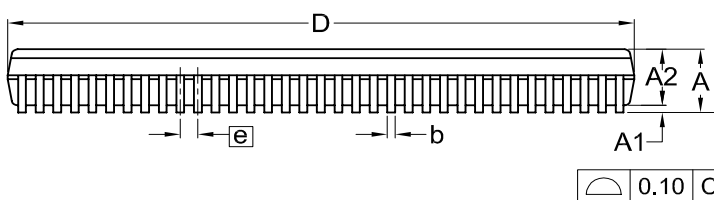
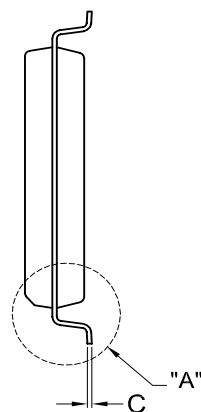
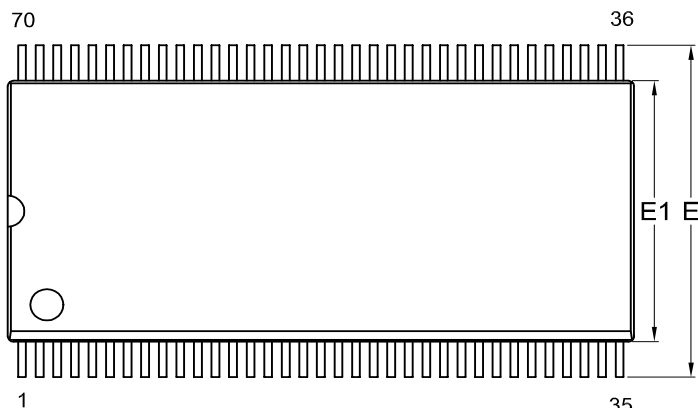


Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

**TIMING DIAGRAM**
**RANDOM READ**

**PAGE READ**


**PACKAGE INFORMATION**
**Title: Package Outline for SSOP 70L (500MIL)**


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
UNIT													
mm	Min.	---	0.10	2.56	0.30	0.17	28.37	15.73	12.47		0.61	1.51	0
	Nom.	---	0.15	2.69	0.35	0.20	28.50	16.03	12.60	0.80	0.81	1.71	5
	Max.	3.05	0.23	2.82	0.40	0.25	28.63	16.33	12.73		1.01	1.91	10
Inch	Min.	---	0.004	0.101	0.012	0.007	1.117	0.619	0.491		0.024	0.060	0
	Nom.	---	0.006	0.106	0.014	0.008	1.122	0.631	0.496	0.031	0.032	0.068	5
	Max.	0.120	0.009	0.111	0.016	0.010	1.127	0.643	0.501		0.040	0.075	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1503	5				11-26-'03

**REVISION HISTORY**

<b>Revision No.</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
1.1	Modify supply voltage-- 3.3V $\pm$ 5% for temporary period, 3.3V $\pm$ 10% after new product available	P1,2,3	JUL/11/2003
1.2	1. Removed "Preliminary" on page 1 2. Operating : 60mA(max.) --> 80mA(max.) 3. Input pulse levels : 0.4V~2.4V --> 0.4V~2.8V	P1 P1,3 P3	FEB/25/2004
1.3	1. Added "for socket solution only" on page 1	P1	SEP/02/2004



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