

SANYO Semiconductors **DATA SHEET**

An ON Semiconductor Company

LC79430KNE — Dot-Matrix LCD Drivers

Overview

The LC79430KNE is a large-scale dot matrix LCD common driver LSI. The LC79430KNE contains an 80-bit bidirectional shift register and is equipped with a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the IC's number of bits. The LC79430KNE can be used in conjunction with segment driver LC79401KNE (QIP100E) to drive a wide-screen LCD panel.

Features

- On-chip LCD drive circuit (80 bits)
- Display duty selection ranging from 1/64 to 1/256
- On-chip input/output pins support a further increases in bit number
- Supports externally supplied bias voltage
- On-chip 80-bit bidirectional shift register (supports 40-bit × 2 division)
- Supports single mode (80-bit shift register) and dual mode (40-bit × 2 shift register) applications

All four of the shift direction selection listed above all supported

• Operating power supply voltage/operating temperature include

V_{DD} (Logic section) : 2.7 to 5.5V/-20 to +85°C V_{DD}-V_{EE} (LCD section) : 12 to 32V/-20 to +85°C

- CMOS process
- 100-pin flat plastic package (QIP100E)
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Specifications

Absolute Maximum Ratings at $Ta = 25\pm2^{\circ}C$, $V_{SS} = 0V$

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (Logic)	V _{DD} max		-0.3 to +7.0	V
Maximum supply voltage (LCD)	V _{DD} -V _{EE} max	*1	0 to 35	V
Maximum input voltage	V _I max		-0.3 to V _{DD} +0.3	V
Storage temperature	Tstg		-40 to +125	°C

Note *1 The following relations between elements should be maintained: V_{DD}≥V1>V2>V5>V_{EE}, V_{DD}-V2≤7V, V5-V_{EE}≤7V

Allowable Operating Ranges at $Ta = -20 \text{ to } +85^{\circ}\text{C}, V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (Logic)	V_{DD}		2.7		5.5	V
Supply voltage (LCD)	V _{DD} -V _{EE}	*2, 3	12		32	V
Input high level voltage	V _{IH}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF	0.8V _{DD}			V
Input low level voltage	V _{IL}	DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF			0.2V _{DD}	٧
CP Shift clock	fCP	СР			1	MHz
CP pulse width	tWC	СР	63			ns
Setup time	[†] SETUP	$\begin{array}{c} \text{DIO1} \rightarrow \text{CP, DIO80} \rightarrow \text{CP,} \\ \text{DMIN} \rightarrow \text{CP} \end{array}$	100			ns
Hold time	tHOLD	$\begin{array}{c} \text{DIO1} \rightarrow \text{CP, DIO80} \rightarrow \text{CP,} \\ \text{DMIN} \rightarrow \text{CP} \end{array}$	100			ns
CP rise time	t _R	СР			50	ns
CP fall time	t _F	СР			50	ns

Note *2 The following relations between elements should be maintained: V_{DD}≥V1>V2>V5>V_{EE}, V_{DD}-V2≤7V, V5-V_{EF}≤7V

Electrical Characteristics at $Ta = 25\pm2^{\circ}C$, $V_{DD} = 2.7$ to 5.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Input high level current	lін	V _{IN} =V _{DD} , V _{DD} =5.5V, DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF			1	μА
Input low level current	l _{IL}	V _{IN} =V _{SS} , V _{DD} =5.5V, DIO1, DIO80, CP, M, DMIN, MODE, RS/LS, DISPOFF				μА
Output high level voltage	V _{OH}	I _{OH} =-0.4mA, DIO1, DIO80	V _{DD} -0.4			V
Output low level voltage	V _{OL}	I _{OL} =0.4mA, DIO1, DIO80			0.4	V
Driver on resistance	R _{ON} (1)	V _{DD} -V _{EE} =30V, V _{DE} -V _O =0.5V V _{DD} =4.5V, O1 to O80 *4			1.0	kΩ
	R _{ON} (2)	V _{DD} -V _{EE} =20V, V _{DE} -V _O =0.5V V _{DD} =4.5V, O1 to O80 *4			1.0	kΩ
Consumable current drain (1)	ISS	V_{DD} - V_{EE} =30V, CP=14kHz no-load, V_{DD} =5.5V ; V_{SS}			100	μА
Consumable current drain (2)	IEE	V_{DD} - V_{EE} =30V, CP=14kHz no-load, V_{DD} =5.5V ; V_{EE}			100	μА
Input capacitance	CI	f=1MHz ; CP		8		pF

Note *4 $V_{DE} = V1$ or V2 or V5 or V_{EE} , $V1 = V_{DD}$, V2 = 16/17 (V_{DD} - V_{EE}), V5 = 1/17 (V_{DD} - V_{EE})

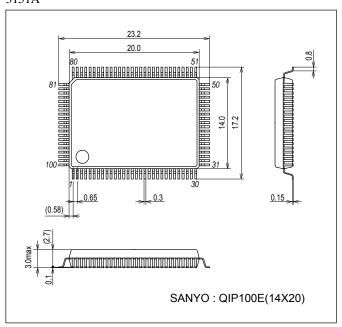
Switching Characteristics at $Ta = 25\pm2^{\circ}C$, $V_{SS} = 0V$, $V_{DD} = 2.7$ to 5.5V

Parameter	Symbol	Conditions	min	typ	max	unit
Output delay time	^t PLH	CL=15pF ; CP \rightarrow DIO1, CP \rightarrow DIO80			250	ns
	tPHL	CL=15pF ; CP \rightarrow DIO1, CP \rightarrow DIO80			250	ns

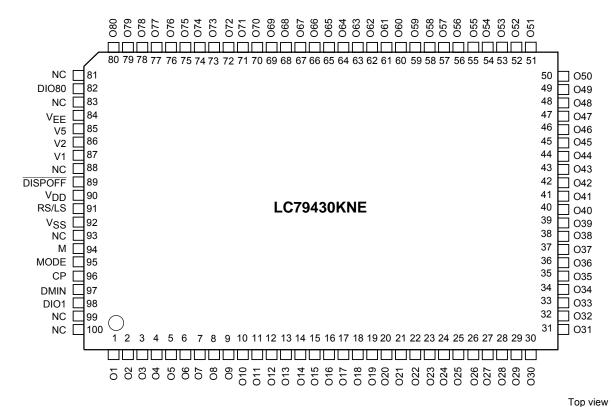
^{*3} When the power supply is turned on, power to the LCD driver is turned on after or simultaneously with the turning on of the logic section's power supply. When the power supply is turned off, the logic power supply is turned off after or at the same time the LCD driver power supply is turned off.

Package Dimensions

unit:mm (typ) 3151A

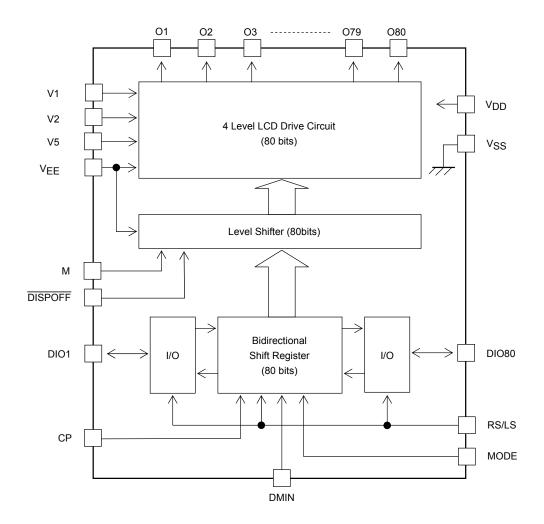


Pin Assignment



rop view

Equivalent Circuit Block Diagram

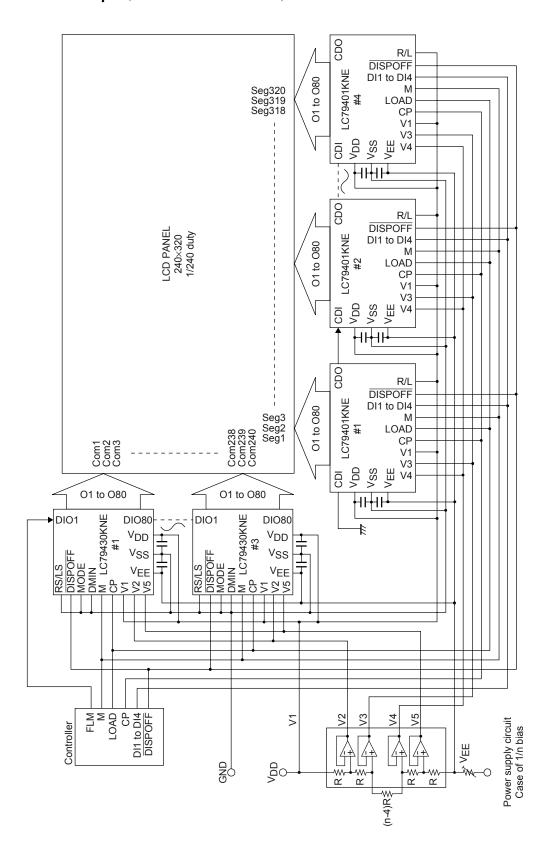


LC79430KNE

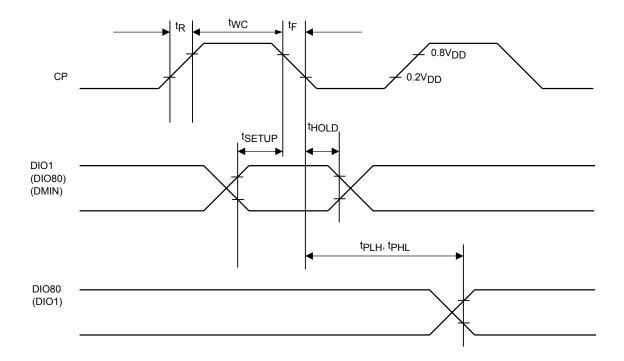
Pin Function

Pin No	Pin Fun	CHOH										
Supply Vos V	Pin No	Symbol	I/O	Function								
Supply Vondame Vonda	90	V _{DD}										
Second	92	V _{SS}	Supply									
Supply V1 YEE Selected level V2 V3 V3 V4 V4 V5 V4 V5 V5 V5 V5	84	V _{EE}		ADD-AEE - F	ADD-AFF : FOD alive circuit bowel subbis							
S	87	V1		LCD drive lev	el power supply							
96	86	V2	Supply	V1, V _{EE} : Se	lected level							
MODE	85	V5		V2, V5 : Uns	elected level							
98	96	CP	1	Bidirectional	shift register shift clo	ck (falling ed	ge trigger)					
98									1			
Second Figure Second				MODE	RS/LS	Data Trar	nsfer Direction	DIO1	DIO80	DMIN		
91				L	L (Shift right)	01	→ O80	IN	OUT	*		
Section Sect	82	DIO80	I/O	(Single)	H (Shift left)	08	0 → O1	OUT	IN	*		
95 97 MODE DMIN I I (Dual) H (Shift left) O30 → 041 OUT IN IN IN O1 O20 → 01 OUT IN IN IN O1 O20 → 01 OUT IN IN IN O1 O20 → 01 OUT O1 OUT	01	RS/I S			I (Chift right)	01	→ O40	INI	OUT	INI		
H (Shift left)				Н	L (Shiit right)	O41	→ O80	IIV	001	114		
NC No No No No No No No	97	DMIN	1	(Dual)	H (Shift left)) → O41	OUT	INI	INI		
94 M							001	IIN	114			
NC September				* Don't care (May be set to either "H" or "L")								
1	94		I	LCD drive ou	LCD drive output alternation signal							
The output levels are determined by the combination of the output the data, The M signal, and the DISPOFF pin as shown in the table. M	89	DISPOFF	- I	O1 to O80 ou	tput controlling input	pins.						
NC The M signal, and the DISPOFF pin as shown in the table. M	1	01			•							
M Data DISPOFF Output								out the data,				
L L H V2									Outrut	\neg		
O L H H V5 H H H V1 * Don't care (May be set to either "H" or "L") 80										_		
H				-						_		
H			0							_		
* * * L V1 * Don't care (May be set to either "H" or "L") 80 81 83 88 93 99 NC - Must be left open.						Н Н				_		
* Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L") * Don't care (May be set to either "H" or "L")										_		
80 O80 81 83 88 93 99				L								
83 88 93 99 NC - Must be left open.	80	O80		Don't care (may be set to either	H OF L)						
88 NC - Must be left open. 99	81											
93 99 NC - Must be left open.	83											
93 99	88) NO		Much had to								
	93	NC NC	-	iviust be left o	ppen.							
100	99											
	100											

Application Example (LC79401KNE/LC79430KNE)



Switching Characteristics Diagram



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