Panasonic
NMOS MEMORY
Panasonic

DIGITAL INTEGRATED CIRCUITS DATA

MN4164-15
MN4164P-15
MN4164-20
MN4164P-20
MN4164-25
MN4164P-25

MN4164 NMOS 65,536 x 1 BIT DYNAMIC RAM

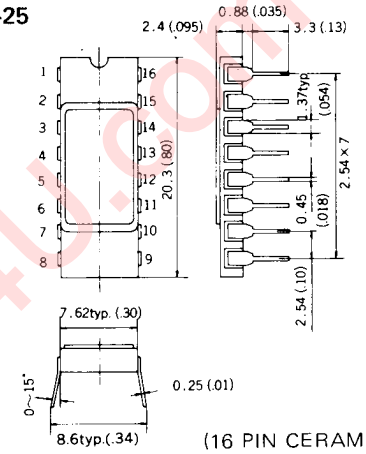
Description

System oriented features include operation from a single +5V ±10% tolerance power supply, direct TTL interfacing capability, on-chip addresses and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system.

The RAM module also incorporates several flexible operating modes: "Read", "Write", "Read-Modify-Write" cycles, "Page-Mode" operation and "$\overline{RAS}$-Only" refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (for operating in page mode).

MN4164-15
MN4164-20
MN4164-25

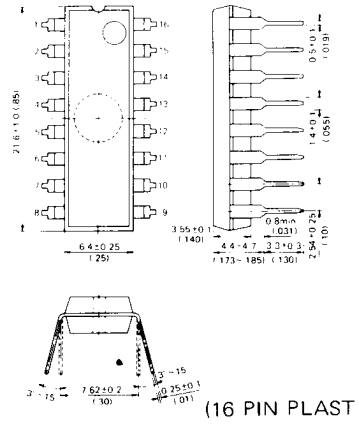
Unit: mm (inch)



(16 PIN CERAMIC DIL)

MN4164P-15
MN4164P-20
MN4164P-25

Unit: mm (inch)



(16 PIN PLASTIC DIL)

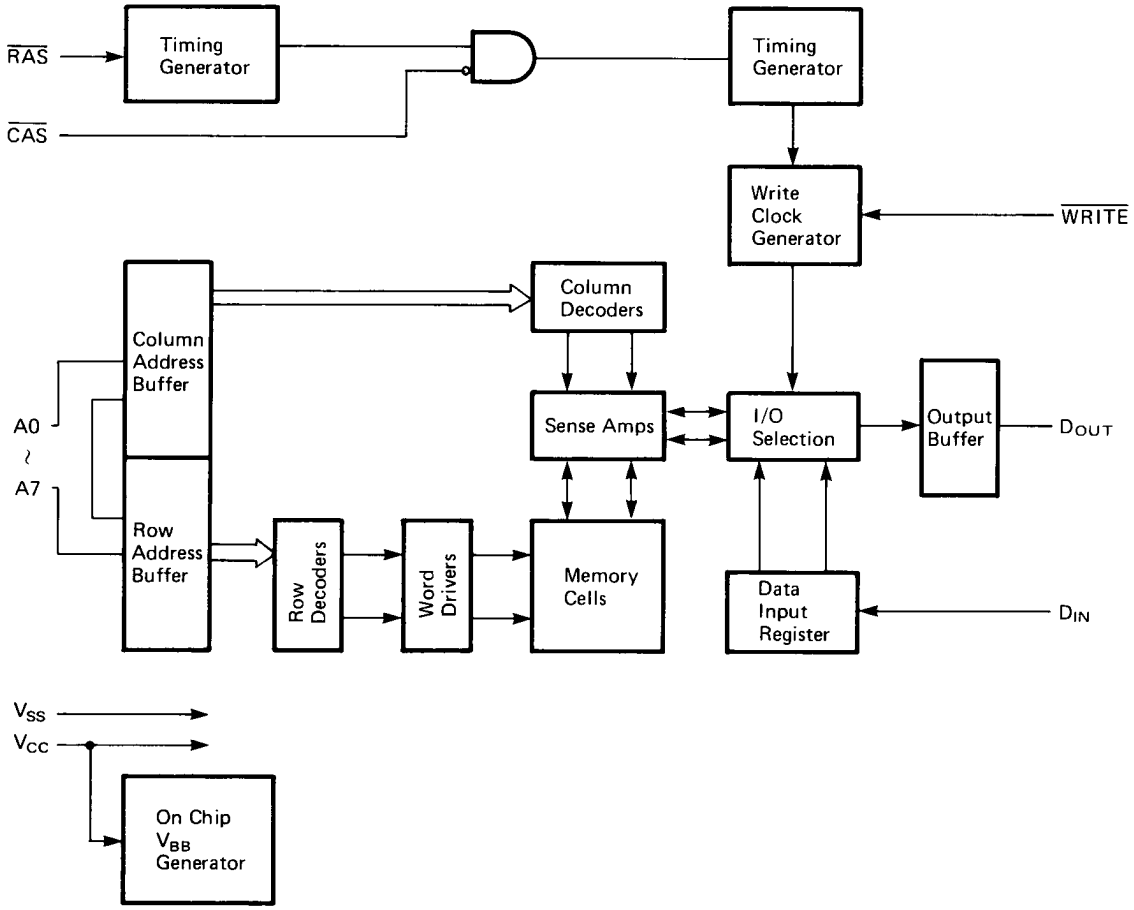
Features

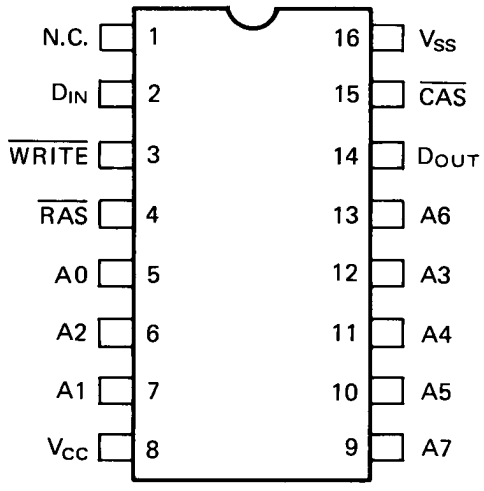
- 65,536 x 1 RAM, 16-pin package
- Row access time:
  - 150 ns Max. (MN4164-15/MN4164P-15)
  - 200 ns Max. (MN4164-20/MN4164P-20)
  - 250 ns Max. (MN4164-25/MN4164P-25)
- Cycle time:
  - 270 ns Max. (MN4164-15/MN4164P-15)
  - 330 ns Max. (MN4164-20/MN4164P-20)
  - 410 ns Max. (MN4164-25/MN4164P-25)
- Low power dissipation:
  - 275 mW Max. (active)
  - 27.5 mW Max. (standby)
- Single 5V supply, ±10% tolerance
- 128 refresh cycles/2ms

69 ORIG

003693 PAN

3693 SKI





Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any Pin relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to + 7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1.0 to + 7.0	V
Operating Temperature	T_{OP}	0 to + 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Current	I_{OS}	50	mA

Note:

Exceeding Absolute Maximum Ratings may cause permanent device damage. Functional operating of the device is not implied outside the operating conditions. Exposure to absolute maximum ratings for extended periods of time may impact device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.2	–	V_{CC}+1.0V	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	–	0.8	V	

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	–	–	10	pF
Output Capacitance	C_{OUT}	–	–	12	pF

DC Characteristics (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Current Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	I_{CC1}	–	–	50	mA	1)
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	–	5	mA	
Referesh Current Average supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min)	I_{CC3}	–	–	40	mA	1)
Page Mode Current Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	I_{CC4}	–	–	40	mA	1)
Input Leakage Current Input leakage current, any input (0V ≦ V_{IN} ≦ 5.5V, all other pins not under test = 0V)	I_{LI}	–10	0.1	10	μA	
Output Leakage Current (Data out is disabled, 0V ≦ V_{OUT} ≦ 5.5V)	I_{LO}	–10	0.1	10	μA	
Output Level Output low voltage (I_{OL} = 4.2 mA)	V_{OL}	–	–	0.4	V	
Output Level Output high voltage (I_{OH} = –5 mA)	V_{OH}	2.4	–	–	V	

Note:

1) I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate and output loading. Specifications are for maximum cycle rate and no load. Supply current may be scaled according to the following equation:

$$I(t_{RC}) = \frac{t_{RC}\ \text{min} \times I\ (t_{RC}\ \text{min}) + (t_{RC} - t_{RC}\ \text{min}) \times I_{CC2}}{t_{RC}}$$

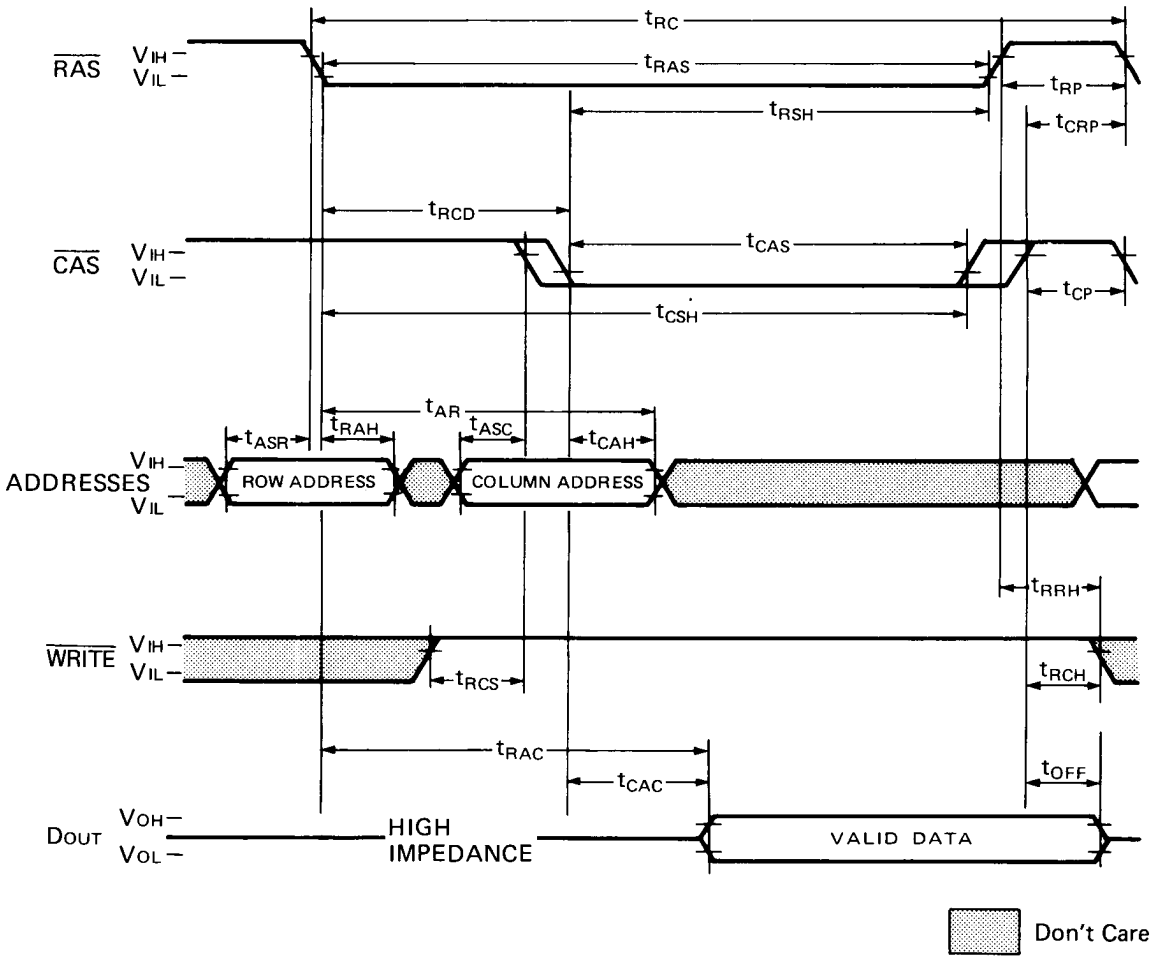
AC Characteristics[1, 2] (Recommended operating conditions unless otherwise noted.)

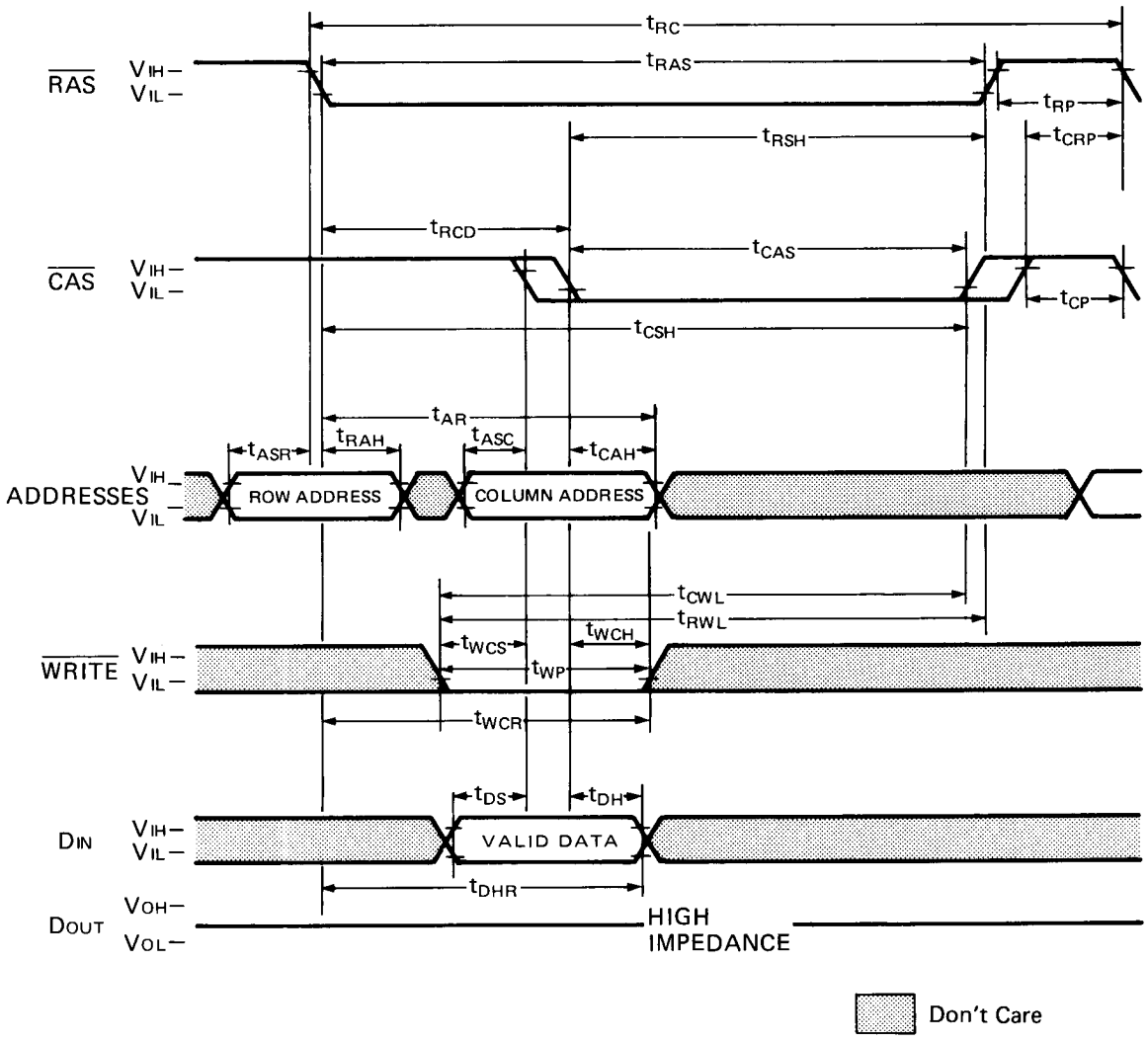
Parameter	Symbol	Unit	MN4164-15 MN4164P-15		MN4164-20 MN4164P-20		MN4164-25 MN4164P-25		Note
			Min	Max	Min	Max	Min	Max	
Refresh period	t_{REF}	ms	–	2	–	2	–	2	
Random read or write cycle time	t_{RC}	ns	270	–	330	–	410	–	
Read-write cycle time	t_{RWC}	ns	310	–	375	–	515	–	
Page mode cycle time	t_{PC}	ns	170	–	225	–	275	–	
Acces time from $\overline{RAS}$	t_{RAC}	ns	–	150	–	200	–	250	4), 6), 8)
Acces time from $\overline{CAS}$	t_{CAC}	ns	–	100	–	135	–	165	5), 6), 8)
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	0	60	7)
Transition time	t_T	ns	3	50	3	50	3	50	3)
$\overline{RAS}$ precharge time	t_{RP}	ns	100	–	120	–	150	–	
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	250	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100	–	135	–	165	–	
$\overline{CAS}$ precharge time	t_{CP}	ns	50	–	80	–	100	–	
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	165	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150	–	200	–	250	–	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	65	40	85	8)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	–20	–	–20	–	–20	–	
Row Address set-up time	t_{ASR}	ns	0	–	0	–	0	–	
Row Address hold time	t_{RAH}	ns	20	–	20	–	35	–	
Column Address set-up time	t_{ASC}	ns	–5	–	–5	–	–5	–	
Column Address hold time	t_{CAH}	ns	45	–	55	–	75	–	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95	–	120	–	160	–	
Read command set-up time	t_{RCS}	ns	0	–	0	–	0	–	
Read command hold time	t_{RCH}	ns	0	–	0	–	0	–	
Write command set-up time	t_{WCS}	ns	–20	–	–20	–	–20	–	10)
Write command hold time	t_{WCH}	ns	45	–	55	–	75	–	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95	–	120	–	160	–	
Write command pulse width	t_{WP}	ns	45	–	55	–	75	–	
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	60	–	80	–	100	–	
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	60	–	80	–	100	–	
Data-in set-up time	t_{DS}	ns	0	–	0	–	0	–	9)
Data-in hold time	t_{DH}	ns	45	–	55	–	75	–	9)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95	–	120	–	160	–	
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	ns	80	–	95	–	125	–	10)
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	ns	130	–	160	–	200	–	10)
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20	–	25	–	35	–	

Note:

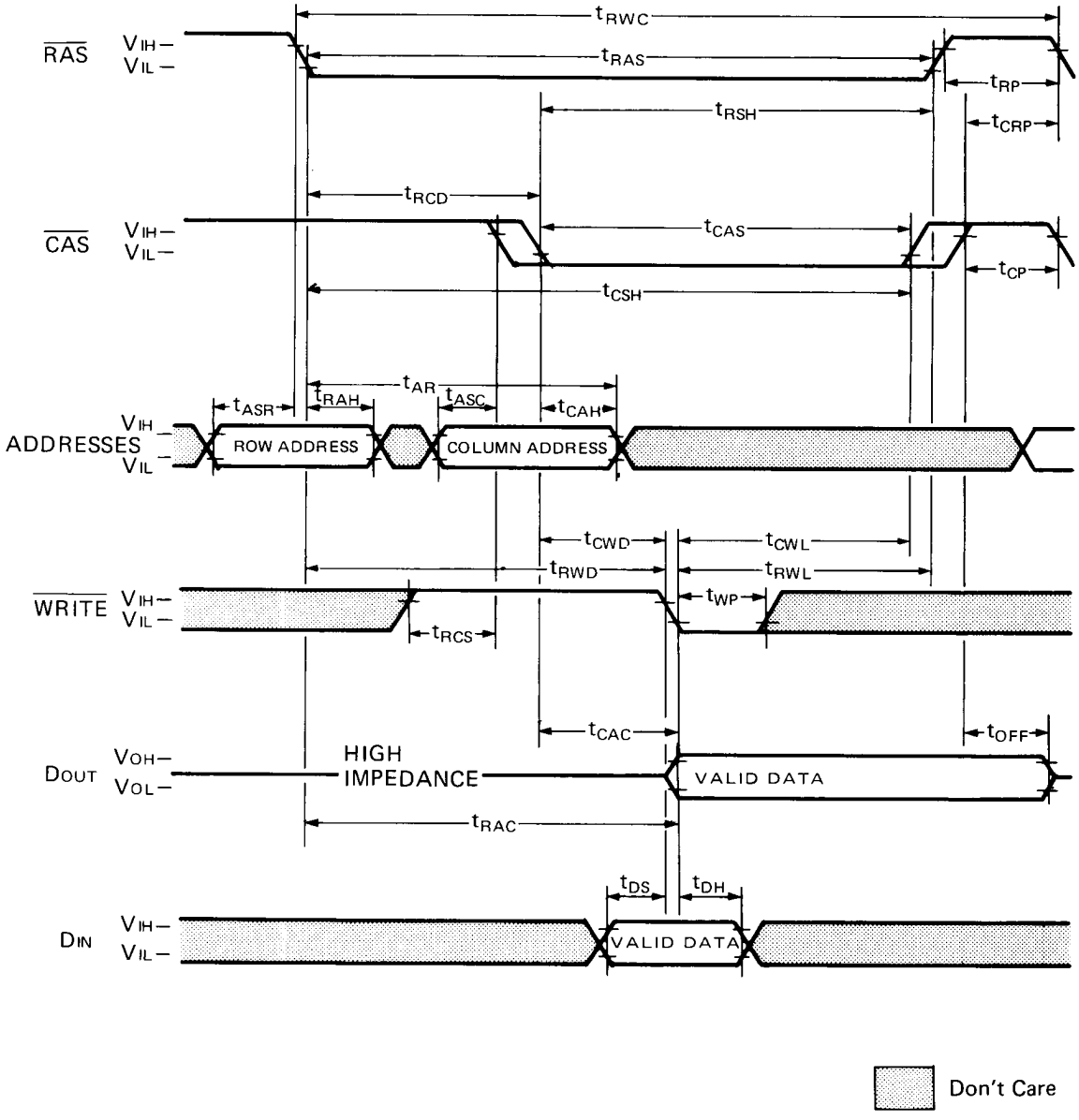
1) Several cycles are required after power up or prolonged periods of $\overline{RAS}$ inactivity (2 ms) before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2) AC measurements assume t_T = 5.0 ns.
3) V_{IH} and V_{IL} are reference levels for measuring signal timings and transition times.
4) Assumes that $t_{RCD} \leqq t_{RCD}$ (Max).
5) Assumes that $t_{RCD} \geqq t_{RCD}$ (Max).
6) Measure with load equivalent to 2 TTL loads and 100pF.
7) t_{OFF} defines the time at which the output enters high impedance state. It is not referenced to levels of V_{IH} and V_{IL}.
8) Operation within the t_{RCD} (Max) limit ensures that t_{RAC} (Max) can be met. t_{RCD} is specified as a reference point only; if t_{RCD} is greater than the specifed t_{RCD} limit, then row access time is $t_{RCD} + t_{CAC}$.
9) These parameters are referenced to leading edge of $\overline{CAS}$ (Early-Write) or $\overline{WRITE}$ (Delayed-Write or Read-Modify-Write) whichever occurs last.
10) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included under AC Characteristics as electrical characteristics only. If $t_{WCS} \leqq t_{WCS}$ (Min), the cycle is an Early-Write cycle and the data out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (Min) and $t_{RWD} \geqq t_{RWD}$ (Min), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE

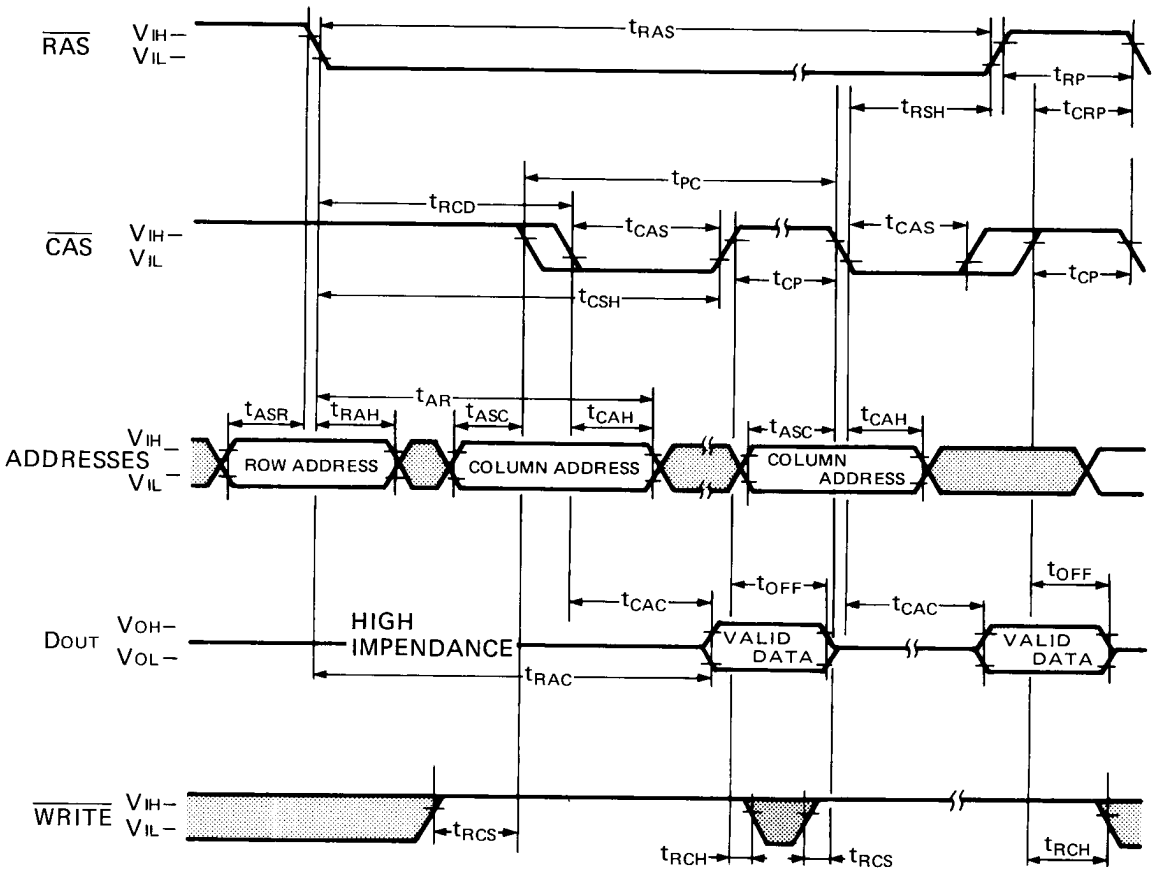




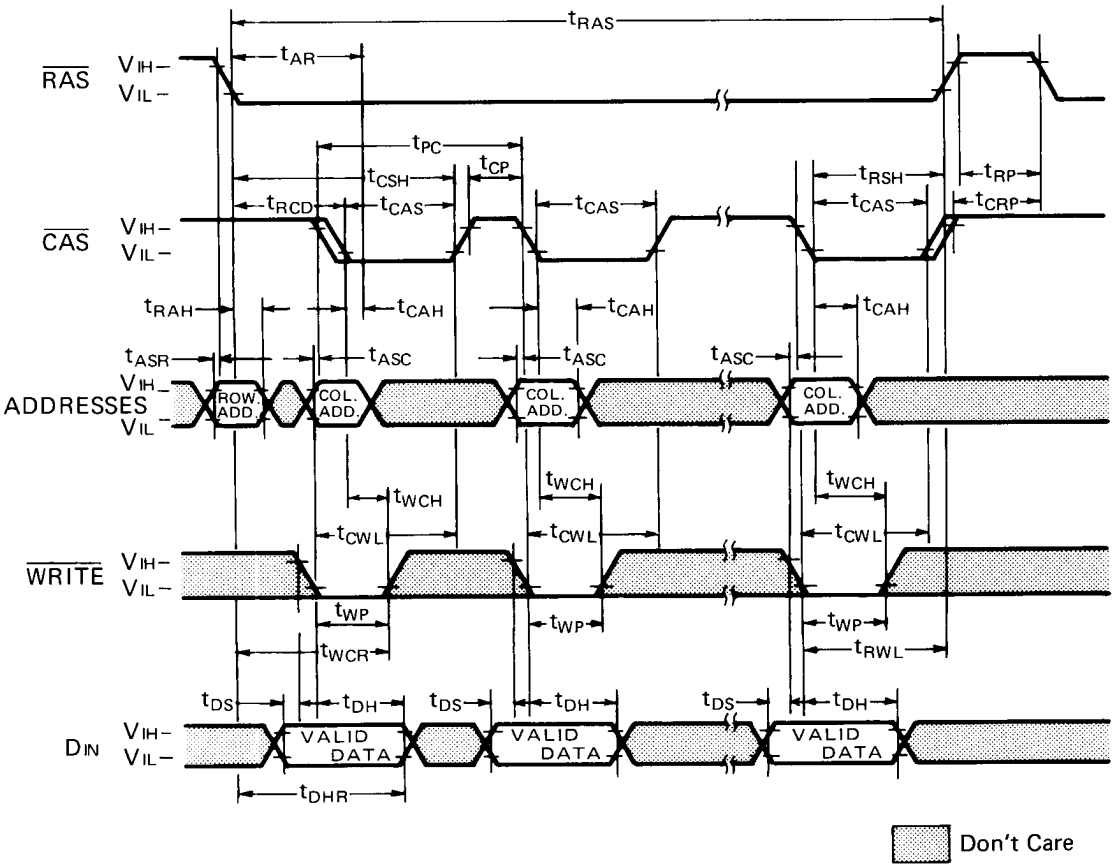
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

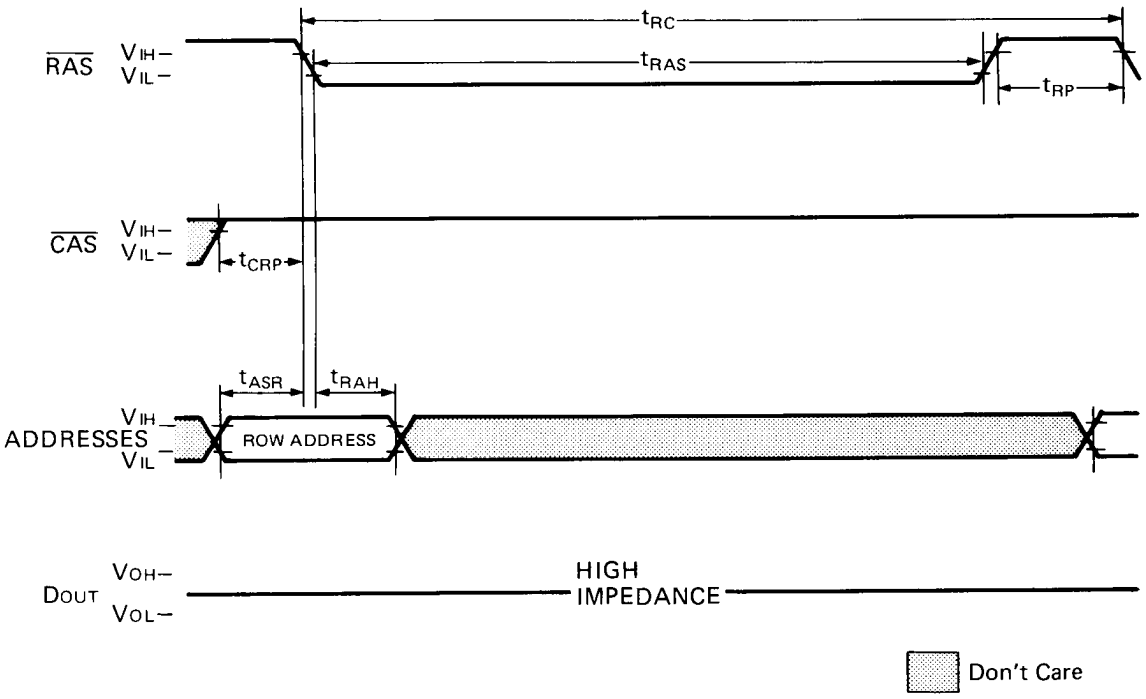


PAGE MODE WRITE CYCLE



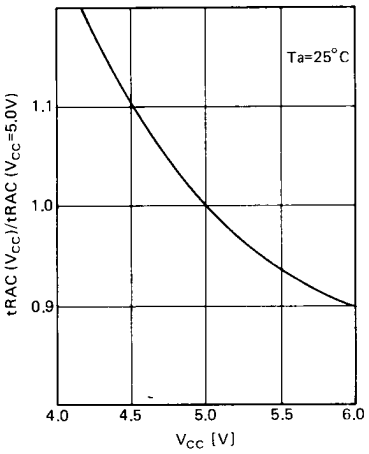
"RAS ONLY" REFRESH CYCLE

Note: $\overline{\text{WRITE}}$ = Don't Care

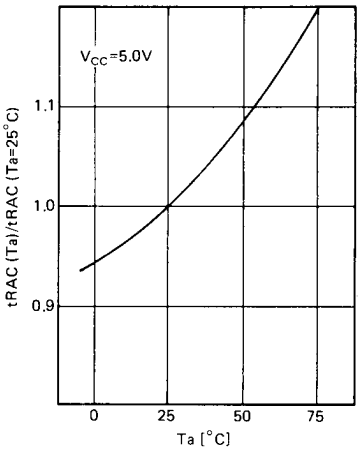


Typical Characteristics Curves

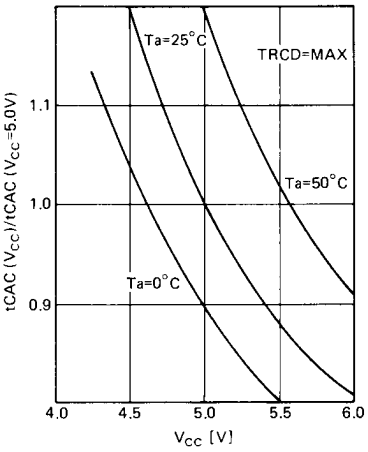
Access time from $\overline{RAS}$ (Relative value) v.s. V_{CC}



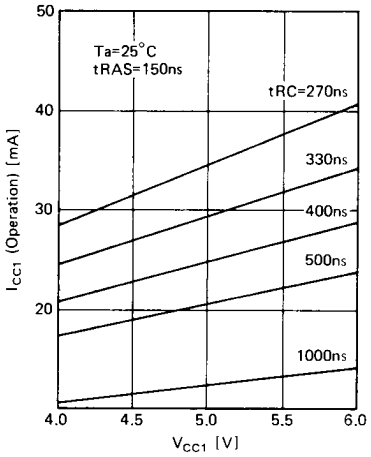
Access time from $\overline{RAS}$ (Relative value) v.s. Ta



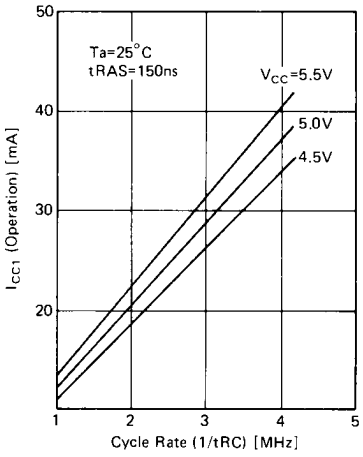
Access time from $\overline{CAS}$ (Relative value) v.s. V_{CC}



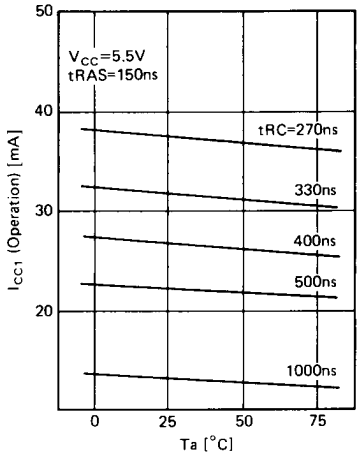
I_{CC1} (tRAS: Constant) v.s. V_{CC}



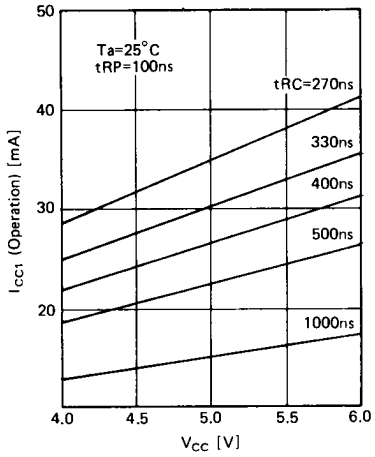
I_{CC1} (tRAS: Constant) v.s. Cycle Rate



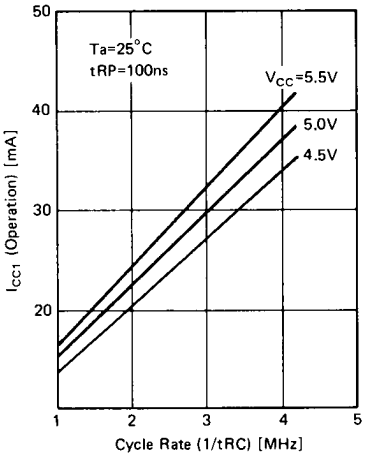
I_{CC1} (tRAS: Constant) v.s. Ta



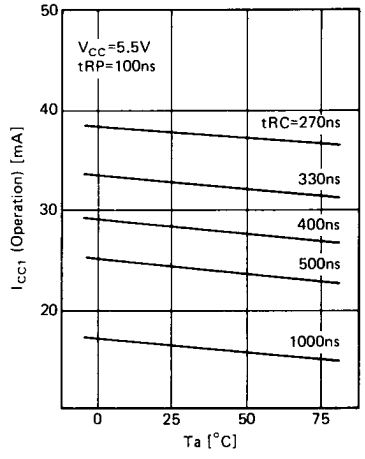
I_{CC1} (tRP: Constant) v.s. V_{CC}



I_{CC1} (tRP: Constant) v.s. Cycle Rate

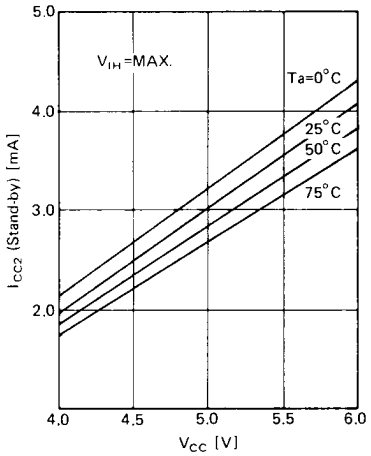


I_{CC1} (tRP: Constant) v.s. Ta

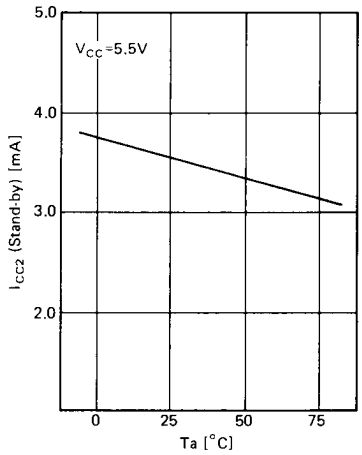


Typical Characteristics Curves (Continued)

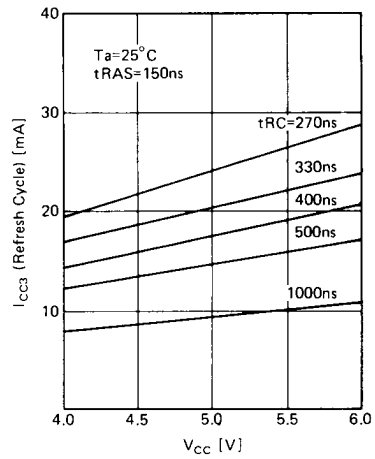
I_{CC2} vs. V_{CC}



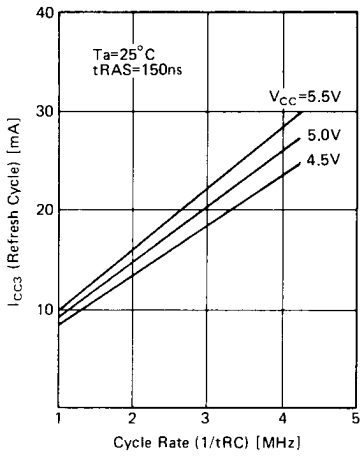
I_{CC2} v.s. Ta



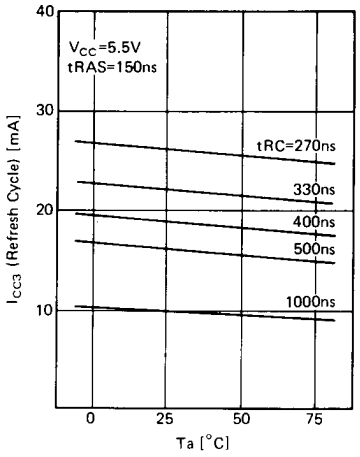
I_{CC3} (tRAS: Constant) v.s. V_{CC}



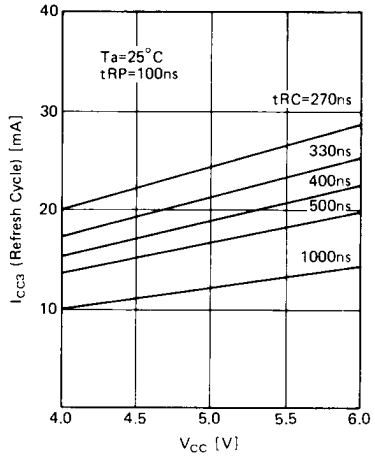
I_{CC3} (tRAS: Constant) v.s. Cycle Rate



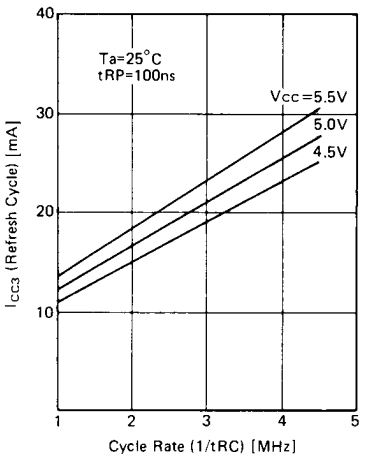
I_{CC3} (tRAS: Constant) v.s. Ta



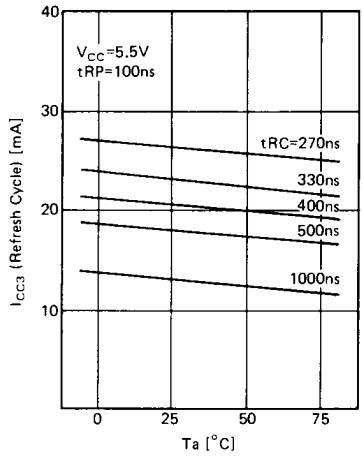
I_{CC3} (tRP: Constant) v.s. V_{CC}



I_{CC3} (tRP: Constant) v.s. Cycle Rate

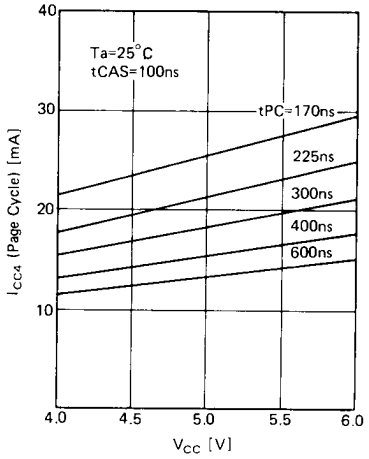


I_{CC3} (tRP: Constant) v.s. Ta

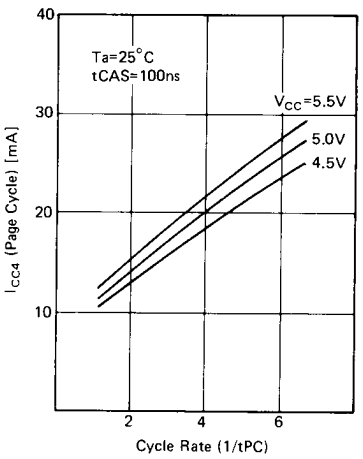


Typical Characteristics Curves (Continued)

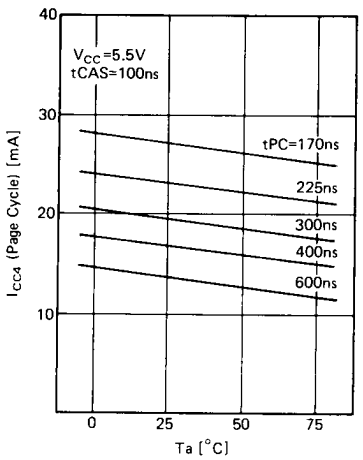
I_{CC4} (tCAS: Constant) v.s. V_{CC}



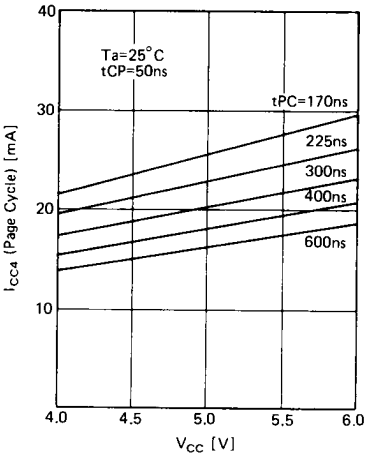
I_{CC4} (tCAS: Constant) v.s. Cycle Rate



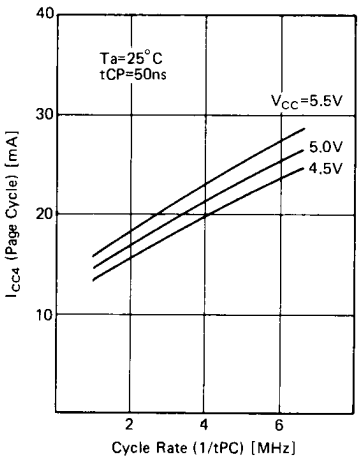
I_{CC4} (tCAS: Constant) v.s. Ta



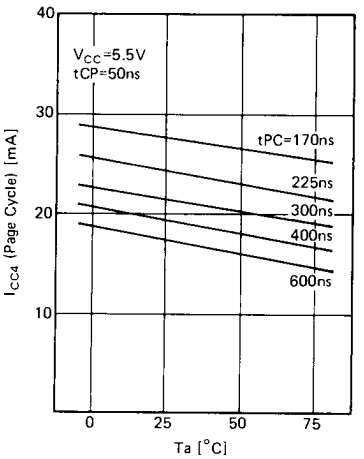
I_{CC4} (tCP: Constant) v.s. V_{CC}



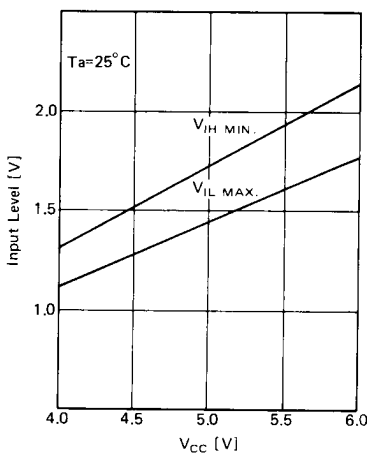
I_{CC4} (tCP: Constant) v.s. Cycle Rate



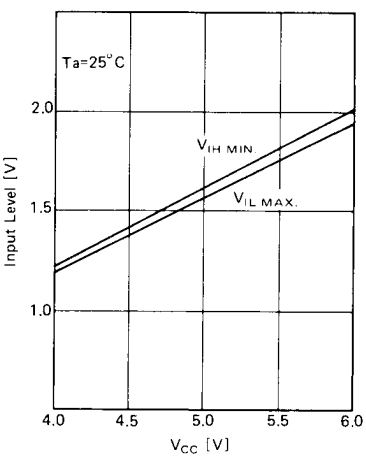
I_{CC4} (tCP: Constant) v.s. Ta



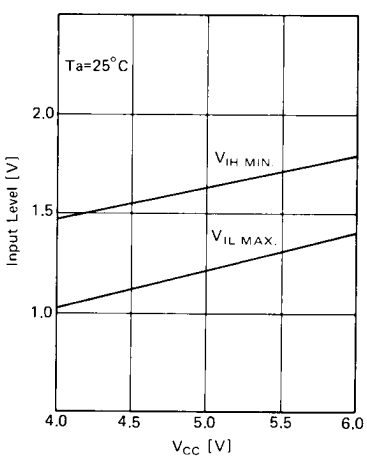
Address Input v.s. V_{CC}



Data Input v.s. V_{CC}

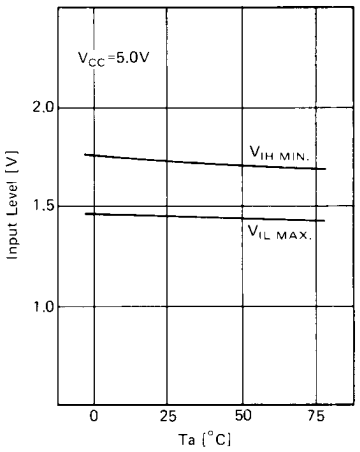


Clock Input v.s. V_{CC}

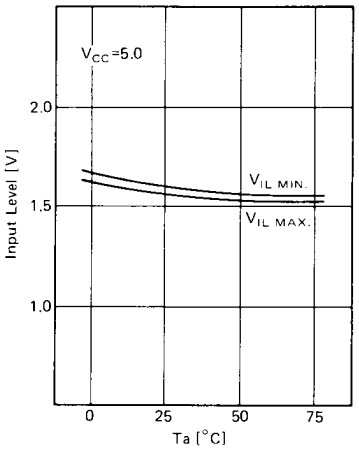


Characteristics Curves (Continued)

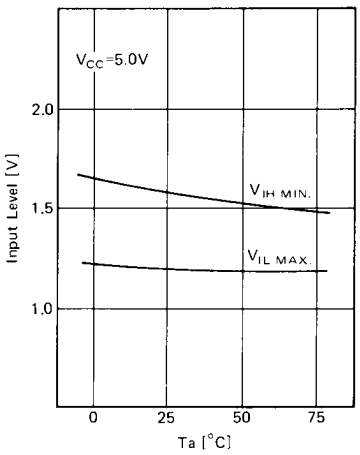
Address Input v.s. Ta



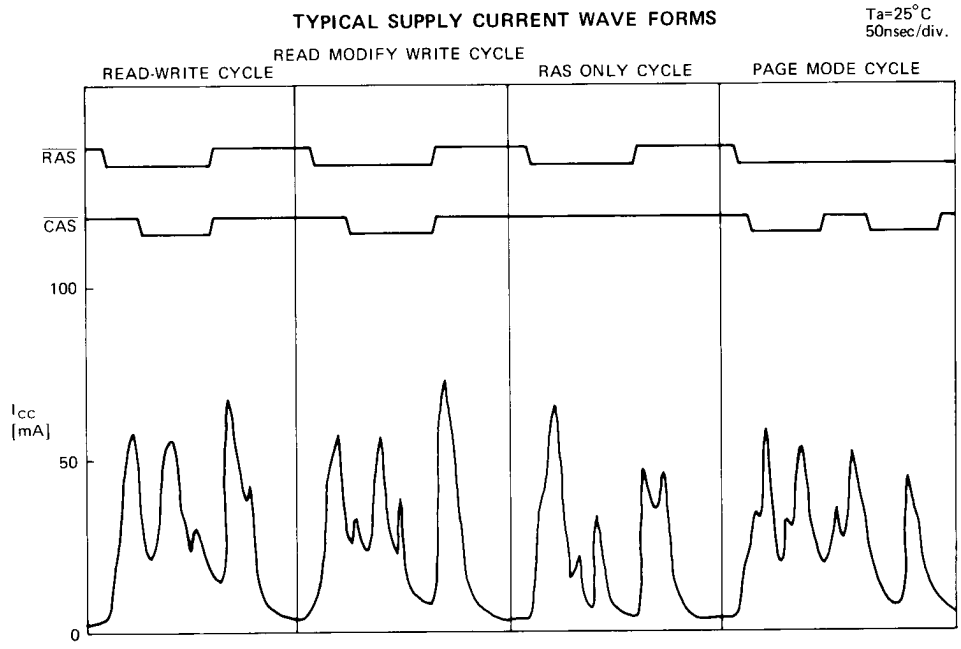
Data Input v.s. Ta



Clock Input v.s. Ta



Typical Supply Current Wave Forms



Functional Description

Address Input

The 16 address bits required to decode 1 of the 65,536 cell locations within the RAM module are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 8 row addresses bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. ($A_0 \sim A_7$ are row and column address input.) Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by defferent delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated CAS" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time (t_{RAH}) has been satisfied and the address inputs have been changed from row address to column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing specifications result from the internal gating of $\overline{CAS}$; they are t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the RAM module at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determind exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be increased by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input Control

Data is retrieved from memory in a read cycle by maintainig $\overline{WRITE}$ in the inactive or high state throghout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data in register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set up and hold times are referenced to $\overline{CAS}$.

If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a Read-Modify-Write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this delayed write cycle, the data input set up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.(To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the "Read-Modify-Write" cycle while the "WRITE" and "Page-Mode-Write" cycle diagrams show D_{IN} referenced to $\overline{CAS}$.)

Data Output

The normal condition of the data output (D_{OUT}) of the RAM module is a high impedance state. That is to say, any time $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the outputs will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high) conditions.

If the memory cycle in progress is "Read" or "Read-Modify-Write" cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active the output will remain valid until $\overline{CAS}$ is taken to the precharge state, whether or not $\overline{RAS}$ goes into precharge

If the cycle in progress is a "Write" cycle (Write active before $\overline{CAS}$ goes acrtive), then the output pins will maintain the high impedance throughout the entire cycle.

Note that with this type of output corfiguration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during write operations, and the pulse width of $\overline{CAS}$ during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (streching cycle). This type of output operation results in some very significant system implications.

Common I/O

If all write operations are handled in the "Write" cycle mode ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then D_{IN} can be connected directly to D_{OUT} respectively for common I/O data bus.

$\overline{RAS}$ and $\overline{CAS}$ Chip Selection

Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle. Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory device in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If a common $\overline{CAS}$ scheme is used where $\overline{RAS}$ is decoded for module selection, then total memory power can be conserved. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Page Mode

The "Page-Mode" feature of the RAM module allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing row address into the chip and maintaing the $\overline{RAS}$ signal at a logic 0 throughout all succesive memory cycle in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The succesive memory operations in "Page-Mode" may be any sequence of read, write, or read-modify-write operations.

The page boundary of a single RAM module is limited to the 256 column locations determined by all combinations of the 8 column address bits. However, in system applications which utilize more than 65,536 data words (more than one 64K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 ms time interval. Althogh any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycles. $\overline{RAS}$-Only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

MATSUSHITA ELECTRONICS CORPORATION
SEMICONDUCTOR DIVISION
Nagaokakyo, Kyoto, Japan

Export Division: MATSUSHITA ELECTRIC TRADING CO., LTD.
- Head Office: P.O. Box 288, Osaka Japan

U.S. Sales Office: PANASONIC INDUSTRIAL COMPANY, Division of Matsushita Electric Corporation of America Electronics Components Division
- Head Office: One Panasonic Way, Secaucus, N.J. 07094
  Tel: (201) 348-5268 (S.C. General), 348-5273 (OPT)
  348-5270 (IC/LSI), 348-5274 (TR)
- Eastern Regional Office: One Panasonic Way, Secaucus, N.J. 07094
  Tel: (201) 348-5233
- Central Regional Office: 425 East Argonquin Road, Arlington Hights, Ill. 6005
  Tel: (312) 981-4837
- Western Regional Office: 6550 Katella Ave, Cypress, Ca. 90630
  Tel: (714) 895-7200
- Southern Regional Office: Two MECA Way, Norcross, Ga. 30093
  Tel: (404) 923-9700

Distributor:

02833M Ⓐ Printed in JAPAN