MAS9188

12 × 8-Bit D to A Converter

- **3-Pin Serial Data Interface**
- **Low Voltage Output Buffer**
- **Replaces 12 Potentiometers**
- **Individually Programmable Outputs**
- **Fully Operational Down to 1.2 V**

DESCRIPTION

MAS9188 is 12-channel 8-bit DAC, designed primarily for trimmer replacement. The device is controlled by a simple 3-line input.

The DAC is selected with the four first bits in the serial input data (SDI-pin) and the DAC output value is set according to the last 8 bits in the serial input data.

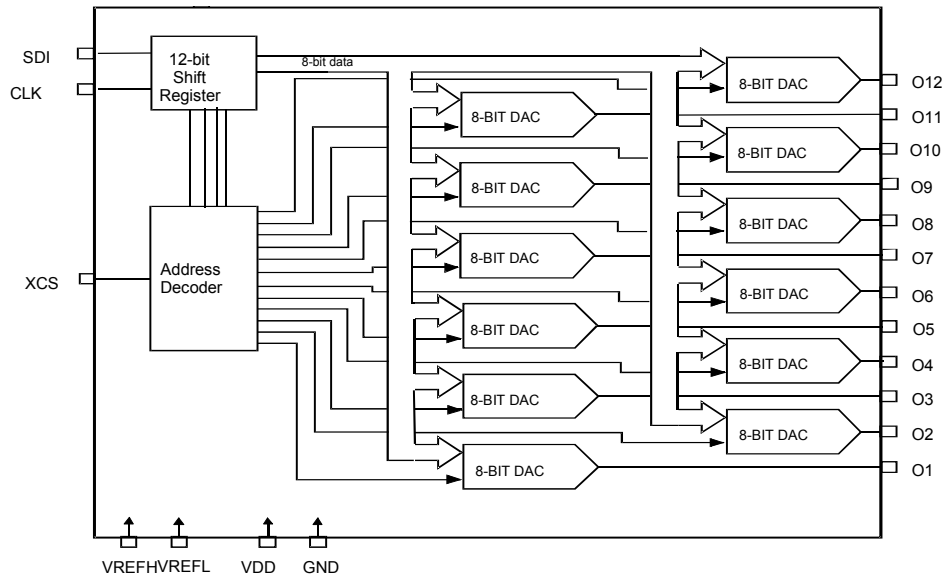
FEATURES

- Twelve 8-Bit DACs on a Single Monolithic Chip
- Voltage Level Output
- TSSOP-20 Package
- Single, Low +1.2 V Supply
- Power-On Reset
- Functionally and Pin Compatible with AD8802/AD8804

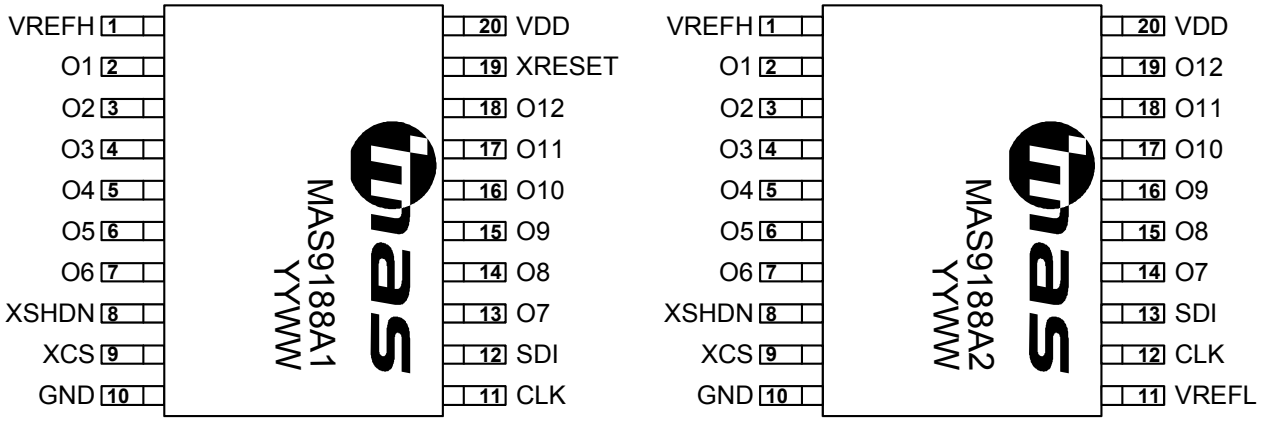
APPLICATIONS

- High Resolution Monitors
- Automatic Gain Control
- Trimmer Replacement
- Portable and Battery-Operated Equipment

BLOCK DIAGRAM



PIN CONFIGURATION



Top view
YYWW = year, week

PIN DESCRIPTION

Pin Number	MAS9188 A1	MAS9188 A2	Function
1	VREFH	VREFH	DAC output reference high voltage
2	O1	O1	DAC 1, address 0x0
3	O2	O2	DAC 2, address 0x1
4	O3	O3	DAC 3, address 0x2
5	O4	O4	DAC 4, address 0x3
6	O5	O5	DAC 5, address 0x4
7	O6	O6	DAC 6, address 0x5
8	XSHDN	XSHDN	Device analog part power-down signal (active low)
9	XCS	XCS	Device enable signal (rising edge loads data to DAC)
10	GND	GND	Device ground-pin
11	CLK	VREFL	Data clock / DAC output low reference voltage
12	SDI	CLK	Serial input data / Data clock
13	O7	SDI	DAC 7, address 0x6 / Serial input data
14	O8	O7	DAC 8, address 0x7 / DAC 7, address 0x6
15	O9	O8	DAC 9, address 0x8 / DAC 8, address 0x7
16	O10	O9	DAC 10, address 0x9 / DAC 9, address 0x8
17	O11	O10	DAC 11, address 0xA / DAC 10, address 0x9
18	O12	O11	DAC 12, address 0xB / DAC 11, address 0xA
19	XRESET	O12	Device Digital part reset – middle code preset pin / DAC 12, address 0xB
20	VDD	VDD	Device power supply pin

MAS9188 has two bonding options available:

- MAS9188A1, where VREFL pin is bonded to GND pin and XRESET pin can be used
- MAS9188A2, where XRESET pin is bonded to VDD pin and VREFL pin can be used

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply (VDD to GND)	VDD		-0.3	6.0	V
Input Voltage Range (any other pin)			-0.3	VDD + 0.3	V
Operating Temperature Range			-40	+85	°C
Storage Temperature Range			-65	+150	°C

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VDD		1.2	3.6	5.5	V
Operating Temperature Range	Temp		-40		+85	°C

ELECTRICAL CHARACTERISTICS

DC Parameters

◆ Digital Inputs

VDD = 2.4…5.5 V, VREFH = VDD, VREFL = 0 V, -40°C ≤ T_A ≤ +85°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DAC Resolution	N			8		Bits
DAC Differential Nonlinearity Error	DNL		-1		+1	LSB
DAC Integral Nonlinearity Error	INL		-1		+1	LSB
DAC Full-scale Error	GFSE		-1		+1	LSB
DAC Zero Code Error	BZSE		-1		+1	LSB
DAC Output Resistance	ROUT		3	5	8	kΩ

◆ Reference Input

VDD = 2.4…5.5 V, VREFH = VDD, VREFL = 0 V, -40°C ≤ T_A ≤ +85°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFH Voltage Range	VREFH	$V_{REFH} > V_{REFL}$	0		VDD	
REFL Voltage Range (MAS9188A2 only)	VREFL	$V_{REFH} > V_{REFL}$	0		VDD	
REFH Input Resistance	RREFH		0.5	1.1		kΩ
REFL Input Resistance	RREFL			1.1		kΩ
ROUT Matching ($\Delta R_{OUT}/R_{OUT}$)	RMATCH			0.4	2	%

◆ Digital Input

VDD = 2.4…5.5 V, VREFH = VDD, VREFL = 0 V, -40°C ≤ T_A ≤ +85°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Logic High	VIH		0.7 × VDD			
Digital Logic Low	VIL				0.3 × VDD	
Digital Input Current	IIL				± 1	µA

◆ Power Supplies

VDD = 2.4…5.5 V, VREFH = VDD, VREFL = 0 V, -40°C ≤ T_A ≤ +85°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Range	VDD		1.2		5.5	V
Supply Current	IDD			0.01	5	µA
Shutdown Current	ISHDN			0.01	5	µA

AC Parameters

◆ AC Characteristics

Dynamic Performance

VDD = 2.4…5.5 V, VREFH = VDD, VREFL = 0 V, -40°C ≤ T_A ≤ +85°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Sensitivity	$\frac{\Delta V_{OUT}}{\Delta V_{DD}}$	ΔV_{DD} = 1.1 × V_{DD} – 0.9 × V_{DD}		0.12		%
Power Supply Sensitivity (100 Hz)	PSRR			65		dB
Vout Settling time (±1/2 LSB error band)	TS			5		µs
Crosstalk between adjacent outputs	CT			50		dB

Switching Characteristics

VDD = 3.6 V, VREFH = VDD, VREFL = 0 V, T_A = +25°C unless otherwise noted

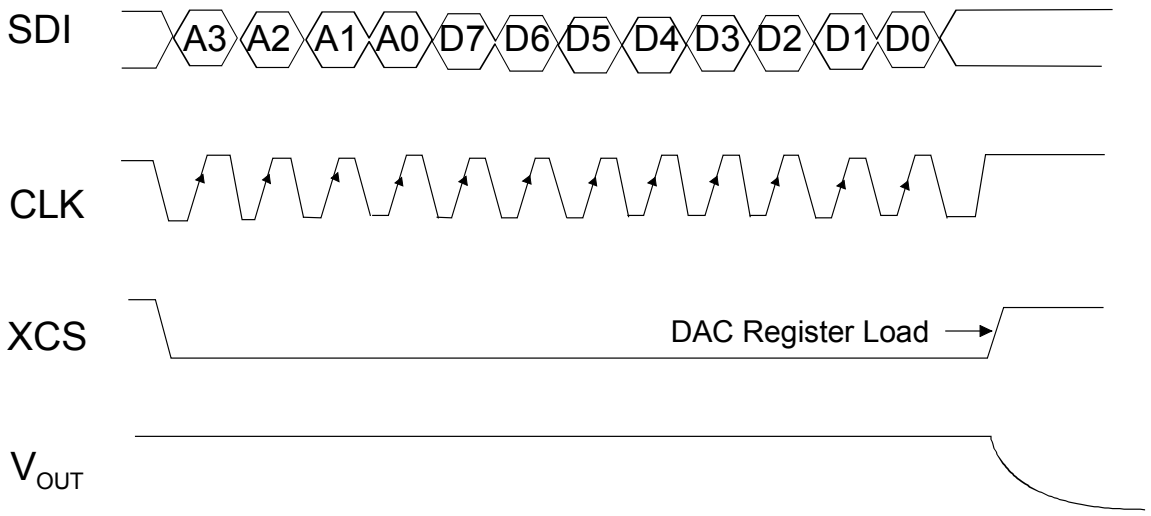
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Clock High Pulse Width	TCH			17		ns
Input Clock Low Pulse Width	TCL			8		ns
Data Setup Time	TDS			-7		ns
Data Hold Time	TDH			24		ns
XCS Fall to First Clock Pulse Fall	TCLCL			18		ns
XCS High Pulse Width	TCSW			10		ns
CLK Rise to XCS Rise Hold Time	TCSH			22		ns
XCS Rise to CLOCK Rise Setup	TCS1			7		ns
RESET Pulse Width	TRS			18		ns

OPERATING MODES

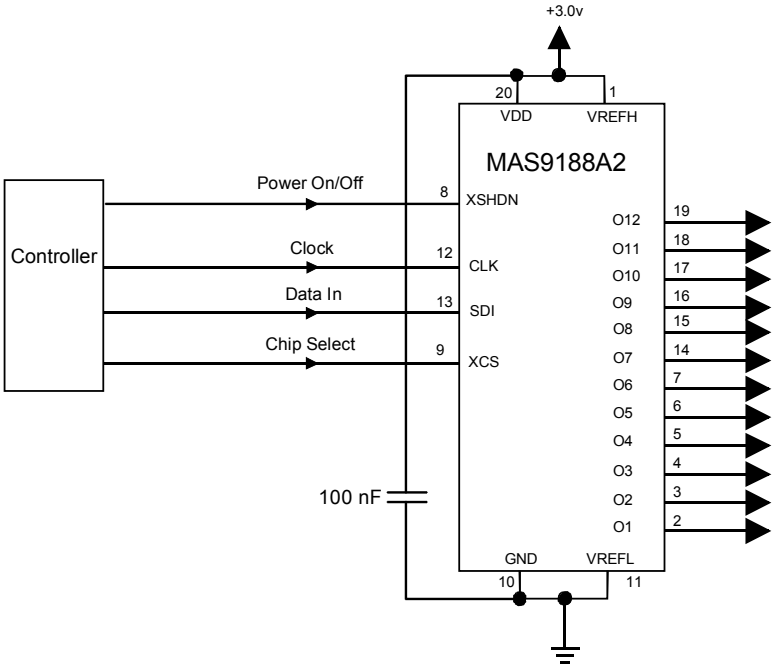
DAC maximum output voltage is set using VREFH and VREFL pins (= 255/256 * (VREFH-VREFL)+VREFL) (note: VREFL = GND in case of MAS9188A1). The XRESET pin is used for middle code preset: DAC registers are reset and middle code will appear at the DAC output.

Serial input data is written to SDI while XCS is low. Data is read at CLK rising edge to on-chip shift register. Rising XCS-pin reads data and 12 CLK-cycles are used as the input data (4 address bits and 8 data bits). The last 12 bits before rising XCS are used as input data.

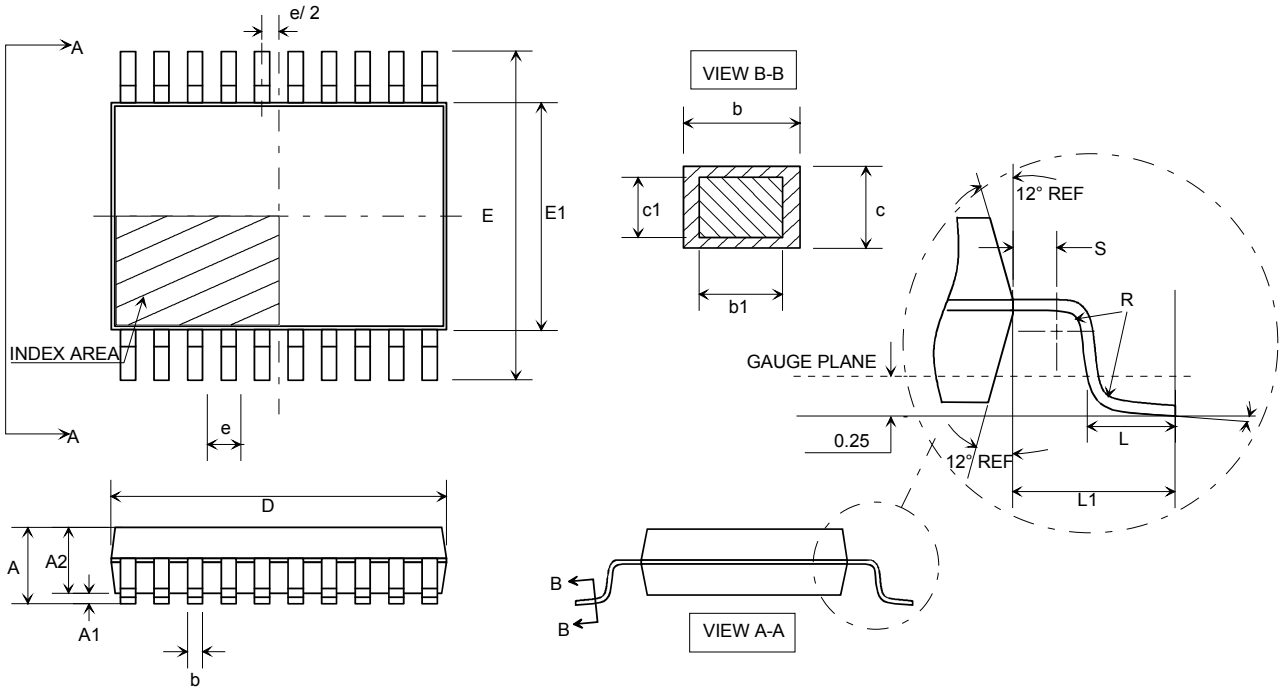
◆ **Timing diagram**



APPLICATION AND TEST CIRCUIT INFORMATION



PACKAGE (TSSOP-20) OUTLINES



Symbol	Min	Nom	Max	Unit
A	--	--	1.10	mm
A1	0.05	--	0.15	mm
A2	0.85	0.90	0.95	mm
b	0.19	--	0.30	mm
b1	0.19	0.22	0.25	mm
c	0.09	--	0.20	mm
c1	0.09	--	0.16	mm
D	6.40	6.50	6.60	mm
E		6.4 BSC		mm
E1	4.30	4.40	4.50	mm
e		0.65 BSC		mm
L	0.50	0.60	0.75	mm
L1		1.00 REF		
R	0.09	--	--	mm
S	--	0.20	--	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.
Reference Standard : JEDEC MO-153 .

SOLDERING INFORMATION

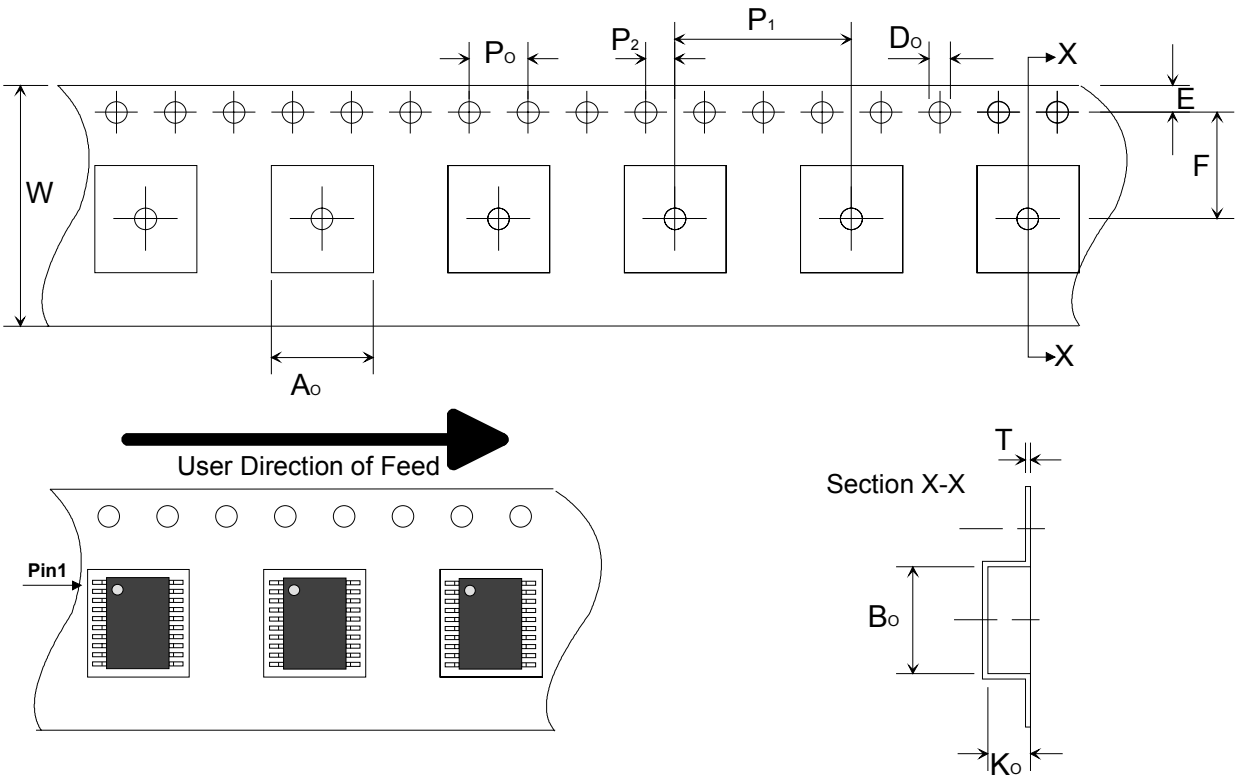
◆ **For For Eutectic Sn/Pb TSSOP-20**

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

◆ **For Green (Pb Free, RoHS Compliant) TSSOP-20**

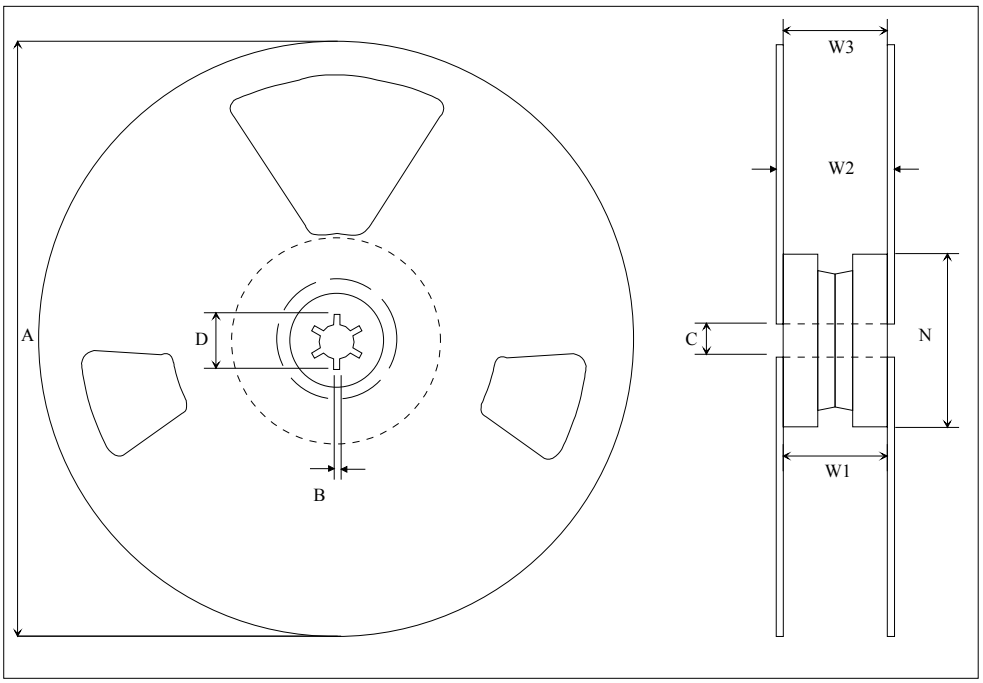
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS

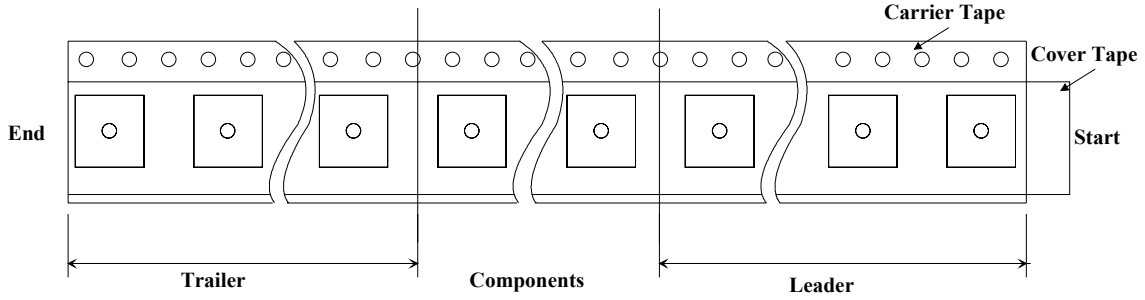


Dimension	Min/Max	Unit
A_o	6.70 ±0.10	mm
B_o	6.90 ±0.10	mm
D_o	1.50 +0.1/-0.0	mm
E	1.75	mm
F	7.50 ±0.10	mm
K_o	1.30 ±0.10	mm
P_o	4.0	mm
P_1	12.0 ±0.10	mm
P_2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	16.00 +0.30/-0.10	mm

REEL SPECIFICATIONS



- 2500 Components on Each Reel
- Reel Material: Conductive, Plastic Antistatic or Static Dissipative
- Carrier Tape Material: Conductive
- Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	16.4	18.4	mm
W_2 (measured at hub)		22.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9188AUA1	12 x 8-bit D to A Converter	TSSOP-20	0 V Reference Level
MAS9188AUA2	12 x 8-bit D to A Converter	TSSOP-20	Adjustable Reference Level
MAS9188A1UC06	12 x 8-bit D to A Converter	TSSOP-20 Pb free, RoHS compliant	0 V Reference Level
MAS9188A2UC06	12 x 8-bit D to A Converter	TSSOP-20 Pb free, RoHS compliant	Adjustable Reference Level

LOCAL DISTRIBUTOR

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