



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LC74900 — CMOS IC Silicon gate LCD PROCESSOR LSI for small size display

Overview

LC74900 is a highly integrated multi-purpose LCD Panel (up to WVGA) controller processing analog and digital video signal.

It contains A/D converter, video decoder, De-interlacer/Scaler, and picture improvement.

Features

(1) Video Input/Output

- Analog input: 4ch CVBS (NTSC, PAL, and SECAM) with 1ch 10bit A/D converter
- Digital input: 24bit RGB and YCbCr, 16bit YCbCr (4:2:2), and 8bit YC (BT.656)
- Digital output: 8bit video decoder output (BT.656)

(2) YC separation video decoder

- Adaptive 3line comb filter, automatic gain and chrominance control

(3) De-interlacer and Scaler

- Horizontal and vertical programmable scaler separately, and supports panels up to WVGA resolutions

(4) Picture Improvements

- CDEX (Color Depth Expander): high quality expansion for low-resolution graphics
- Dynamic gamma correction: picture adapted automatic luminance control
- Sharpness control, LTI and CTI: peaking enhancement without glares
- Color exciter: 6 phases RGBYMC gain control separately

(5) Panel interface

- 24bit RGB output and 18bit RGB output with dithering process
- Pulse Width Modulation for automatic LED backlight control
- Timing controller for LCD driver with horizontal or vertical reversing signals
- Pin swapping : replace output pin assignment of the RGB channel or bit

Continued on next page.

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment. The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for new introduction or other application different from current conditions on the usage of automotive device, communication device, office equipment, industrial equipment etc. , please consult with us about usage condition (temperature, operation time etc.) prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co., Ltd.

<http://semicon.sanyo.com/en/network>

Continued from preceding page.

(6) On Screen Display

- Built-in OSD controller with integrated font ROM, which contains 501 fonts, and font RAM, which contains 8 fonts
- Character Numbers displayed on the screen: 24 characters by 8 rows, 24 characters by 10 rows, or 32 characters by 8 rows
- Character Size: 16 pixels wide by 20 pixels high
- Character Colors: 8 font colors for each character, 8 back colors for each character, and 8 font border colors for each row
- Inverting font colors and back colors each character, Blinking fonts each character, and Fringing each row
- Pin assignment for an optional external OSD controller: 24bit, 18bit, 12bit, and 6bit RGB

(7) EEPROM booting

- Quick boot from an external EEPROM in power on sequence before starting a system controller
- Waiting timer between data transfers
- Verifying boot datas
- EEPROM Size: Up to 512K bits with I²C or SPI interface

(8) Parallel data outputs, panel interface and video decoder output

- Reentering video decoder outputs, which are processed by an external graphic engine as digital inputs

(9) System Controller Interface

- SPI (Max 1Mbit/s) or I²C bus (100Kbit/s or 400Kbit/s)

LSI Specification

- Supply voltage: 1.5V (core), 3.3V (IO)
- Maximum operation frequency: 60MHz (video processing)
- Package: 120pin TQFP

Applications

- For mediam or small size LCD Panel
- Automobile use: car TV, portable navigation, etc.
- Home use: Photo Frame, Portable DVD, Door Phone, etc.

LC74900

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $ADC0AV_{SS} = 0\text{V}$, $ADC1AV_{SS} = 0\text{V}$, $PLLAV_{SS} = 0\text{V}$, $XV_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (I/O)	DV_{DD33} XV_{DD33} DV_{DD3318}		-0.3 to +3.96	V
Maximum supply voltage (Analog)	$ADC0AV_{DD33}$ $ADC1AV_{DD33}$ $PLLAV_{DD33}$		-0.3 to +3.96	V
Maximum supply voltage (Core)	DV_{DD15}		-0.3 to +1.8	V
Digital input voltage	V_I		-0.3 to $DV_{DD33}+0.3$	V
	V_I (5V Tolerant)		-0.3 to $DV_{DD3318}+0.3$	
Digital output voltage	V_O		-0.3 to $DV_{DD33}+0.3$	V
			-0.3 to $DV_{DD3318}+0.3$	
Maximum allowable loss	$P_d \text{ max}$	$T_a = 85^\circ\text{C}$, With evaluation board*	0.7	W
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$

*: Board size: 150mm × 150mm × 1.6mm, FR-4, 6layers

Allowable Operation Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $ADC0AV_{SS} = 0\text{V}$, $ADC1AV_{SS} = 0\text{V}$, $PLLAV_{SS} = 0\text{V}$, $XV_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (I/O)	DV_{DD33} XV_{DD33}		3.15	3.3	3.45	V
	DV_{DD3318}		3.15	3.3	3.45	V
			1.7	1.8	1.9	V
Supply voltage (Analog)	$ADC0AV_{DD33}$ $ADC1AV_{DD33}$ $PLLAV_{DD33}$		3.15	3.3	3.45	V
Supply voltage (Core)	DV_{DD15}		1.4	1.5	1.6	V
Input voltage range	V_{IN}		0		DV_{DD33} DV_{DD3318}	V
Input voltage range (5V Tolerant)	V_{IN5}		0		5.5	V

LC74900

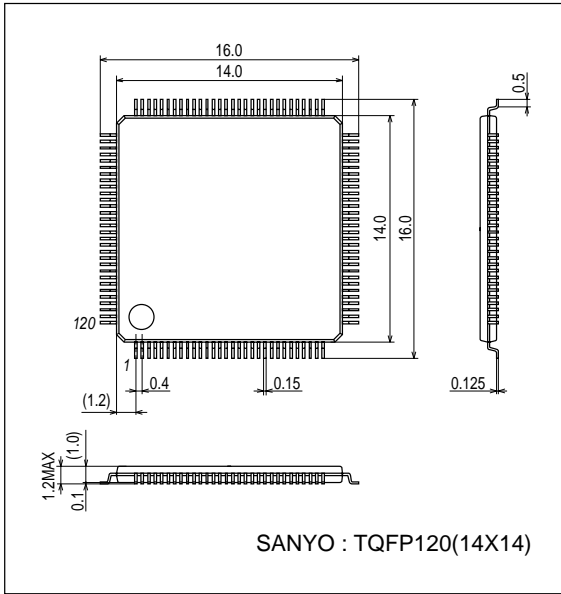
DC Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $DV_{SS} = 0\text{V}$, $ADC0AV_{SS} = 0\text{V}$, $ADC1AV_{SS} = 0\text{V}$, $PLLAV_{SS} = 0\text{V}$, $XV_{SS} = 0\text{V}$, $DV_{DD33} = 3.15\text{V}$ to 3.45V , $DV_{DD3318} = 3.15\text{V}$ to 3.45V or 1.7V to 1.9V , $DV_{DD15} = 1.42\text{V}$ to 1.58V , $XV_{DD33} = 3.15\text{V}$ to 3.45V , $ADC0AV_{DD} = 3.15\text{V}$ to 3.45V , $ADC1AV_{DD} = 3.15\text{V}$ to 3.45V , $PLLAV_{DD} = 3.15\text{V}$ to 3.45V

Parameter	Symbol	Conditions	min	typ	max	unit
Input high-level voltage	V_{IH}	CMOS level inputs	$0.7DV_{DD33}$ $0.7DV_{DD3318}$			V
		CMOS level Schmitt inputs	$0.7DV_{DD33}$			V
Input low-level voltage	V_{IL}	CMOS level inputs	0		$0.3DV_{DD33}$ $0.3DV_{DD3318}$	V
		CMOS level Schmitt inputs	0		$0.3DV_{DD33}$	V
Input high-level current	I_{IH}	$V_I = DV_{DD33}$				μA
		$V_I = DV_{DD3318}$				μA
Input low-level current	I_{IL}	$V_I = DV_{SS}$				μA
Output high-level voltage	V_{OH}	Type B: $I_{OH} = -4\text{mA}$ Type G: $I_{OH} = -6\text{mA}$ $DV_{DD3318} = 3.15\text{V}$ to 3.45V	$DV_{DD33}-0.6$			V
		Type J: $I_{OH} = -4\text{mA}$ Type K: $I_{OH} = -6\text{mA}$	$DV_{DD3318}-0.6$			V
		$DV_{DD3318} = 1.7\text{V}$ to 1.9V Type J: $I_{OH} = -3\text{mA}$ Type K: $I_{OH} = -5\text{mA}$	$DV_{DD3318}-0.4$			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leakage current	I_{OZ}	When in high-impedance output mode	-10		10	μA
Operating current drain	I_{DDOP}	Output open, tck = 9MHz, 10steps $T_a = 25^\circ\text{C}$, $DV_{DD33} = 3.3\text{V}$, $DV_{DD3318} = 3.3\text{V}$, $XV_{DD} = 3.3\text{V}$, $DV_{DD15} = 1.5\text{V}$, $ADC0AV_{DD} = 3.3\text{V}$, $ADC1AV_{DD} = 3.3\text{V}$, $PLLAV_{DD} = 3.3\text{V}$		95		mA
		Output open, tck = 33MHz, 10steps $T_a = 25^\circ\text{C}$, $DV_{DD33} = 3.3\text{V}$, $DV_{DD3318} = 3.3\text{V}$, $XV_{DD} = 3.3\text{V}$, $DV_{DD15} = 1.5\text{V}$, $ADC0AV_{DD} = 3.3\text{V}$, $ADC1AV_{DD} = 3.3\text{V}$, $PLLAV_{DD} = 3.3\text{V}$		139		mA
Static current drain	I_{DDST}	Output open, tck: stop $V_I = DV_{SS}$, $T_a = 25^\circ\text{C}$, $DV_{DD33} = 3.3\text{V}$, $DV_{DD3318} = 1.8\text{V}$, $XV_{DD} = 3.3\text{V}$, $DV_{DD15} = 1.5\text{V}$, $ADC0AV_{DD} = 3.3\text{V}$, $ADC1AV_{DD} = 3.3\text{V}$, $PLLAV_{DD} = 3.3\text{V}$		34		μA

Package Dimensions

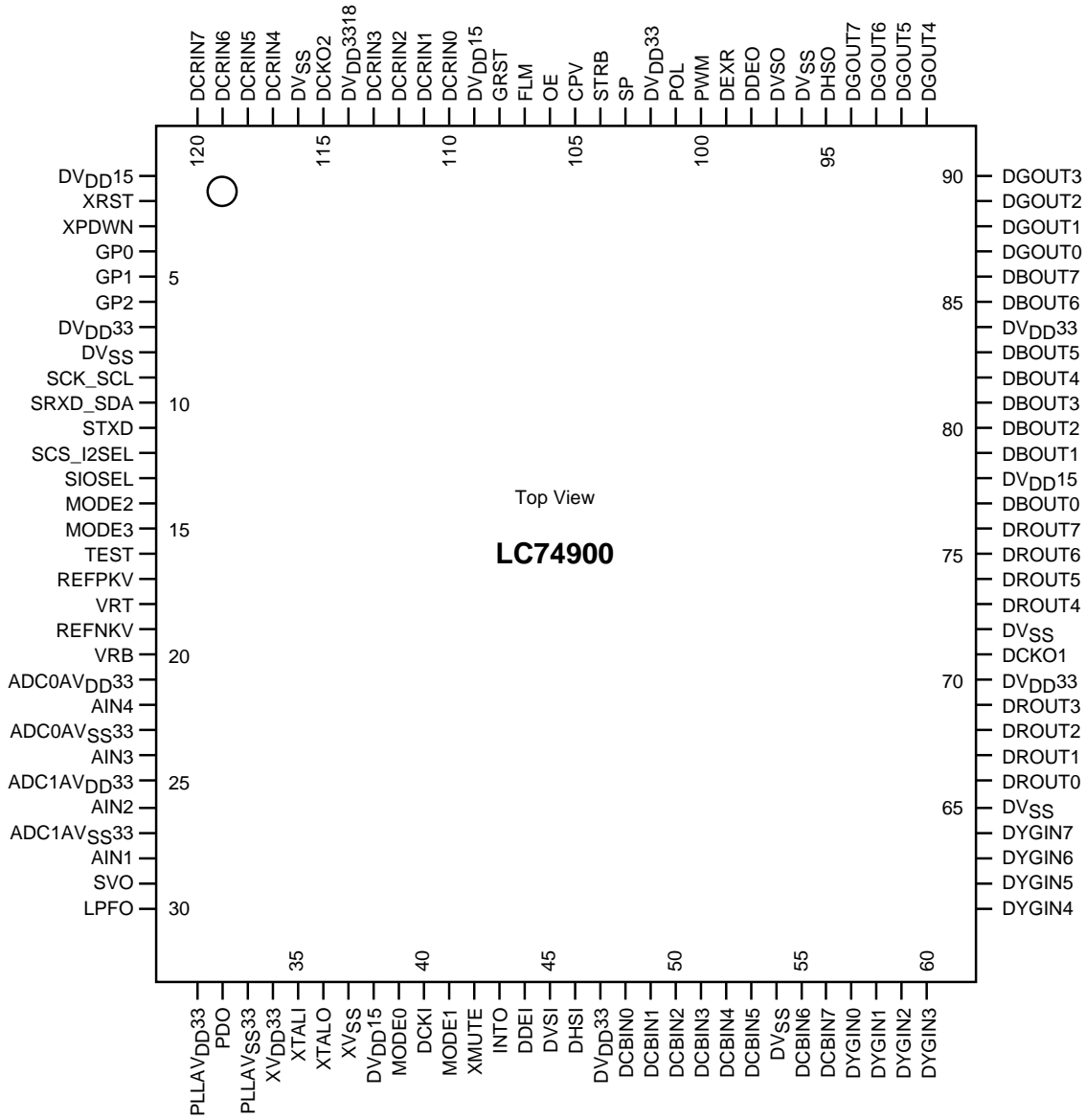
unit : mm (typ)

3257A



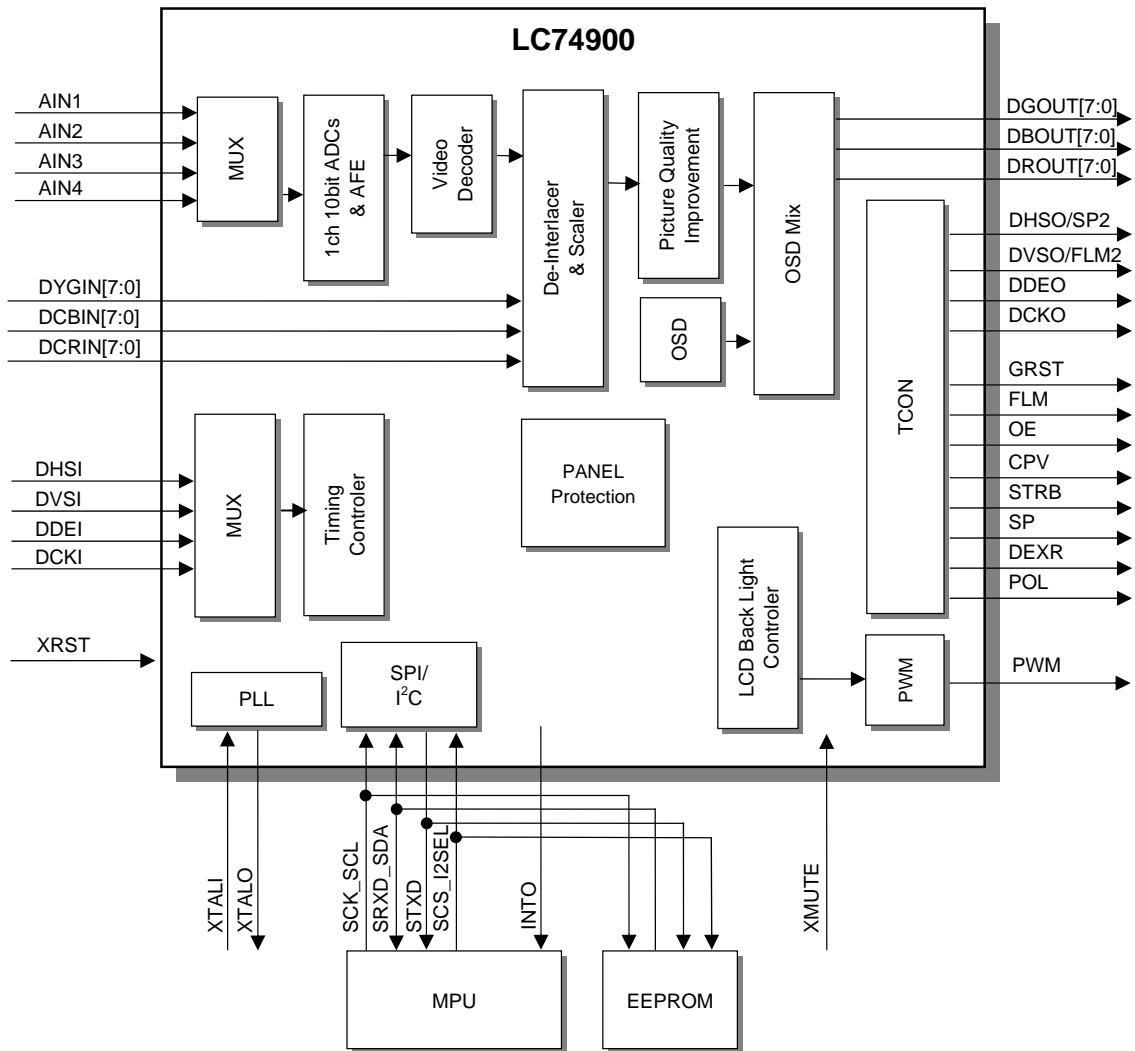
LC74900

Pin Assignment



LC74900

Block Diagram



LC74900

Pin Functions

Pin No.	Pin symbol	I/O format		Connected to		Digital IO power supply	Remarks
		I/O	Format				
1	DV _{DD} 15	P	-	Core voltage	Digital		Power supply for core (1.5V)
2	XRST	I	A	CMOS	Digital	DV _{DD} 33	Reset pin (active at a low voltage level)
3	XPDWN	I	A	CMOS	Digital	DV _{DD} 33	Fixed at a high voltage level
4	GP0	I/O	B	CMOS	Digital	DV _{DD} 33	Input: Digital input/OSD enable (pull down if not used) Output: Global port/Video decoder Vsync
5	GP1	I/O	B	CMOS	Digital	DV _{DD} 33	Input: Digital input/OSD halftone (pull down if not used) Output: Global Port/Video DecoderHsync
6	GP2	I/O	B	CMOS	Digital	DV _{DD} 33	Global port output
7	DV _{DD} 33	P	-	IO voltage	Digital		Power supply for IO (3.3V)
8	DV _{SS}	P	-	GND	Digital		GND for digital
9	SCK_SCL	I/O	C	CMOS	Digital	DV _{DD} 33	I ² C: I ² C Clock inout, SPI: Clock input
10	SRXD_SDA	I/O	C	CMOS	Digital	DV _{DD} 33	I ² C: data inout, SPI: data input
11	STXD	I/O	B	CMOS	Digital	DV _{DD} 33	SPI: data output
12	SCS_I2SEL	I	A	CMOS	Digital	DV _{DD} 33	I ² C: Select I ² C slave address, SPI: Chip select
13	SIOSEL	I	D	CMOS	Digital	DV _{DD} 33	Select CPU I/F, "L": I ² C, "H": SPI
14	MODE2	I	D	CMOS	Digital	DV _{DD} 33	Operation mode control
15	MODE3	I	D	CMOS	Digital	DV _{DD} 33	Operation mode control
16	TEST	I	D	CMOS	Digital	DV _{DD} 33	For production test (Fixed at a low voltage level)
17	REFPKV	I	E		Analog		Top reference level Buffer-AMP input for ADC
18	VRT	I	E		Analog		Top reference level for ADC
19	REFNKV	I	E		Analog		Bottom reference level Buffer-AMP input for ADC
20	VRB	I	E		Analog		Bottom reference level for ADC
21	ADC0AV _{DD} 33	P	-	Analog voltage	Analog		Power supply for ADC (3.3V)
22	AIN4	I	E		Analog		CVBS input 4
23	ADC0AV _{SS} 33	P	-	GND	Analog		GND for ADC
24	AIN3	I	E		Analog		CVBS input 3
25	ADC1AV _{DD} 33	P	-	Analog voltage	Analog		Power supply for ADC (3.3V)
26	AIN2	I	E		Analog		CVBS input 2
27	ADC1AV _{SS} 33	P	-	GND	Analog		GND for ADC
28	AIN1	I	E		Analog		CVBS input 1
29	SVO	O	E		Analog		AFE output
30	LPFO	O	E		Analog		External AGC control level
31	PLLAV _{DD} 33	P	-	Analog voltage	Analog		Power supply for PLL (3.3V)
32	PDO	O	-		Analog		Test port for PLL (Open)
33	PLLAV _{SS} 33	P	-	GND	Analog		GND for PLL
34	XV _{DD} 33	P	-	IO voltage	Digital		Power supply for 27MHz X'tal (3.3V)
35	XTALI	I	F	CMOS	Digital	XV _{DD} 33	27MHz X'tal input
36	XTALO	O	F	CMOS	Digital	XV _{DD} 33	27MHz X'tal output
37	XV _{SS}	P	-	GND	Digital		GND for 27MHz X'tal
38	DV _{DD} 15	P	-	Core voltage	Digital		Power supply for core (1.5V)
39	MODE0	I	D	CMOS	Digital	DV _{DD} 33	Operation mode control
40	DCKI	I	D	CMOS	Digital	DV _{DD} 33	Digital video clock
41	MODE1	I	D	CMOS	Digital	DV _{DD} 33	Operation mode control
42	XMUTE	I	A	CMOS	Digital	DV _{DD} 33	Mute control (active at a low voltage level)
43	INTO	I/O	B	CMOS	Digital	DV _{DD} 33	Interrupt output
44	DDEI	I	D	CMOS	Digital	DV _{DD} 33	Digital video enable/OSD enable
45	DVSI	I	D	CMOS	Digital	DV _{DD} 33	Digital video Vsync/OSD half tone
46	DHSI	I	D	CMOS	Digital	DV _{DD} 33	Digital video Hsync
47	DV _{DD} 33	P	-	IO voltage	Digital		Power supply for IO (3.3V)
48	DCBIN0	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
49	DCBIN1	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
50	DCBIN2	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)

Continued on next page.

LC74900

Continued from preceding page.

Pin No.	Pin symbol	I/O format		Connected to		Digital IO power supply	Remarks
		I/O	Format				
51	DCBIN3	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
52	DCBIN4	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
53	DCBIN5	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
54	DV _{SS}	P		GND	Digital		GND for digital
55	DCBIN6	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
56	DCBIN7	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
57	DYGIN0	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
58	DYGIN1	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
59	DYGIN2	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
60	DYGIN3	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
61	DYGIN4	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
62	DYGIN5	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
63	DYGIN6	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
64	DYGIN7	I	D	CMOS	Digital	DV _{DD} 33	Digital video input/OSD input (pull down if not used)
65	DV _{SS}	P		GND	Digital		GND for digital
66	DROUT0	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (LSB) (input port in test mode)
67	DROUT1	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
68	DROUT2	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
69	DROUT3	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
70	DV _{DD} 33	P		IO voltage	Digital		Power supply for IO (3.3V)
71	DCKO1	O	G	CMOS	Digital	DV _{DD} 33	Panel clock output
72	DV _{SS}	P		GND	Digital		GND for digital
73	DROUT4	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
74	DROUT5	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
75	DROUT6	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (input port in test mode)
76	DROUT7	I/O	B	CMOS	Digital	DV _{DD} 33	Panel R output (MSB) (input port in test mode)
77	DBOUT0	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (LSB) (input port in test mode)
78	DV _{DD} 15	P		Core voltage	Digital		Power supply for core (1.5V)
79	DBOUT1	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
80	DBOUT2	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
81	DBOUT3	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
82	DBOUT4	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
83	DBOUT5	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
84	DV _{DD} 33	P		IO voltage	Digital		Power supply for IO (3.3V)
85	DBOUT6	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (input port in test mode)
86	DBOUT7	I/O	B	CMOS	Digital	DV _{DD} 33	Panel B output (MSB) (input port in test mode)
87	DGOUT0	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (LSB) (input port in test mode)
88	DGOUT1	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
89	DGOUT2	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
90	DGOUT3	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
91	DGOUT4	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
92	DGOUT5	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
93	DGOUT6	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (input port in test mode)
94	DGOUT7	I/O	B	CMOS	Digital	DV _{DD} 33	Panel G output (MSB) (input port in test mode)
95	DHSO	I/O	B	CMOS	Digital	DV _{DD} 33	Panel Hsync/Start pulse for source driver/ Video decoder Vsync output (input port in test mode)
96	DV _{SS}	P		GND	Digital		GND for digital
97	DVSO	I/O	B	CMOS	Digital	DV _{DD} 33	Panel Vsync/Start pulse for gate driver/ Video decoder Vsync output (input port in test mode)
98	DDEO	I/O	B	CMOS	Digital	DV _{DD} 33	Panel enable output (input port in test mode)
99	DEXR	I/O	B	CMOS	Digital	DV _{DD} 33	Invert control signal for DTR/ Video decoder output 1[7](BT.656) (input port in test mode)

Continued on next page.

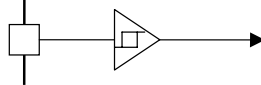
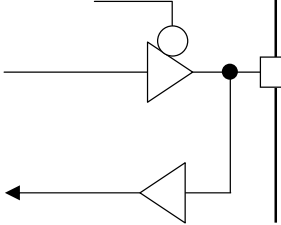
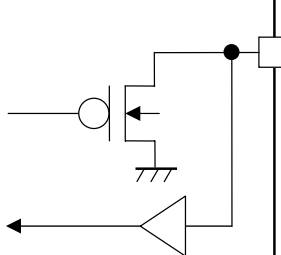
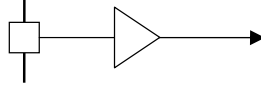

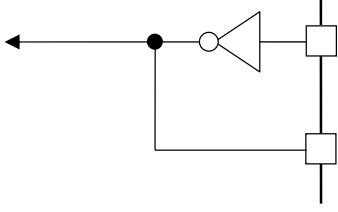
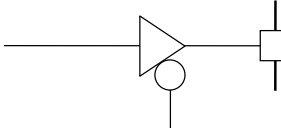
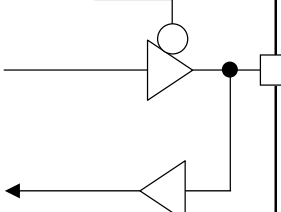
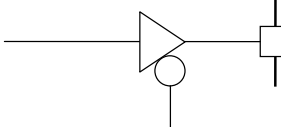
LC74900

Continued from preceding page.

Pin No.	Pin symbol	I/O format		Connected to		Digital IO power supply	Remarks
		I/O	Format				
100	PWM	I/O	B	CMOS	Digital	DV _{DD} 33	Pulse width modulation (input port in test mode)
101	POL	I/O	B	CMOS	Digital	DV _{DD} 33	Polarity control for source driver/ Video decoder output 1[6] (BT.656) (input port in test mode)
102	DV _{DD} 33	P		IO voltage	Digital		Power supply for IO (3.3V)
103	SP	I/O	B	CMOS	Digital	DV _{DD} 33	Start pulse for source driver/ Video decoder output 1[5] (BT.656) (input port in test mode)
104	STRB	I/O	B	CMOS	Digital	DV _{DD} 33	Data stroboscope for source driver/ Video decoder output 1[4] (BT.656) (input port in test mode)
105	CPV	I/O	B	CMOS	Digital	DV _{DD} 33	Clock for gate driver/ Video decoder output 1[3] (BT.656) (input port in test mode)
106	OE	I/O	B	CMOS	Digital	DV _{DD} 33	Output enable for gate driver/ Video decoder output 1[2] (BT.656) (input port in test mode)
107	FLM	I/O	B	CMOS	Digital	DV _{DD} 33	Start pulse for gate driver/ Video decoder output 1[1] (BT.656) (input port in test mode)
108	GRST	I/O	B	CMOS	Digital	DV _{DD} 33	Reset for gate driver/ Video decoder output 1[0] (BT.656) (input port in test mode)
109	DV _{DD} 15	P		Core voltage	Digital		Power supply for core (1.5V)
110	DCRIN0	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[0] (BT.656)
111	DCRIN1	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[1] (BT.656)
112	DCRIN2	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[2] (BT.656)
113	DCRIN3	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[3] (BT.656)
114	DV _{DD} 3318	P	-	IO voltage	Digital		Power supply for IO (3.3V/1.8V)
115	DCKO2	O	J	CMOS	Digital	DV _{DD} 3318	Video decoder clock output
116	DV _{SS}	P	-	GND	Digital		GND for digital
117	DCRIN4	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[4] (BT.656)
118	DCRIN5	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[5] (BT.656)
119	DCRIN6	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[6] (BT.656)
120	DCRIN7	I/O	H	CMOS	Digital	DV _{DD} 3318	Input: Digital video input/OSD input (pull down if not used) Output: Video decoder output 2[7] (BT.656)

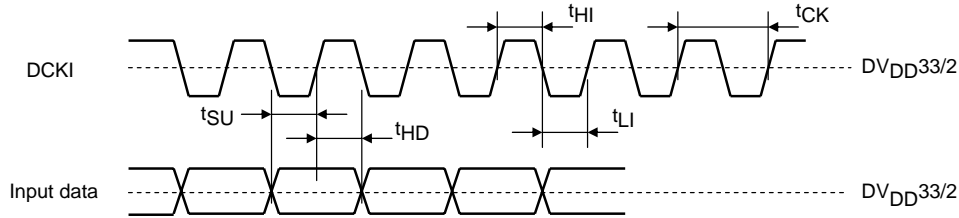
LC74900

Pin Type

I/O type	Function	Equivalent circuit	Applicable pins
A	Schmitt trigger CMOS input		XRST, XPDWN, SCS_I2SEL, XMUTE
B	8mA 3-STATE drive CMOS I/O		GP0, GP1, GP2, STXD, INTO, DROUT0, DROUT1, DROUT2, DROUT3, DROUT4, DROUT5, DROUT6, DROUT7, DBOUT0, DBOUT1, DBOUT2, DBOUT3, DBOUT4, DBOUT5, DBOUT6, DBOUT7, DGOUT0, DGOUT1, DGOUT2, DGOUT3, DGOUT4, DGOUT5, DGOUT6, DGOUT7 DVSO, DHSO, DDEO, DEXR, PWM, POL, SP, STRB, CPV, OE, FLM, GRST
C	8mA OpenDrain output CMOS input*		SCK_SCL, SRXD_SDA
D	CMOS input		SIOSEL, MODE2, MODE3, TEST, MODE0, DCKI, MODE1, DDEI, DVSI, DSI, DCBIN0, DCBIN1, DCBIN2, DCBIN3, DCBIN4, DCBIN5, DCBIN6, DCBIN7, DYGIN0, DYGIN1, DYGIN2, DYGIN3, DYGIN4, DYGIN5, DYGIN6, DYGIN7
E	Analog I/O		REFPKV, VRT, REFNKV, VRB, AIN4, AIN3, AIN2, AIN1, SVO, LPFO
F	Oscillator circuit I/O		XTALI, XTALO
G	12mA 3-STATE drive CMOS output		DCKO1
H	3.3V: 8mA 1.8V: 3mA 3-STATE drive CMOS I/O		DCRIN0, DCRIN1, DCRIN2, DCRIN3, DCRIN4, DCRIN5, DCRIN6, DCRIN7
J	3.3V: 12mA 1.8V: 5mA 3-STATE drive CMOS output		DCKO2

I/O Data Timing

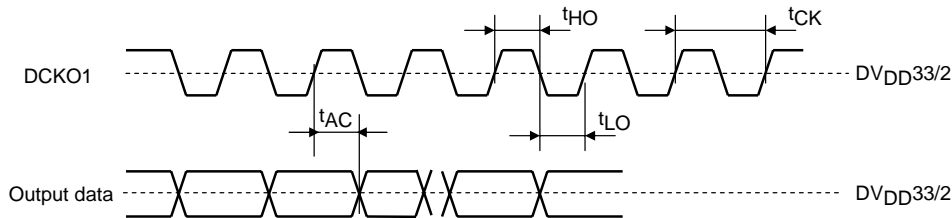
(1) Input data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKI	Clock cycle	t_{CK}	16.7			ns
	Duty			50		%
DCRIN*, DYGIN*, DCBIN*, DVSI, DHSI, DDEI	Input data setup time ($DV_{DD33} = 3.15V$ to $3.45V$) ($DV_{DD3318} = 3.15V$ to $3.45V$)	t_{SU}	3			ns
	Input data hold time ($DV_{DD33} = 3.15V$ to $3.45V$) ($DV_{DD3318} = 3.15V$ to $3.45V$)	t_{HD}	2			ns

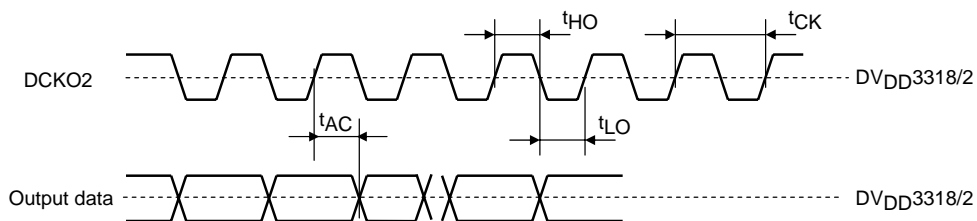
* The recommended duty ratio of input clock is 50%

(2) Output data timing



Pin name	Parameter	Symbol	min	typ	max	unit
DCKO1	Clock cycle	t_{CK}	16.7			ns
	Duty			50		%
DROUT*, DGOUT*, DBOUT*, DVSO, DHSO, DDEO, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST	Output data delay time $DV_{DD33} = 3.15V$ to $3.45V$	t_{AC}	-3		3	ns

* DCKO1 output is not inverted. Output capacitance: 15pF



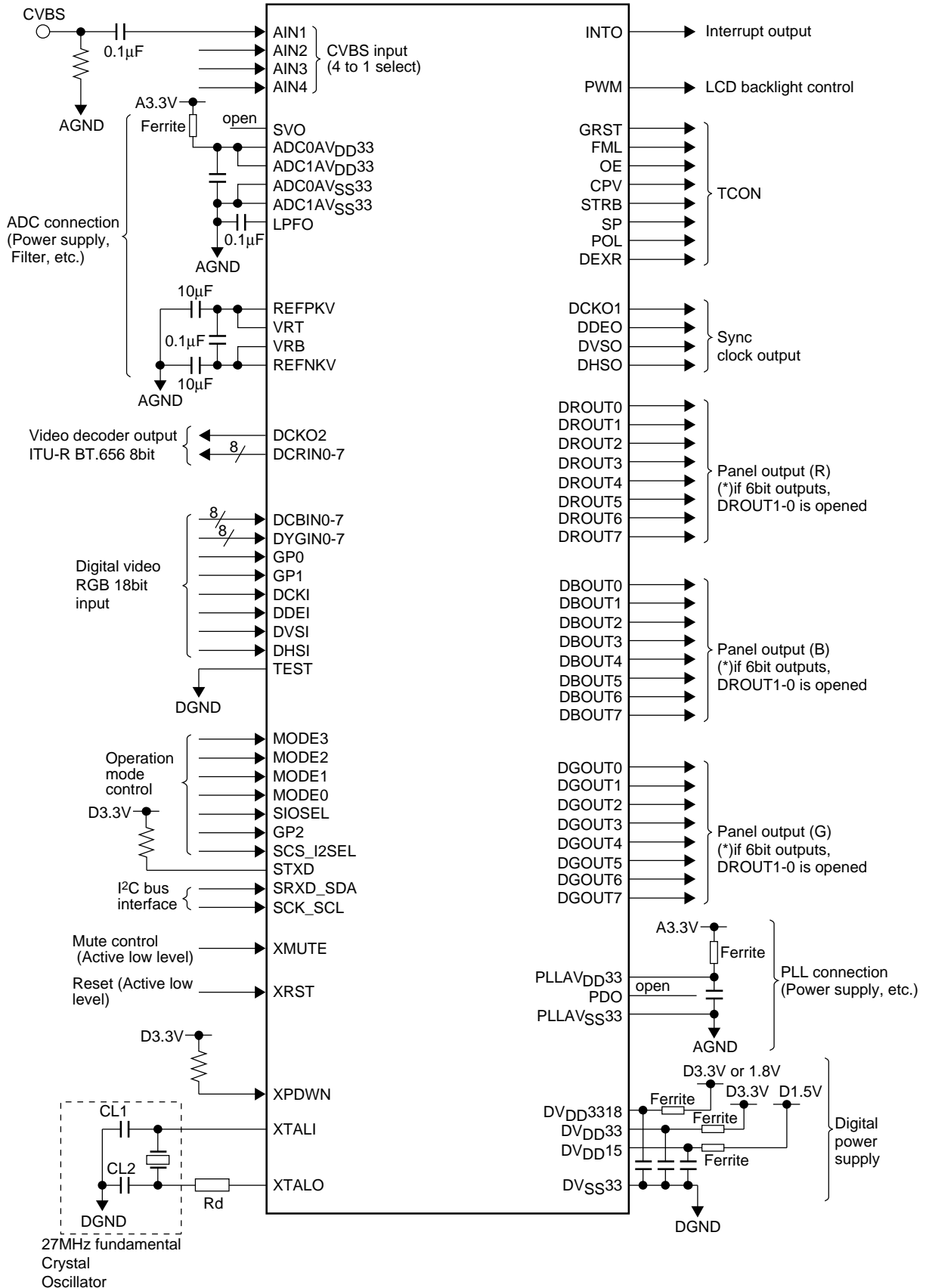
Pin name	Parameter	Symbol	min	typ	max	unit
DCKO2	Clock cycle	t_{CK}	37			ns
	Duty			50		%
DCRIN*, DEXR, POL, SP, STRB, CPV, OE, FLM, GRST, GP0, GP1, DVSO, DHSO	Output data delay time $DV_{DD3318} = 3.15V$ to $3.45V$ $DV_{DD33} = 3.15V$ to $3.45V$	t_{AC}	-3		3	ns
DCRIN*	Output data delay time $DV_{DD3318} = 1.7V$ to $1.9V$	t_{AC}	-6		6	ns

* DCKO1 output is not inverted. Output capacitance: 15pF

LC74900

Connection Example of Parallel Output Mode (Panel/Video Decoder)

* For details, see Application Note.



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of March, 2012. Specifications and information herein are subject to change without notice.