Ordering number : ENA2082

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC786800E — CMOS LSI Compressed Audio signal Processor IC with USB host controller

Overview

The LC786800E integrates ARM7TDMI-S™, USB host processing, SD memory card host processing, Compressed audio encode/decode processing, Audio signal processing, Electronic volume and a flash memory which stores the program for ARM7TDMI-S™ and the various data. The sophisticated programs in the flash memory for the USB host processing or for the SD memory card processing or Electronic Volume control processing, etc. make the load of external main micro controller to be light and are very useful to develop a much features/high performance audio player system with less development burden.

Features

- USB host function (Full speed as 12Mbps), SD memory card host function
- MP3*, WMA*, AAC* decoder processing and normal speed MP3* encoder processing of external input with Sampling rate convertor and High frequency compensation filter
- Various Audio processing functions such as original Surround(AViSS®), seven band Equalizer, etc.

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- Three stereo channels of analog input and four channels of Electronic Volume output (LF, LR, RF, RR)
- ARM7TDMI-S™ as internal CPU core, flash memory for program and various data storage
- Operating voltage: 3.3V typical
- Operating temperature: -40°C to +85°C
- Packages: QIP100 (14 × 20)

Detail of Functions

[Compressed audio functions]

- MP3 decode (ISO/IEC 11172-3, ISO/IEC 13818-3)
  - Sampling rate support: MPEG1-Layer1/2/3 (32kHz, 44.1kHz, 48kHz)
    MPEG2-Layer1/2/3 (16kHz, 22.05kHz, 24kHz)
    MPEG2.5-Layer3 (8kHz, 11.025kHz, 12kHz)
  - Bit rate support: All Bit Rate (Variable Bit Rate support)
  - MPEG header read support
- MP3 encode (ISO/IEC 11172-3)
  - MPEG1-Layer3
  - Sampling rate: 44.1kHz
  - Bit rate: 32kbps to 320kbps (Not support variable bit rate)
- WMA decode (Version 9 standard)
  - Sampling rate support: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: 5kbps to 384kbps (Variable Bit Rate support)
- AAC decode (ISO/IEC 14496-3, ISO/IEC 13818-7)
  - Profile: MPEG4-AAC-LowComplexity
  - Sampling rate support: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: Monaural 8kbps to 160kbps (Variable bit rate support)
    Stereo 16kbps to 320kbps (Variable bit rate support)

[Audio processing functions]

<Audio data processing block>

- SANYO original surround (AViSS)
- 7band graphic equalizer
- Sampling Rate Converter (Fs = 44.1kHz) and High frequency compensation filter for compressed audio playback
- Mute function (-12dB, -∞)and Digital attenuator
- De-emphasis filter

<Audio input processing block>

- Analog Audio data input (Three channels by stereo)
  - Single Ended input: 2 channels
  - Differential input: 1 channel (single end operation is also available)
  - Input Gain: -12.5dB to +18.5dB (1dB step)

  24bit accuracy AD converter (Three input selector)
- Digital Audio data input (Three channels by stereo)

  Four signals connection (384Fs, LRCK, BCK and DATA) is required.
  Corresponding in one of two ways.
  (1) 384Fs input and three lines input synchronized.
  (2) 384Fs output and three lines input synchronized.
  Data Format: IIS, MSB first right justified, etc.

<Audio output processing block>

- Analog Audio data output (One channel by stereo)
  Eight-fold over-sampling digital filter (24bit)
  Secondary LPF for audio output
- Electronic Volume/Fader
  Output channel : Left Front (LF)/Left Rear (LR), Right Front (RF)/Right Rear (RR)
  Output Range : 0dB to -90dB, -∞
  0dB to -32dB : Analog control, 0.25dB step
  -32dB to -70dB : Analog control, 1.0dB step
  -70dB to -90dB : Digital attenuator control
  Decrease the noise at the volume change timing by the digital and analog composite control.
  Individual volume control for LF, LR, RF and RR output is available.
- Digital Audio data output (One channel by stereo)
  Four lines interface, Format: IIS, MSB first right justified, etc.

[External interface functions]

<USB host control block>

- Open Host Controller Interface 1.0a
- Universal Serial Bus Specification 1.1
  Supports up to Full speed (12MHz)for USB2.0
  Only detection at the device insertion is available for Low speed specification.
- Supports four kinds of transfer type (Control/Bulk/Interrupt/Isochronous)
- Two USB ports

<SD memory card host control block>

- Multimedia Card Specification v2.11
- Secure Digital Memory Card Physical Layer Specification v0.96

* Individual contract is necessary to use SD memory card controller. For detail, please contact to us.

[Internal Microcontroller functions]

<Sequencer control>

- USB, SD memory card playback control
  USB/SD files analysis, etc.
- Audio playback control
  Various digital audio filter control, Electronic volume control, etc.

<Communication control between main controller>

- Communication format: SIO

<Peripheral interface block>

- GPIO port 37 ports maximum (Shared with other functions. Several pins are 5V tolerant.)
- External interrupt pins 4 pins maximum (Shared with other functions.)
- Serial interface

SIO	clock synchronized full duplex (3 lines)	3 channels
UART	full duplex	2 channels
IIC	master function	1 channel

<Program memory block>

- Flash memory
  Program version up from the external media (USB/CDROM*) or main controller is available.
  * The update of program from CDROM will only be available if CD system is used with this IC.

<Others>

- Watch Dog Timer
  Notify to outside from the pin or reset internally.
- Power management
  2 kinds of sleep mode
  (1) Only CPU core operates at slow clock and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Useful functions for CD-DSP IC connection usage]

<CD TEXT processing block>

- Buffers CD-TEXT data
- Starts buffering from desired ID3/ID4 of CD-TEXT data.

* Necessary to connect subcode synchronization signals (SBSY and SFSY), shift clock (SBCK) and data (PW).

<CD-ROM processing block>

- Up to quadruple speed operation available
- CD-ROM decoding (Mode1, Mode2<form1, form2>)
- Outputs CD-ROM decoded data

* Necessary to connect three signals (LRCK, BCK and DATA).
  It is possible if desired to connect C2 error flag.

[Others]

<Internal power supply>

- 1.5V regulator for internal blocks

Specifications

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V

Parameter	Symbol	Pin names	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	DV_{DD}, $AV_{DD}1$, $AV_{DD}2$, XV_{DD}, $VV_{DD}2$, $VV_{DD}3$		-0.3 to +3.95	V
Input voltage 1	$V_{IN}1$	Input pins other than $V_{IN}2$		-0.3 to DV_{DD}+0.3	V
Input voltage 2	$V_{IN}2$	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, JTRSTB, JTCK, JTDI, JTMS		-0.3 to +5.6	V
Output voltage	V_{OUT}	All digital output pins and input/output pins		-0.3 to DV_{DD}+0.3	V
Allowable power dissipation	Pd max		Ta ≤ 85°C Mounted reference PCB (*)	519	mW
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-40 to +125	°C

(*)Reference PCB: 114.3mm×76.1mm×1.6mm, glass epoxy resin

Allowable Operating Ranges at Ta = -40 to +85°C, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Supply voltage	$V_{DD}1$	DV_{DD}, $AV_{DD}1$, $AV_{DD}2$, XV_{DD}, $VV_{DD}2$, $VV_{DD}3$		3.00		3.60	V
High-level input voltage	$V_{IH}(1)$	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, JTMS, JTRSTB, JTCK, JTDI	Schmitt	2.00		5.50	V
	$V_{IH}(2)$	GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	Schmitt	2.00		$V_{DD}1$	V
Low-level input voltage	$V_{IL}(1)$	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, JTMS, JTRSTB, JTCK, JTDI	Schmitt	0		0.80	V
	$V_{IL}(2)$	GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53, TEST0, TEST1	Schmitt	0		0.80	V
Oscillator frequency	FX1	XIN XOUT	Oscillator circuit		12.0 or 16.9344		MHz

Electrical Characteristics at Ta = -40 to +85°C, $V_{DD}1$ = 3.0V to 3.6V, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	Unit
Current drain	$I_{DD}1$	DV_{DD}, $AV_{DD}1$, $AV_{DD}2$, XV_{DD}, $VV_{DD}2$, $VV_{DD}3$			85	135	mA
High-level input current	I_{IH}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, JTMS, JTRSTB, JTCK, JTDI	Schmitt, V_{IN} = 5.50V Built-in Pull-down resistor OFF			10.00	µA
	I_{IH}(2)	GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	Schmitt, V_{IN} = $V_{DD}1$ Built-in Pull-down resistor OFF			10.00	µA
Low-level input current	I_{IL}(1)	RESB, SIFCK, SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53, JTMS, JTRSTB, JTCK, JTDI, TEST0, TEST1	Schmitt, V_{IN} = 0V	-10.00			µA
High-level output voltage	V_{OH}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	CMOS, I_{OH} = -2mA	$V_{DD}1$-0.6			V
	V_{OH}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, JTDO, JTRTCK	CMOS, I_{OH} = -4mA	$V_{DD}1$-0.6			V
Low-level output voltage	V_{OL}(1)	GP04, GP05, GP06, GP07, GP12, GP13, GP14, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53	CMOS, I_{OL} = 2mA			0.40	V
	V_{OL}(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, GP10, GP11, JTDO, JTRTCK	CMOS, I_{OL} = 4mA			0.40	V
Built-in Pull down resistor	RPD	SIFDO, SIFCE, BUSYB, GP03, GP04, GP05, GP06, GP07, GP10, GP11, GP12, GP13, GP14, GP30, GP31, GP32, GP33, GP34, GP35, GP36, GP37, GP40, GP41, GP42, GP43, GP44, GP45, GP46, GP47, GP50, GP51, GP52, GP53		50	100	200	kΩ
Output off-leakage current	IOFF(1)	AFILT	Hi-Z Out	-10.00		10.00	µA
	IOFF(2)	SIFDO	Hi-Z Out	-10.00		10.00	µA
Charge pump output current	IAFILH	AFILT			15.0		µA
	IAFILL	AFILT			15.0		µA

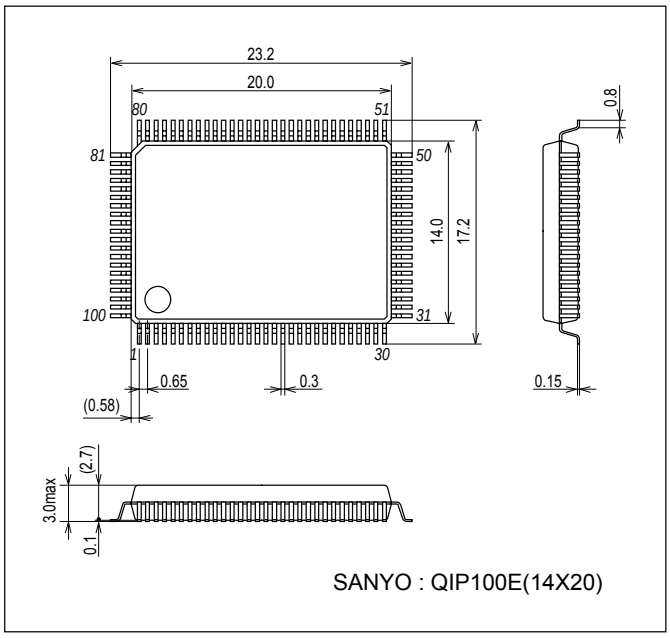
<Note>

- Put a internal pull down resistor or external pull down resistor or external pull up resistor to the SIFDO pin if its output condition is set to 3-State mode.

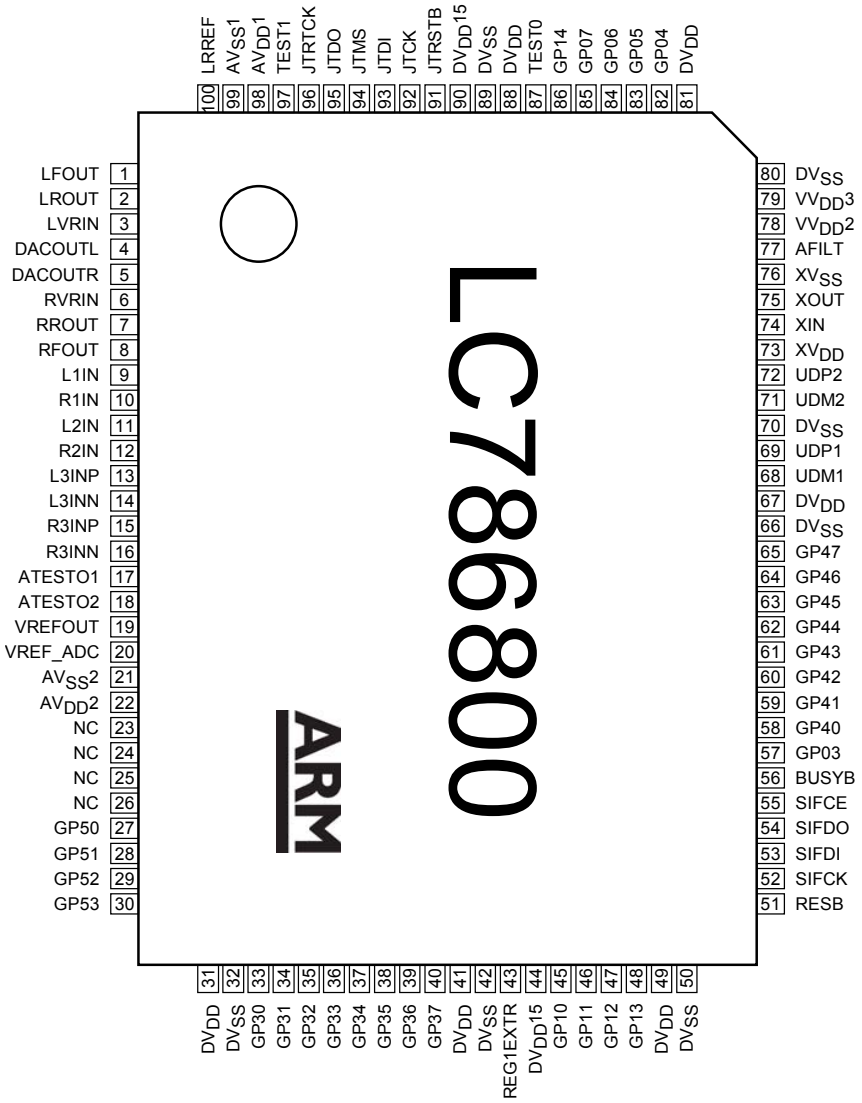
Package Dimensions

unit : mm (typ)

3151A



Pin Assignment



Top view

Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	LFOUT	AO	Undefined	Electronic Volume : Left channel Front output
2	LROUT	AO	Undefined	Electronic Volume : Left channel Rear output
3	LVRIN	AI	Input	Electronic Volume : Left channel volume input
4	DACOUTL	AO	Undefined	Audio DAC : Left channel output
5	DACOUTR	AO	Undefined	Audio DAC : Right channel output
6	RVRIN	AI	Input	Electronic Volume : Right channel volume input
7	RROUT	AO	Undefined	Electronic Volume : Right channel Rear output
8	RFOUT	AO	Undefined	Electronic Volume : Right channel Front output
9	L1IN	AI	Input	Analog stereo Left channel Single Ended input 1
10	R1IN	AI	Input	Analog stereo Right channel Single Ended input 1
11	L2IN	AI	Input	Analog stereo Left channel Single Ended input 2
12	R2IN	AI	Input	Analog stereo Right channel Single Ended input 2
13	L3INP	AI	Input	Analog stereo Left channel Differential input (Positive) / Analog stereo Left channel Single Ended input 3
14	L3INN	AI	Input	Analog stereo Left channel Differential input (Negative)
15	R3INP	AI	Input	Analog stereo Right channel Differential input (Positive) / Analog stereo Right channel Single Ended input 3
16	R3INN	AI	Input	Analog stereo Right channel Differential input (Negative)
17	ATESTO1	AO	Undefined	Analog test output 1. This pin must be left open.
18	ATESTO2	AO	Undefined	Analog test output 2. This pin must be left open.
19	VREFOUT	AO	$AV_{DD}2/2$	Reference voltage output
20	VREF_ADC	AO	$AV_{DD}2/2$	Capacitor connection pin for audio ADC reference voltage
21	$AV_{SS}2$	-	-	Analog system ground. This pin must be connected to the 0V level.
22	$AV_{DD}2$	-	-	Analog system power supply
23	NC	-	-	NC pin. This pin must be left open.
24	NC	-	-	NC pin. This pin must be left open.
25	NC	-	-	NC pin. This pin must be left open.
26	NC	-	-	NC pin. This pin must be left open.
27	GP50	I/O	Input (L)	General purpose I/O port with pull down resistor
28	GP51	I/O	Input (L)	General purpose I/O port with pull down resistor
29	GP52	I/O	Input (L)	General purpose I/O port with pull down resisto
30	GP53	I/O	Input (L)	General purpose I/O port with pull down resistor
31	DV_{DD}	-	-	Digital system power supply
32	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
33	GP30	I/O	Input (L)	General purpose I/O port with pull down resistor
34	GP31	I/O	Input (L)	General purpose I/O port with pull down resistor
35	GP32	I/O	Input (L)	General purpose I/O port with pull down resistor Data 1 input/output for SD memory card
36	GP33	I/O	Input (L)	General purpose I/O port with pull down resistor Data 0 input/output for SD memory card
37	GP34	I/O	Input (L)	General purpose I/O port with pull down resistor Clock output for SD memory card
38	GP35	I/O	Input (L)	General purpose I/O port with pull down resistor Command input/output for SD memory card
39	GP36	I/O	Input (L)	General purpose I/O port with pull down resistor Data 3 input/output for SD memory card
40	GP37	I/O	Input (L)	General purpose I/O port with pull down resistor Data 2 input/output for SD memory card
41	DV_{DD}	-	-	Digital system power supply
42	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
43	REG1EXTR	AO	Undefined	Reserved pin for internal regulator. This pin must be left open.
44	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator

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Pin No.	Pin name	I/O	State when "Reset"	Function
45	GP10	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data transmit
46	GP11	I/O	Input (L)	General purpose I/O port with pull down resistor UART1 data receive
47	GP12	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 1
48	GP13	I/O	Input (L)	General purpose I/O port with pull down resistor Clock control input 2
49	DV_{DD}	-	-	Digital system power supply
50	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
51	RESB	I	-	IC reset input ("L"-active) This pin must be set low once after power is first applied.
52	SIFCK	I	Input	Host-I/F Data transmit clock input for serial communication 1
53	SIFDI	I/O	Input	Host-I/F Data input for serial communication 1
54	SIFDO	I/O	Input	Host-I/F Data output for serial communication 1 (CMOS or 3-State output)
55	SIFCE	I/O	Input	Host -I/F Enable signal input for serial communication 1 ("H"-active)
56	BUSYB	I/O	Input (L)	Host -I/F System busy signal output ("L"-active)
57	GP03	I/O	Input (L)	General purpose I/O port with pull down resistor USB device detection flag output
58	GP40	I/O	Input (L)	General purpose I/O port with pull down resistor
59	GP41	I/O	Input (L)	General purpose I/O port with pull down resistor
60	GP42	I/O	Input (L)	General purpose I/O port with pull down resistor
61	GP43	I/O	Input (L)	General purpose I/O port with pull down resistor
62	GP44	I/O	Input (L)	General purpose I/O port with pull down resistor
63	GP45	I/O	Input (L)	General purpose I/O port with pull down resistor
64	GP46	I/O	Input (L)	General purpose I/O port with pull down resistor
65	GP47	I/O	Input (L)	General purpose I/O port with pull down resistor
66	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
67	DV_{DD}	-	-	Digital system power supply
68	UDM1	I/O	-	USB data input/output 1 D- signal connection General purpose I/O port (GP22)
69	UDP1	I/O	-	USB data input/output 1 D+ signal connection General purpose I/O port (GP23)
70	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
71	UDM2	I/O	-	USB data input/output 2 D- signal connection General purpose I/O port (GP20)
72	UDP2	I/O	-	USB data input/output 2 D+ signal connection General purpose I/O port (GP21)
73	XV_{DD}	-	-	Oscillator power supply
74	XIN	I	Oscillation	X'tal oscillator connection
75	XOUT	O	Oscillation	X'tal oscillator connection
76	XV_{SS}	-	-	Oscillator ground. This pin must be connected to the 0V level.
77	AFILT	AO	Undefined	PLL2 charge pump output (for filter connection)
78	$VV_{DD}2$	-	-	PLL2 power supply
79	$VV_{DD}3$	-	-	PLL1 power supply
80	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
81	DV_{DD}	-	-	Digital system power supply
82	GP04	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) clock output
83	GP05	I/O	Input (L)	General purpose I/O port with pull down resistor IIC (master) data input/output

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Pin No.	Pin name	I/O	State when "Reset"	Function
84	GP06	I/O	Input (L)	General purpose I/O port with pull down resistor
85	GP07	I/O	Input (L)	General purpose I/O port with pull down resistor
86	GP14	I/O	Input (L)	General purpose I/O port with pull down resistor
87	TEST0	I	Input	Test input. This pin must be connected to the 0V level.
88	DV_{DD}	-	-	Digital system power supply
89	DV_{SS}	-	-	Digital system ground. This pin must be connected to the 0V level.
90	$DV_{DD}15$	AO	High	Capacitor connection pin for internal regulator
91	JTRSTB	I	Input	JTAG reset input (Connect to pull-down resistor or 0V level in normal mode.)
92	JTCK	I	Input	JTAG clock input (Connect to pull-down resistor or 0V level in normal mode.)
93	JTDI	I	Input	JTAG data input (Connect to pull-down resistor or 0V level in normal mode.)
94	JTMS	I	Input	JTAG mode input (Connect to pull-down resistor or DV_{DD} level in normal mode.)
95	JTDO	O	Low	JTAG data output (Leave open in normal mode.)
96	JTRTCK	O	Low	JTAG return clock output (Leave open in normal mode.)
97	TEST1	I	Input	Test input. This pin must be connected to the 0V level.
98	$AV_{DD}1$	-	-	Analog system power supply
99	$AV_{SS}1$	-	-	Analog system ground. This pin must be connected to the 0V level.
100	LRREF	AO	$AV_{DD}1/2$	Capacitor connection pin for reference voltage for Audio DAC and Electronic Volume.

<Note>

(1) For unused pins:

- The unused input pins must be connected to the GND (0V) level if there is no individual note in the above table.
- The unused output pins must be left open (No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND (0V) or power supply pin for I/O block with internal pull down resistor OFF or be left open with internal pull down resistor ON when input pin mode or must be left open (No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin with internal pull-down resistor OFF at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

(2) For power supply pins:

- Same voltage level must be supplied to DV_{DD}, $AV_{DD}1$, $AV_{DD}2$, XV_{DD}, $VV_{DD}2$ and $VV_{DD}3$ power supply pins.
  (Refer to“Allowable operating ranges”.)

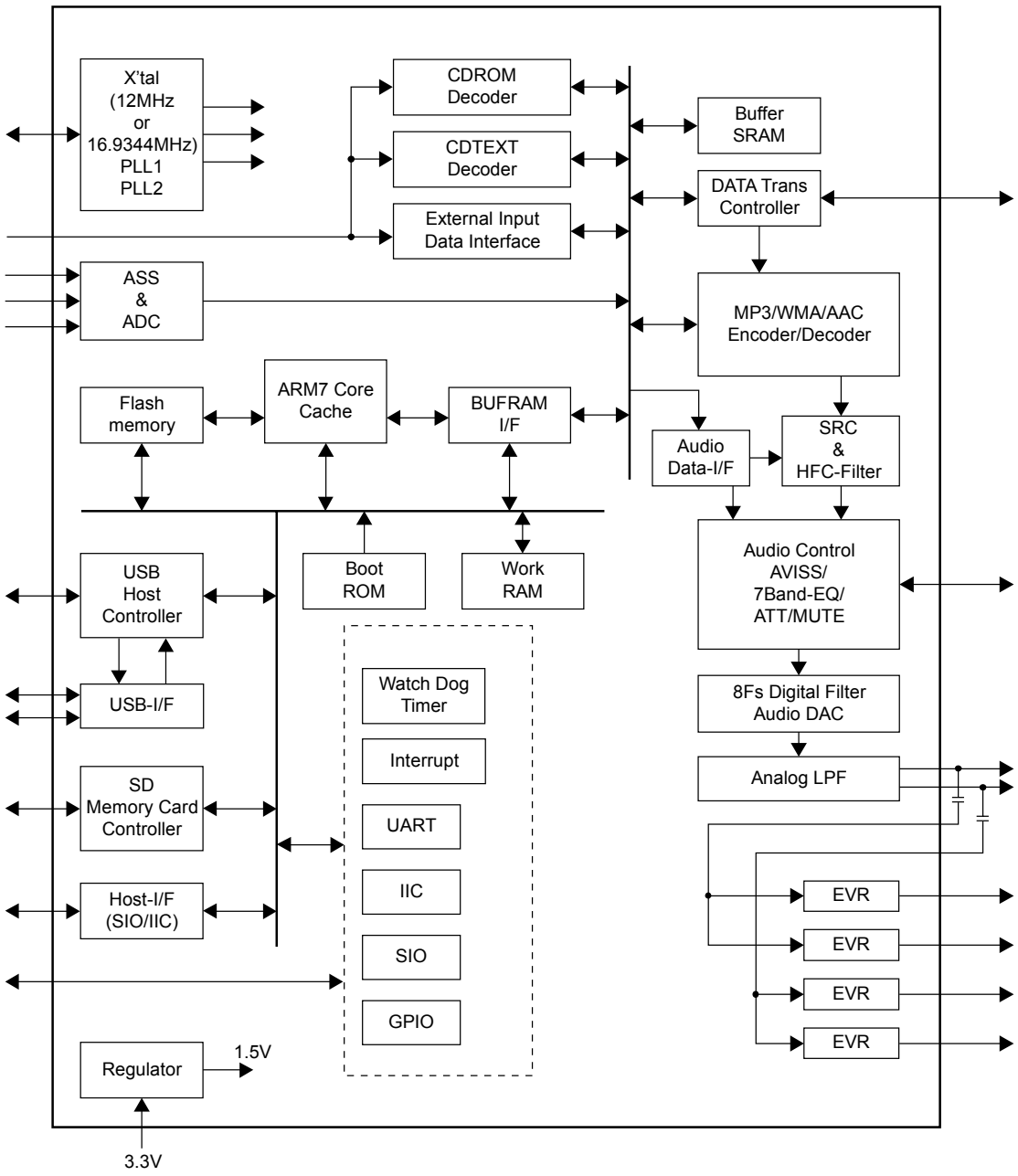
(3) For “Reset” condition:

- This IC is not reset only by making the RESB pin “Low”.
  Refer to “Power on and Reset control” for detail of “Reset” condition.

(4) For “Analog Source” unused pins (9 pin to 16 pin):

- The “Analog Source” unused pins (9 pin to 16 pin) must be connected to the GND (0V) level through the input coupling capacitor.

Block Diagram



Power on and Reset control

- Attention when power on

(1) Reset Control

The RESB pin must be set to “Low” level to initialize the operating state of internal flash memory.
If the power is switched on when the RESB pin is “High” level, this IC may operate incorrectly because the internal flash memory is not initialized. In this case, this IC is not initialized even if a low level supplied to RESB pin. Therefore, the RESB pin must be set to “Low” level when power is first supplied.

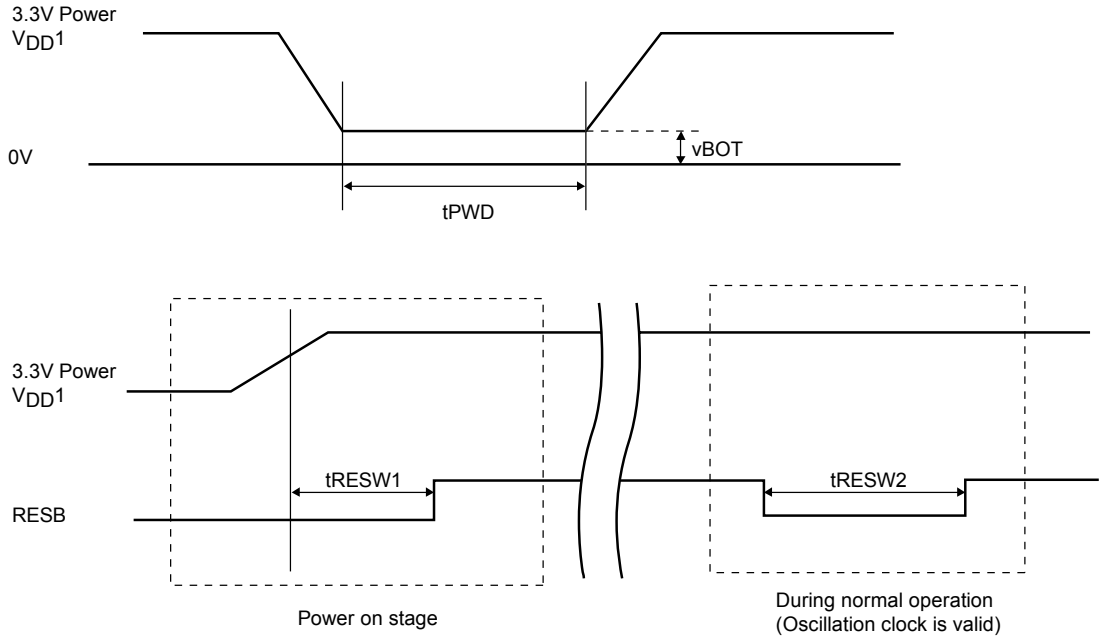
(2) Electronic Volume output

Because the output state of Electronic Volume pins is undefined when the power voltage is first supplied, it is necessary to mute the Electronic Volume output signals externally.

(3) Input voltage for Input pins

You may input the voltage of 3.6V or less to each input terminal when the power supply is off. However, it is necessary to supply a regulated voltage to the power supply beforehand when more than 3.6V voltage is input to the 5V tolerant input pins.

Power ON/Power Down/Reset timing



Parameter	Symbol	min	typ	max	unit
Power down time	tPWD	10			ms
Power down voltage	vBOT	0		0.2	V
Reset time (Power on)	tRESW1	20			ms
Reset time (Normal) (*1)	tRESW2	1			ms

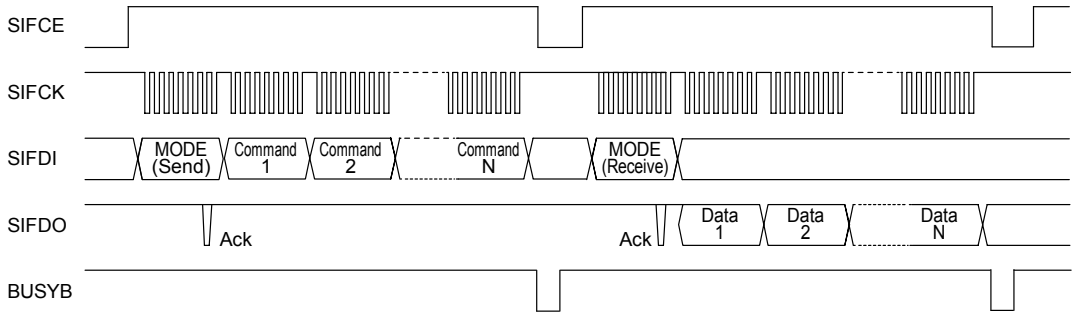
*1: The x'tal oscillation must be stable during tRESW2.
When the x'tal clock has been stopped by the command etc., the specification of tRESW2 could be longer than the value shown above, because it takes time that the x'tal oscillator becomes stable.

Host interface

The data transmission between this IC and Host controller is performed with SPI type synchronous SIO protocol. The transmission procedure is as follows.

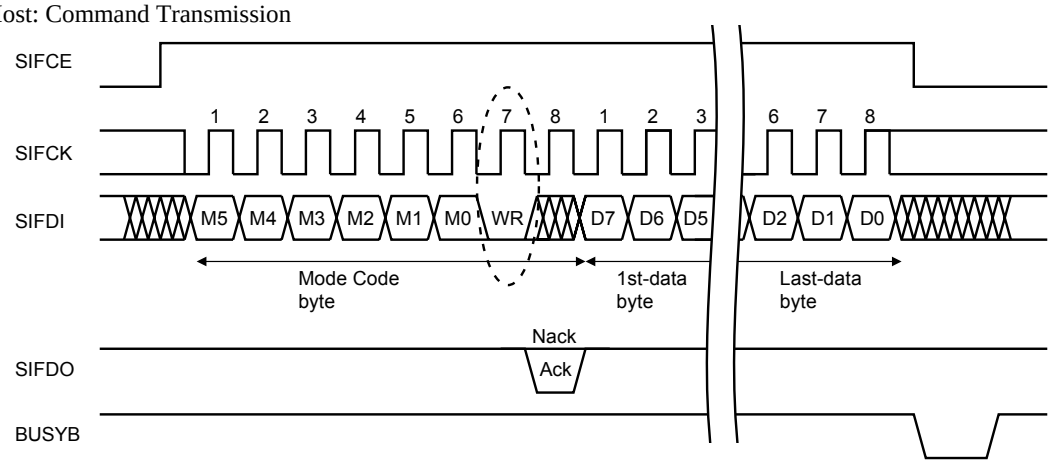
- Refer to the internal software specification of this IC about M5 to M0 code in Mode code transmission.
  When the input data of M5 to M0 coincide to the data in the internal register, the SIFDO pin becomes to “Low” level (Ack) then the transmission is enabled.
  When not coincide, the SIFDO pin keeps “High” level (Nack) then the transmission is not enabled.
- The seventh data in Mode code transmission shows whether the following procedure is the Command transmission or the Data reception. When the seventh data is “Low”, the following procedure is Command transmission. When the seventh data is “High”, the following procedure is Data reception.
- Attention because the specifications of transmission timings are different depending on the internal CPU’s operating speed modes (Low speed or Normal speed). Refer to the table in next page.

Communication Interface format between Host controller

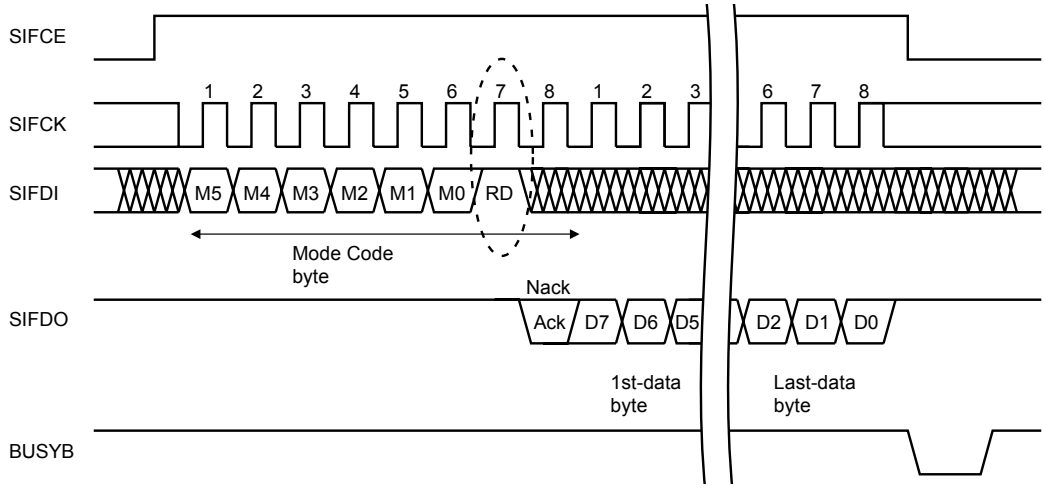


Transmission/Reception format between Host controller

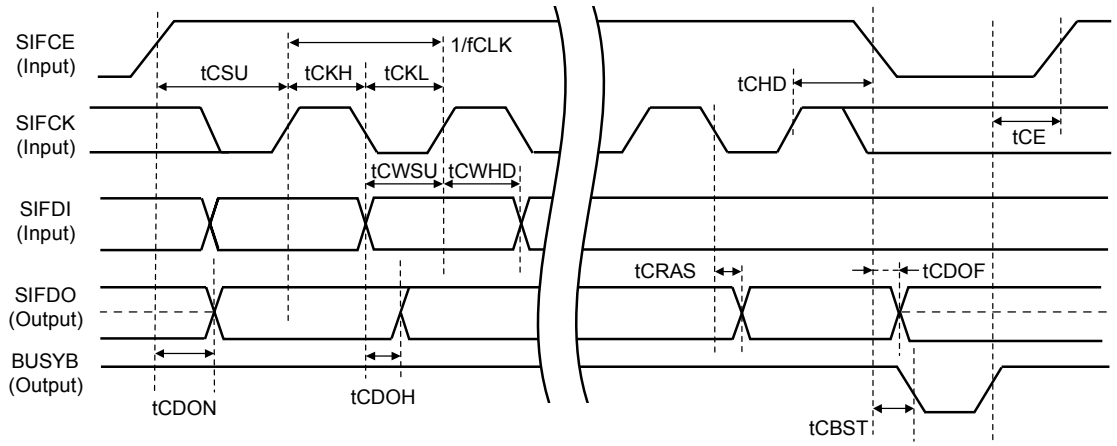
(1) Host: Command Transmission



(2) Host: Data Reception



Communication Timing specification between Host controller



Parameter	Symbol	Pin names	min	typ	max	unit
SIFCK clock frequency	fCLK	SIFCK			3.3 0.725	MHz
SIFCK clock "H" level width	tCKH	SIFCK	150 690			ns
SIFCK clock "L" level width	tCKL	SIFCK	150 690			ns
Transfer start enable time	tCE	BUSYB, SIFCE	0 0			ns
Setup time for transfer start	tCSU	SIFCE, SIFCK	100 200			ns
Hold time for transfer end	tCHD	SIFCE, SIFCK	100 200			ns
Setup time for SIFDI	tCWSU	SIFDI, SIFCK	75 75			ns
Hold time for SIFDI	tCWHD	SIFDI, SIFCK	75 200			ns
Output delay time for SIFDO “H”	tCDOH	SIFDO, SIFCK			100 350	ns
Output delay time for SIFDO	tCRAS	SIFDO, SIFCK			100 350	ns
Turn on time for SIFDO *1	tCDON	SIFDO, SIFCE			100 100	ns
Turn off time for SIFDO *1	tCDOF	SIFDO, SIFCE			150 150	ns
BUSYB "L" level output delay time	tCBST	BUSYB			150 350	ns

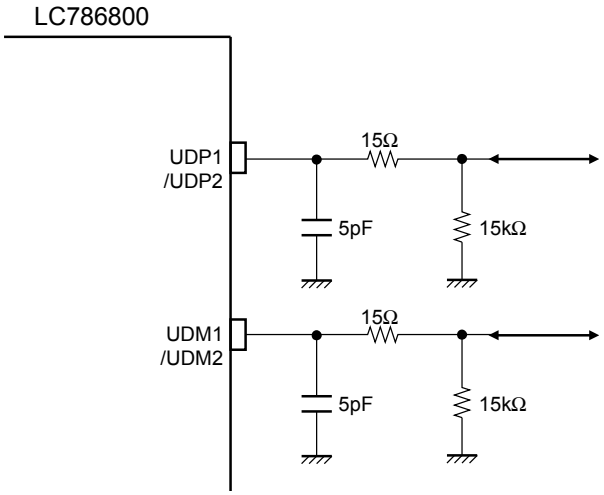
Internal CPU operating speed mode Upper step : Normal speed
Lower step : Low speed

*1: The tCDON and tCDOF specifications are for when the SIFDO pin is set to the 3-State mode.

USB Specification at Ta = -40°C to +85°C, $V_{DD}1$ = 3.0V to 3.6V, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
High-level input voltage	V_{IH} (USB)	UDM1, UDP1, UDM2, UDP2		2.0			V
Low-level input voltage	V_{IL} (USB)					0.8	
Input leakage current	ILI		Output driver: OFF	-10.0		10.0	µA
Differential input sensitivity	VDI		|(UDP) - (UDM)|	0.2			V
Common mode voltage range	VCM		Includes VDI range	0.8		2.5	V
High-level output voltage	V_{OH} (USB)		Connect 15kΩ ±5% pull-down resistor to GND (0V).	2.8		3.6	V
Low-level output voltage	V_{OL} (USB)		Connect 1.5kΩ ±5% pull-up resistor to $V_{DD}1$.	0		0.3	V
Crossover voltage	VCR			1.3		2.0	V
USB data rising time	TUR		CL = 50pF	4.0		20.0	ns
USB data falling time	TUF			4.0		20.0	

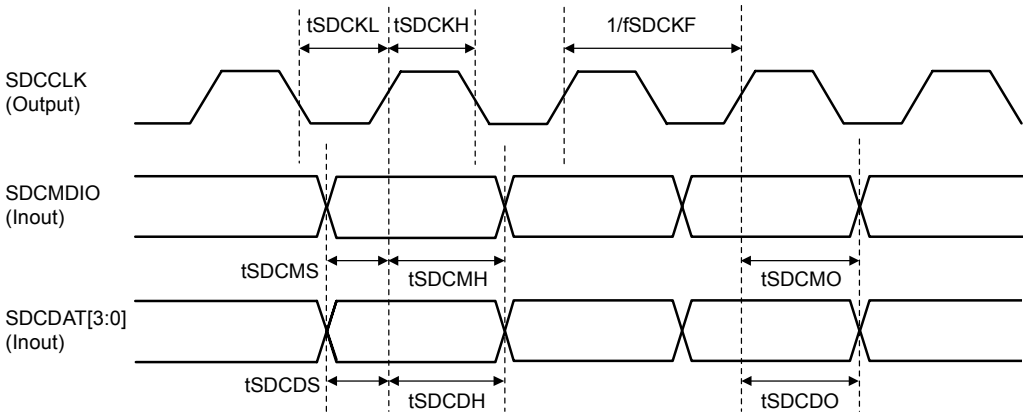
Example circuit for USB application



* The value of resistors and capacitors in this circuit might be needed to be adjusted for each application.

SD Memory Card Interface

SD Memory Card Input/Output Timing specification



* Relationship between signal name and pin name

SDCCLK : GP34 SDCMDIO : GP35 SDCDAT [3] : GP36
SDCDAT [2] : GP37 SDCDAT [1] : GP32 SDCDAT [0] : GP33

Parameter	Symbol	Pin names	min	typ	max	unit
SDCCLK clock frequency	fSDCKF	SDCCLK		6.0		MHz
SDCCLK clock "H" level width	tSDCKH	SDCCLK		83.3		ns
SDCCLK clock "L" level width	tSDCKL	SDCCLK		83.3		ns
Setup time for command input	tSDCMS	SDCMDIO, SDCCLK	30.0			ns
Hold time for command input	tSDCMH	SDCMDIO, SDCCLK	30.0			ns
Command output valid time	tSDCMO	SDCMDIO, SDCCLK			30.0	ns
Setup time for data input	tSDCDS	SDCDAT [3:0], SDCCLK	30.0			ns
Hold time for data input	tSDCDH	SDCDAT [3:0], SDCCLK	30.0			ns
Data output valid time	tSDCDO	SDCDAT [3:0], SDCCLK			30.0	ns

Note: Internal CPU (ARM7) must be set to normal mode. Never use the SD Memory Card interface at the internal CPU's Low speed mode.

Audio Data Input/Output Function

AC Electrical Characteristics at Ta = 25°C, $V_{DD}1$ = 3.3V, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V,
Fs=44.1kHz, Audio Signal Frequency: 1kHz, Measurement Range: 10Hz to 20kHz

Parameter	Symbol	Pin names	Conditions	min	typ	max	unit
(Input selector+ADC)							
Full scale analog input level		L1IN, R1IN, L2IN, R2IN, L3INP, L3INN, R3INP, R3INN		2.605	2.805 ($0.85 \times V_{DD}1$)	3.005	Vp-p
Input impedance				20	30		kΩ
Gain setting level				-12		19	dB
Gain setting step					1		dB
Gain setting step error				-0.5		0.5	dB
Signal to noise ratio	S/N		0dB Data, 20kHz-LPF, A-filter	90	95		dB
Dynamic range	DR		-60dB Data, 20kHz-LPF, A-filter	90	95		dB
Total harmonic distortion	THD+N		Input condition : -3dBFS		-85	-80	dB
Cross talk1	CT1		Between Channels		-100	-85	dB
Cross talk2	CT2		Between Sources		-100	-85	dB
(ADC digital filter)							
Passband frequency			±0.04dB	0		0.4535	Fs
Stopband frequency				0.5465			Fs
Passband ripple						±0.04	dB
Stopband attenuation			>24.1kHz	-69			dB
HPF cut off Frequency for DC offset cancelation					0.00002		Fs
(Audio DAC)							
Full scale analog output level		DACOUTL, DACOUTR		2.605	2.805 ($0.85 \times V_{DD}1$)	3.005	Vp-p
Signal to noise ratio	S/N		0dB Data, 20kHz-LPF, A-filter	95	98		dB
Dynamic range	DR		-60dB Data, 20kHz-LPF, A-filter	94	98		dB
Total harmonic distortion	THD+N		0dB Data, 20kHz-LPF		-85	-80	dB
Cross talk	CT		0dB Data, 20kHz-LPF		-100	-85	dB
(DAC digital filter)							
Passband frequency			±0.015dB	0		0.4535	Fs
Stopband frequency				0.5465			Fs
Passband ripple						±0.015	dB
Stopband attenuation				-62			dB
HPF cut off frequency for DC offset cancelation			-3dB		0.0000385		Fs
(Electronic volume)							
Input impedance		LVRIN,RVRIN		7.5	10		kΩ
Volume setting range		LFOUT, LROUT, RFOUT, RROUT		-70		0	dB
Mute level				80	90		dB
Volume setting step			0dB to -32dB		0.25		dB
			-32dB to -70dB		1.0		dB
Volume setting step error			0 dB to -32dB	-0.125		0.125	dB
			-32 dB to -70dB	-0.5		0.5	dB

Digital Audio Data Interface

• Digital Audio Interface Format

	Mode	Data Length	Slot Length	Fs384 clock
Input	IIS MSB first right justified MSB first left justified	16bit 24bit	32fs, 48fs, 64fs	Internal clock External input clock
Output	IIS MSB first right justified MSB first left justified	16bit 24bit	32fs, 48fs, 64fs	Output internal 384fs clock

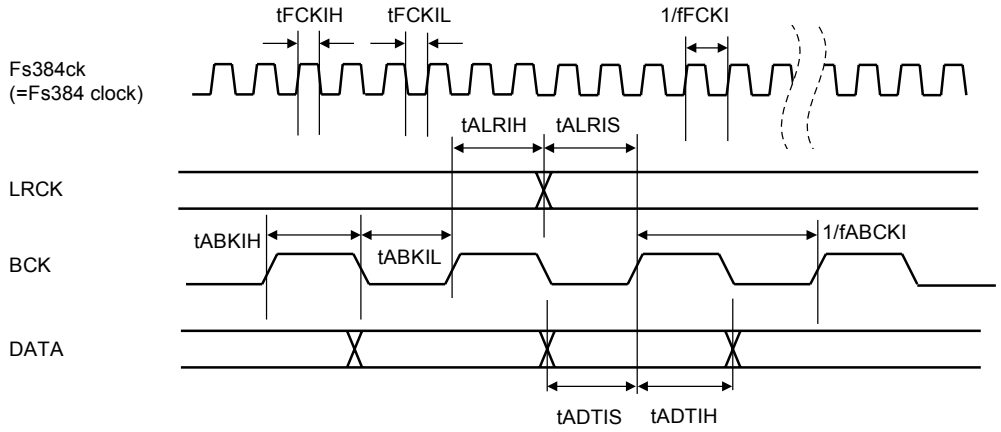
• Used pins

	LRCK	BCK	DATA	Fs384 clock	De-emphasis
Input	GP30 GP40 GP52	GP31 GP41 GP51	GP32 GP42 GP50	GP33 GP43 GP53	GP14, GP46
Output	GP30 GP40 GP52	GP31 GP41 GP51	GP32 GP42 GP50	GP33 GP43 GP53	-

Note : There is a priority level about Digital Audio input setting for the pins from GP30 to GP33 and the pins from GP40 to GP43 and the pins from GP50 to GP53. The priority level is as follows.
(1) GP30 to GP33 > (2) GP40 to GP43 > (3) GP50 to GP53
Only the setting for the pins from GP30 to GP33 will become effective even if all the pins above are set to be the Digital Audio input pins at the same time. Set the Digital Audio input pins only to either of the pins from GP30 to GP33 or the pins from GP40 to GP43 or the pins from GP50 to GP53 if necessary.

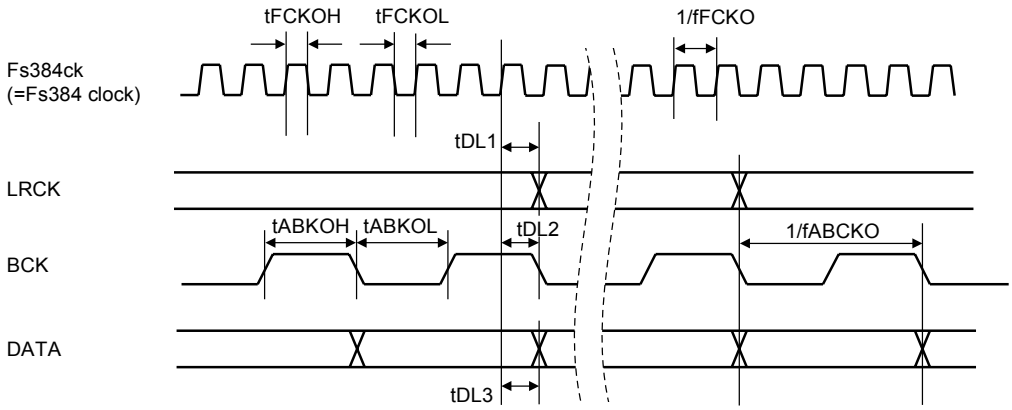
• Others
- Audio output can support 3 types of Fs (32kHz/44.1kHz/48kHz) when 12MHz is used to the oscillator. When 16.9344MHz is used to the oscillator, only Fs=44.1kHz is supported.
- During external audio input, emphasis signal is input from GP14/GP46.

Digital Audio Data Input timing



Parameter	Symbol	Pin Names	min	typ	max	unit
Fs384 clock frequency	fFCKI	Fs384ck			20.0	MHz
Fs384 clock "H" level width	tFCKIH	Fs384ck	20			ns
Fs384 clock "L" level width	tFCKIL	Fs384ck	20			ns
Bit clock frequency	fABCKI	BCK			3.3	MHz
Bit clock "H" level width	tABKIH	BCK	120			ns
Bit clock "L" level width	tABKIL	BCK	120			ns
Setup time for LRCK input	tALRIS	LRCK, BCK	30			ns
Hold time for LRCK input	tALRIH	LRCK, BCK	30			ns
Setup time for DATA input	tADTIS	DATA, BCK	30			ns
Hold time for DATA input	tADTIH	DATA, BCK	30			ns

Digital Audio Data Output timing



Parameter	Symbol	Pin Names	min	typ	max	unit
Fs384 clock frequency	fFCKO	Fs384ck		16.9344 *1		MHz
Fs384 clock "H" level width	tFCKOH	Fs384ck		29.5 *1		ns
Fs384 clock "L" level width	tFCKOL	Fs384ck		29.5 *1		ns
Bit clock frequency	fABCKO	BCK		2.1168 *1		MHz
Bit clock "H" level width	tABKOH	BCK		236.2 *1		ns
Bit clock "L" level width	tABKOL	BCK		236.2 *1		ns
LRCK output delay time	tDL1	LRCK, Fs384ck	0		50	ns
BCK output delay time	tDL2	BCK, Fs384ck	0		50	ns
DATA output delay time	tDL3	DATA, Fs384ck	0		50	ns

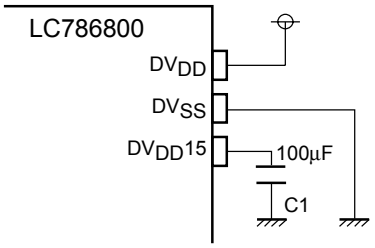
*1: In case of setting the 48-slot length for output format as Fs = 44.1kHz.

Internal Voltage Regulator at Ta = -40°C to +85°C, DV_{SS} = $AV_{SS}1$ = $AV_{SS}2$ = XV_{SS} = 0V

Parameter	Symbol	Condition	min	typ	max	unit
Output voltage	$DV_{DD}15$	$V_{DD}1$ = 3.0V to 3.6V	1.35	1.50	1.65	V
Load current	Iope	$V_{DD}1$ = 3.3V			200	mA

Note : The specification of “load current” above is sum of the load current of two internal voltage regulator.

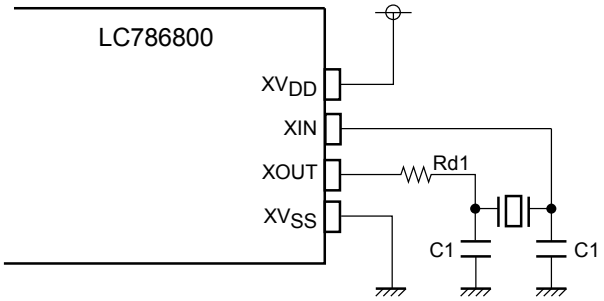
Example circuit for Regulator



* Same circuit need to be mounted both for two regulator pins. (No.44 and No.90)
* The capacitor C1 must be greater than 50µF and low Secure 50µF or more for low ESR and the capacity value in the range of the operating temperature so that there is a possibility of the oscillation when the capacity value changes by the temperature change etc.
  (The recommended value is 100µF.)

Oscillator

Example circuit for Oscillator



(1) XIN/XOUT: 12.0000MHz or 16.9344MHz
- For System Main clock and USB control
- Recommended Oscillator

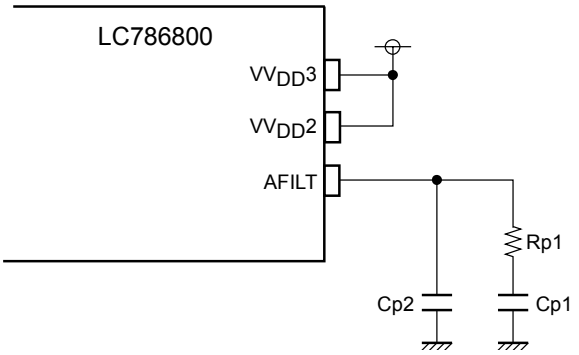
  Nihon Dempa Kogyo Co., Ltd.

Type	Oscillation frequency	Recommended value
NX5032GA	12MHz	Rd1 = 0Ω, C1 = 4pF
NX8045GB	12MHz	Rd1 = 0Ω, C1 = 4pF
AT51-CD2	16.9344MHz	Rd2 = 0Ω, C2 = 8pF

<Notes>
- Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
- The precision of oscillator used in XIN/XOUT should meet the USB standard.
- If oscillation clock is disturbed by noise or by the other factors, it may lead to operation failure. Hence, make sure to connect resistor and capacitor for oscillation circuit as close as XIN/XOUT and the wire should be as short as possible. Also you need to select parts with caution so as to obtain stable external constant value within the guaranteed operating temperature range because the variation of external constant due to temperature change could affect the oscillation precision.
- Concerning about internal circuit for XIN/XOUT, refer to the “Analog Pin Internal Equivalent Circuits” section.

PLL circuit

Example of PLL circuit



- PLL

  LC786800 includes PLL1 and PLL2.

  The functions of PLL1/ PLL2 varies depends on the oscillator connected to XIN/XOUT.

	PLL1	PLL2
When 12MHz oscillator is used	For system clock generation	For audio clock generation
When 16.9344MHz oscillator is used	Unused	For system clock generation

- External filter constant for PLL2

	PLL2 constant
When 12MHz oscillator is used	Rp1 = 4.7kΩ/Cp1 = 3300pF/Cp2 = 220pF
When 16.9344MHz oscillator is used	Rp1 = 4.7kΩ/Cp1 = 0.033μF/Cp2 = 2200pF

<Caution>

- This PLL filter circuit is for resistor (Rp1), capacitance (Cp1, Cp2), audio generation/ system clock generation connected to AFILT. If oscillation clock is disturbed by noise or by the other factors, it may lead to operation failure. Hence, make sure to connect resistor and capacitor that constitute filter circuit as close as AFILT and the wire should be as short as possible. Also if filter constant changes due to temperature change, oscillation of PLL may become unstable and the following problem may occur.

  (1) 12MHz oscillator

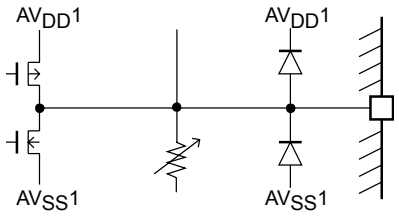
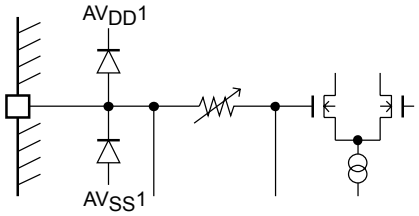
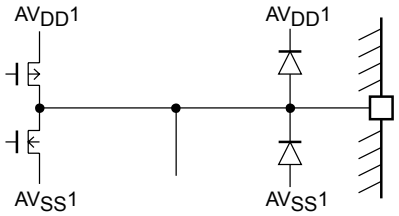
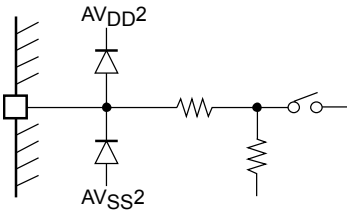
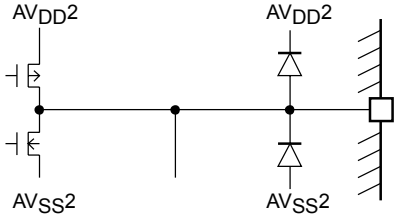
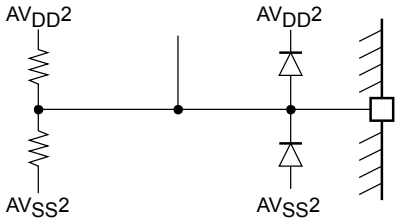
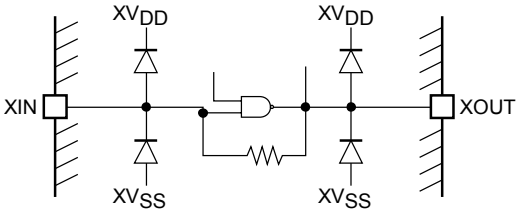
  Due to unstable audio playback clock, audio playback is affected with unstable audio signal input (ADC operation) and output (various filter, DAC operation).

  (2) 16.9344MHz oscillator

  As the internal system clock used in built-in CPU and USB becomes unstable, the LSI operation is affected as well.

  Hence, you need to select parts with caution so as to obtain stable filter constant value within the guaranteed operating temperature range.
- See the section on “Analog Pin Internal Equivalent Circuits” for the internal configuration of AFILT.

Analog Pin Internal Equivalent Circuits

Pin Name (Pin No.)	Equivalent circuit
LFOUT (1) LROUT (2) RROUT (7) RFOUT (8)	
LVRIN (3) RVRIN (6)	
DACOUTL (4) DACOUTR (5)	
L1IN (9) R1IN (10) L2IN (11) R2IN (12) L3INP (13) L3INN (14) R3INP (15) R3INN (16)	
VREFOUT (19)	
VREF_ADC (20)	
XIN (74) XOUT (75)	

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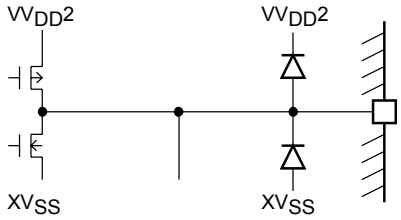
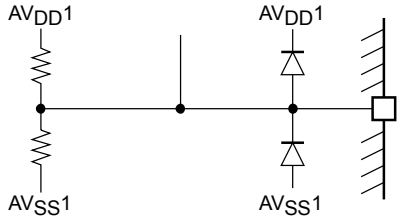
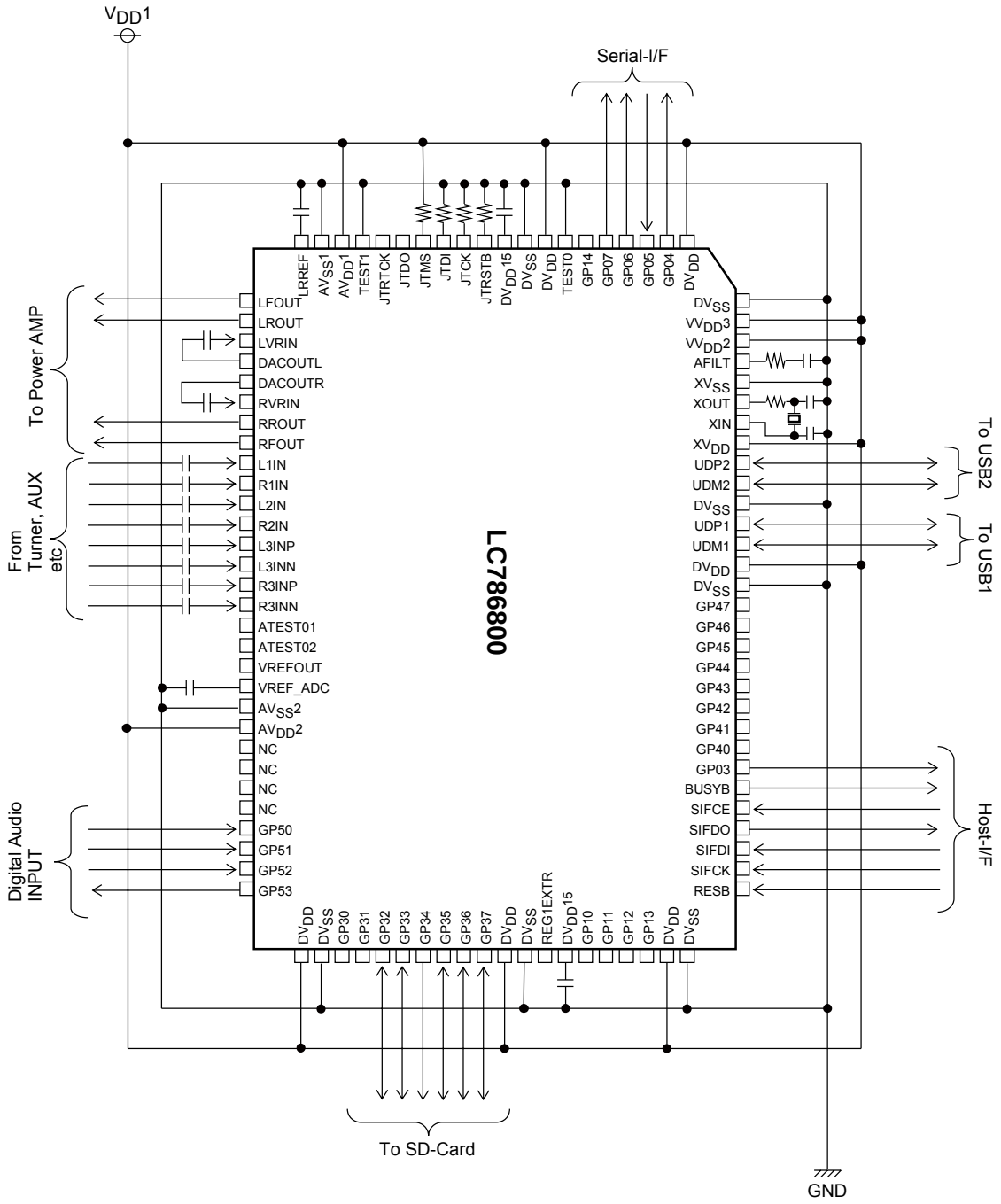
Pin Name (Pin No.)	Equivalent circuit
AFILT (77)	
LRREF (100)	

Sample Application Circuit



- Take care to the input voltage level of the analog audio input.
- Concerning to the application circuit for USB, Regulator and Oscillator, refer to the page 16 and 21 respectively.

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