# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

## DESCRIPTION

The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "fold-back" inverting buffer and control gate $F_C$. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Any of the 32 AND gates can drive bidirectional I/O lines (B), whose output polarity is individually programmable through a set of Ex-OR gates for implementing AND-OR or AND-NOR logic functions. Similarly, any of the 32 AND gates can drive the J-K inputs of all flip-flops. There are 4 AND gates for the Asynchronous Preset/Reset functions.

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

## FEATURES

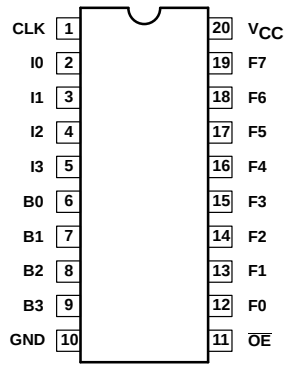
- High-speed version of PLS159
- $f_{MAX}$ = 18MHz
  - 25MHz clock rate
- Field-Programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops ($F_n$ = 1)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge-triggered clock
- Input loading: –100µA (max.)
- Power dissipation: 750mW (typ.)
- TTL compatible
- 3-State outputs

## APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

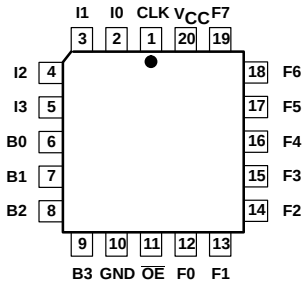
## PIN CONFIGURATIONS

**N Package**




N = Plastic Dual In-Line Package (300mil-wide)

**A Package**




A = Plastic Leaded Chip Carrier

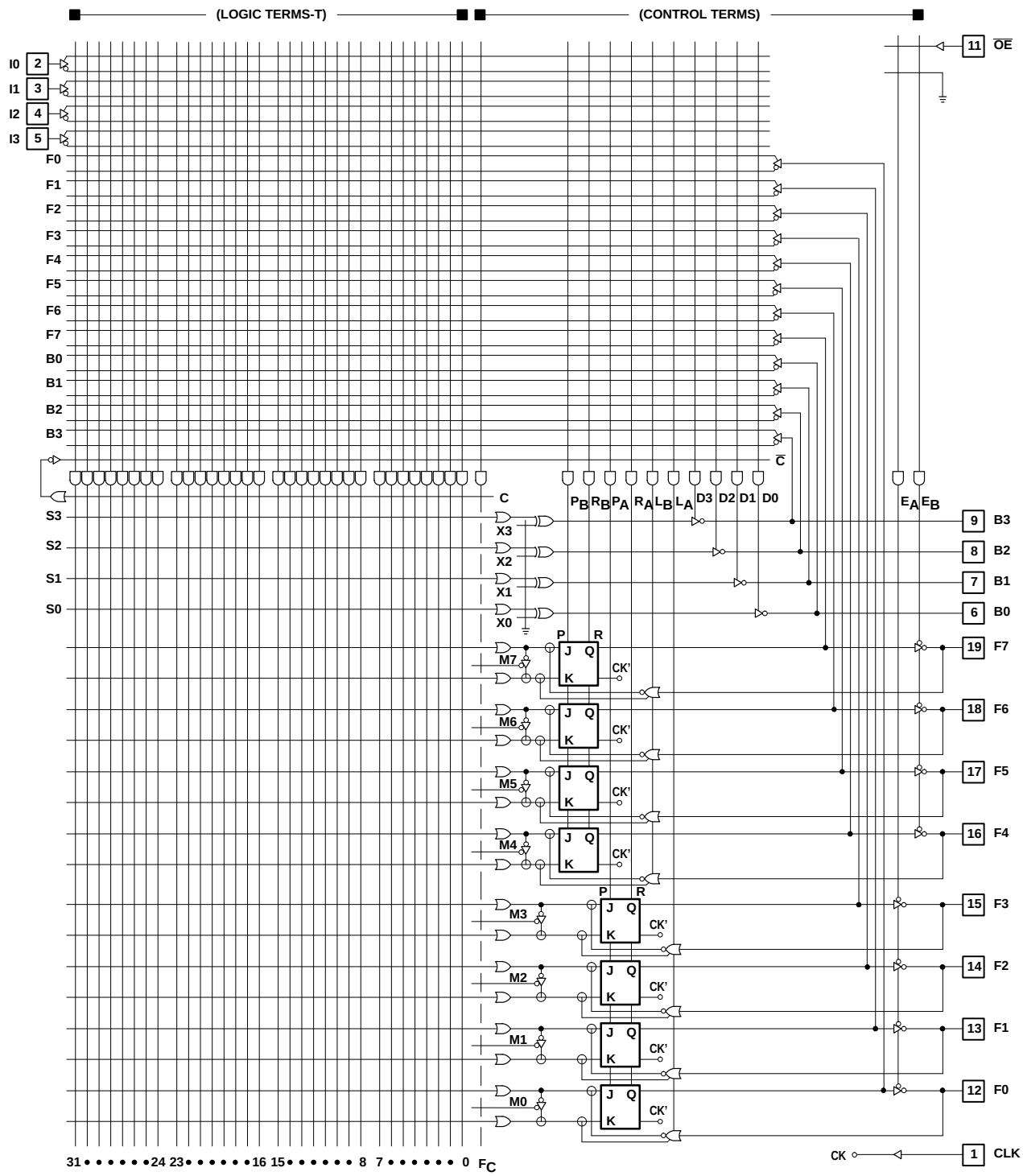
## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | DRAWING NUMBER |
|---|---|---|
| 20-Pin Plastic Dual In-Line Package (300mil-wide) | PLS159AN | 0408D |
| 20-Pin Plastic Leaded Chip Carrier | PLS159AA | 0400E |

# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

## LOGIC DIAGRAM

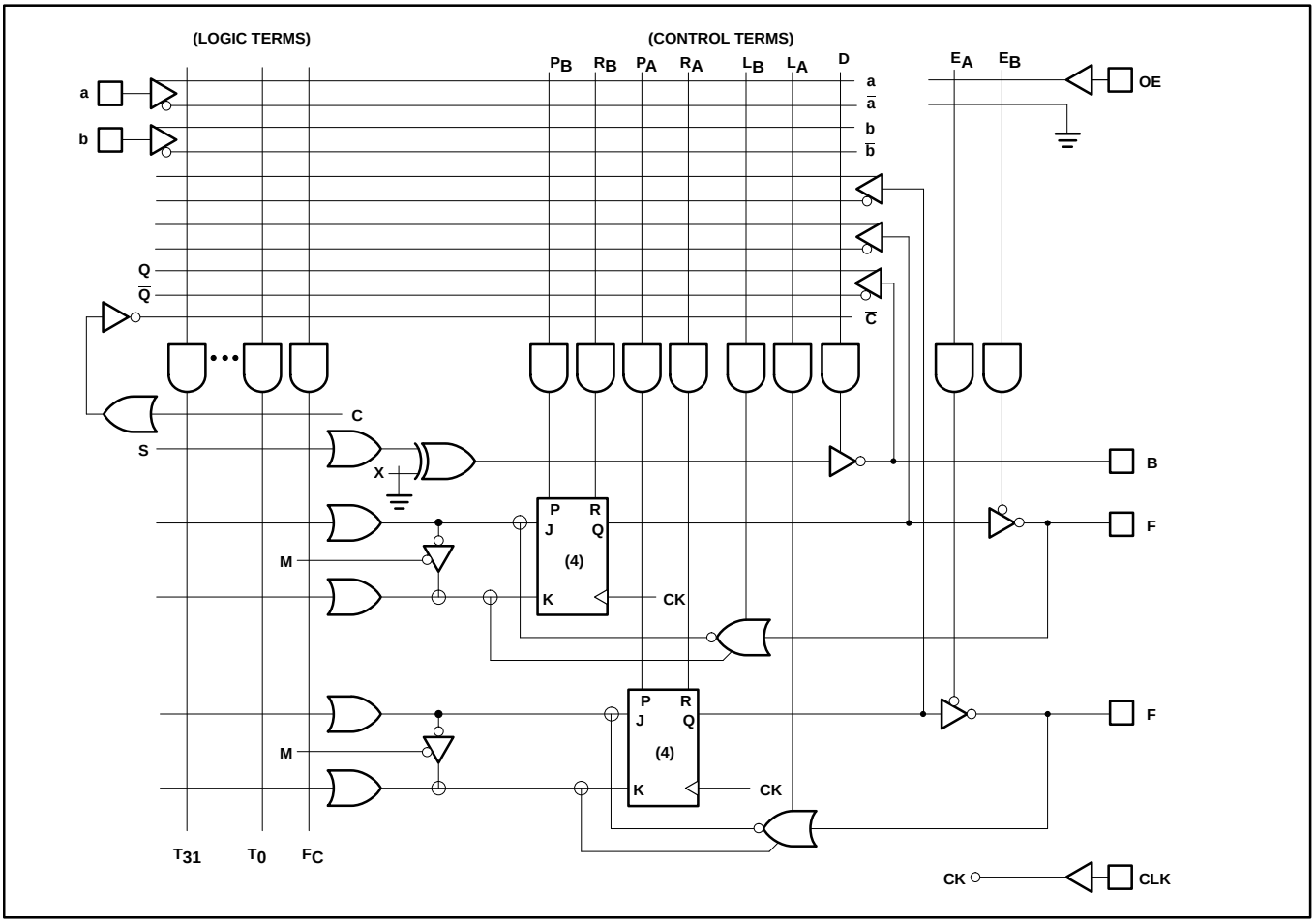



**NOTES:**
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. Programmable connection.

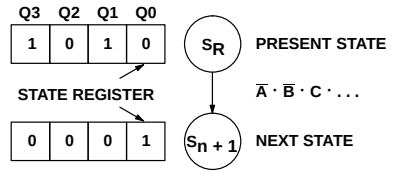
# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

## FUNCTIONAL DIAGRAM




## LOGIC FUNCTION




$\overline{A} \cdot \overline{B} \cdot C \cdot \ldots$

SET $Q_0$: $J_0 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_0 = 0$

RESET $Q_1$: $J_1 = 0$
$K_1 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD $Q_2$: $J_2 = 0$
$K_2 = 0$

TOGGLE $Q_3$: $J_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

**NOTE:**
Similar logic functions are applicable for D and T mode flip-flops.

## FLIP-FLOP TRUTH TABLE

| $\overline{OE}$ | L | CK | P | R | J | K | Q | F |
|---|---|---|---|---|---|---|---|---|
| H | | | | | | | | Hi-Z |
| L | X | X | L | X | X | X | L | H |
| L | X | X | H | L | X | X | H | L |
| L | X | X | L | H | X | X | L | H |
| L | L | ↑ | L | L | L | L | Q | $\overline{Q}$ |
| L | L | ↑ | L | L | L | H | L | H |
| L | L | ↑ | L | L | H | L | H | L |
| L | L | ↑ | L | L | H | H | $\overline{Q}$ | Q |
| H | H | ↑ | L | L | L | H | L | H* |
| H | H | ↑ | L | L | H | L | H | L* |
| +10V | X | ↑ | X | X | L | H | L | H* * |
| | X | ↑ | X | X | H | L | H | L* * |

**NOTES:**
1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 \ldots\ldots\ldots\ldots T_{31}$
   $T_n = \overline{C} \cdot (I0 \cdot I1 \cdot I2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B0 \cdot B1 \cdot \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't care
4. * = Forced at $F_n$ pin for loading the J-K flip-flop in the Input mode. The load control term, $L_n$ must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. * * = Forced at $F_n$ pin to load J-K flip-flop independent of program code (Diagnostic mode), 3-State B outputs.

## VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

## CAUTION: PLS159A PROGRAMMING ALGORITHM

The programming voltage required to program the PLS159A is higher (17.5V) than that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to insure that the correct algorithm is used.

## THERMAL RATINGS

| TEMPERATURE | |
|---|---|
| Maximum junction | 150°C |
| Maximum ambient | 75°C |
| Allowable thermal rise ambient to junction | 75°C |

## ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL | PARAMETER | RATINGS MIN | RATINGS MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | +7 | $V_{DC}$ |
| $V_{IN}$ | Input voltage | | +5.5 | $V_{DC}$ |
| $V_{OUT}$ | Output voltage | | +5.5 | $V_{DC}$ |
| $I_{IN}$ | Input currents | –30 | +30 | mA |
| $I_{OUT}$ | Output currents | | +100 | mA |
| $T_{amb}$ | Operating temperature range | 0 | +75 | °C |
| $T_{stg}$ | Storage temperature range | –65 | +150 | °C |

**NOTES:**

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

## DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP[1] | MAX | |
| **Input voltage[2]** | | | | | | |
| $V_{IH}$ | High | $V_{CC}$ = MAX | 2.0 | | | V |
| $V_{IL}$ | Low | $V_{CC}$ = MIN | | | 0.8 | V |
| $V_{IC}$ | Clamp | $V_{CC}$ = MIN, $I_{IN}$ = –12mA | | –0.8 | –1.2 | V |
| **Output voltage[2]** | | | | | | |
| $V_{OH}$ | High | $V_{CC}$ = MIN, $I_{OH}$ = –2mA | 2.4 | | | V |
| $V_{OL}$ | Low | $I_{OL}$ = 10mA | | 0.35 | 0.5 | V |
| **Input current** | | | | | | |
| $I_{IH}$ | High | $V_{CC}$ = MAX, $V_{IN}$ = 5.5V | | <1 | 80 | µA |
| $I_{IL}$ | Low | $V_{IN}$ = 0.45V | | –10 | –100 | µA |
| **Output current** | | | | | | |
| $I_{O(OFF)}$ | Hi-Z state[4, 7] | $V_{CC}$ = MAX, $V_{OUT}$ = 5.5V | | 1 | 80 | µA |
| | | $V_{OUT}$ = 0.45V | | –1 | –140 | µA |
| $I_{OS}$ | Short circuit[3, 5] | $V_{OUT}$ = 0V | –15 | | –70 | mA |
| $I_{CC}$ | $V_{CC}$ supply current[6] | $V_{CC}$ = MAX | | 150 | 190 | mA |
| **Capacitance** | | | | | | |
| $C_{IN}$ | Input | $V_{CC}$ = 5.0V, $V_{IN}$ = 2.0V | | 8 | | pF |
| $C_{OUT}$ | Output | $V_{OUT}$ = 2.0V | | 15 | | pF |

**NOTES:**
1. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with $V_{IH}$ applied to $\overline{OE}$.
5. Duration of short circuit should not exceed 1 second.
6. $I_{CC}$ is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.
7. Leakage values are a combination of input and output leakage.

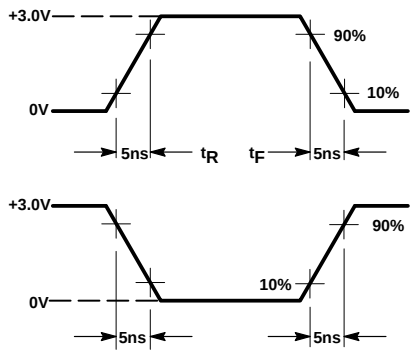
## AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

| SYMBOL | PARAMETER | FROM | TO | TEST CONDITION | LIMITS MIN | LIMITS TYP[1] | LIMITS MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **Pulse width** | | | | | | | | |
| $t_{CKH}$ | Clock[2] High | CK + | CK – | $C_L$ = 30pF | 20 | 15 | | ns |
| $t_{CKL}$ | Clock Low | CK – | CK + | $C_L$ = 30pF | 20 | 15 | | ns |
| $t_{CKP}$ | Period | CK + | CK + | $C_L$ = 30pF | 55 | 45 | | ns |
| $t_{PRH}$ | Preset/Reset pulse | (I,B) – | (I,B) + | $C_L$ = 30pF | 35 | 30 | | ns |
| **Setup time[5]** | | | | | | | | |
| $t_{IS1}$ | Input | (I,B) ± | CK + | $C_L$ = 30pF | 35 | 30 | | ns |
| $t_{IS2}$ | Input (through $F_n$) | F ± | CK + | $C_L$ = 30pF | 15 | 10 | | ns |
| $t_{IS3}$ | Input (through Complement Array)[4] | (I,B) ± | CK + | $C_L$ = 30pF | 55 | 45 | | ns |
| **Hold time** | | | | | | | | |
| $t_{IH1}$ | Input | (I,B) ± | CK + | $C_L$ = 30pF | 0 | –5 | | ns |
| $t_{IH2}$ | Input (through $F_n$) | F ± | CK + | $C_L$ = 30pF | 15 | 10 | | ns |
| **Propagation delay** | | | | | | | | |
| $t_{CKO}$ | Clock | CK + | F ± | $C_L$ = 30pF | | 15 | 20 | ns |
| $t_{OE1}$ | Output enable[3] | $\overline{OE}$ – | F – | $C_L$ = 30pF | | 20 | 30 | ns |
| $t_{OD1}$ | Output disable[3] | $\overline{OE}$ + | F + | $C_L$ = 5pF | | 20 | 30 | ns |
| $t_{PD}$ | Output | (I,B) ± | B ± | $C_L$ = 30pF | | 25 | 35 | ns |
| $t_{OE2}$ | Output enable[3] | (I,B) + | B ± | $C_L$ = 30pF | | 20 | 30 | ns |
| $t_{OD2}$ | Output disable[3] | (I,B) – | B + | $C_L$ = 5pF | | 20 | 30 | ns |
| $t_{PRO}$ | Preset/Reset | (I,B) + | F ± | $C_L$ = 30pF | | 35 | 45 | ns |
| $t_{PPR}$ | Power-on/preset | $V_{CC}$ + | F – | $C_L$ = 30pF | | 0 | 10 | ns |

**NOTES:**
1. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = +25°C.
2. To prevent spurious clocking, clock rise time (10% – 90%) ≤ 10ns.
3. For 3-State output; output enable times are tested with $C_L$ = 30pF to the 1.5V level, and $S_1$ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L$ = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with $S_1$ open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with $S_1$ closed.
4. When using the Complement Array $t_{CKP}$ = 75ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

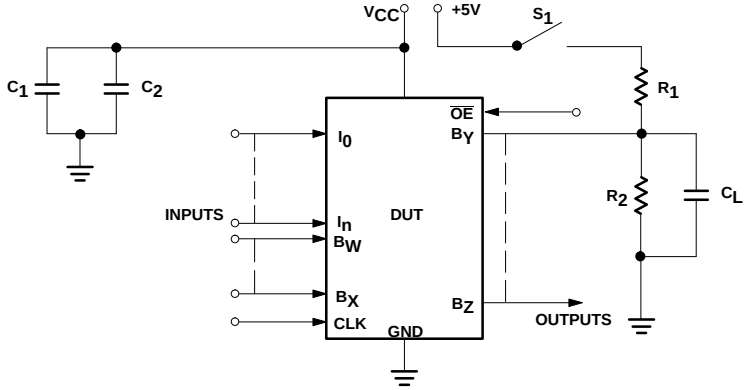
## VOLTAGE WAVEFORMS




**MEASUREMENTS:**
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

**Input Pulses**

## TEST LOAD CIRCUIT

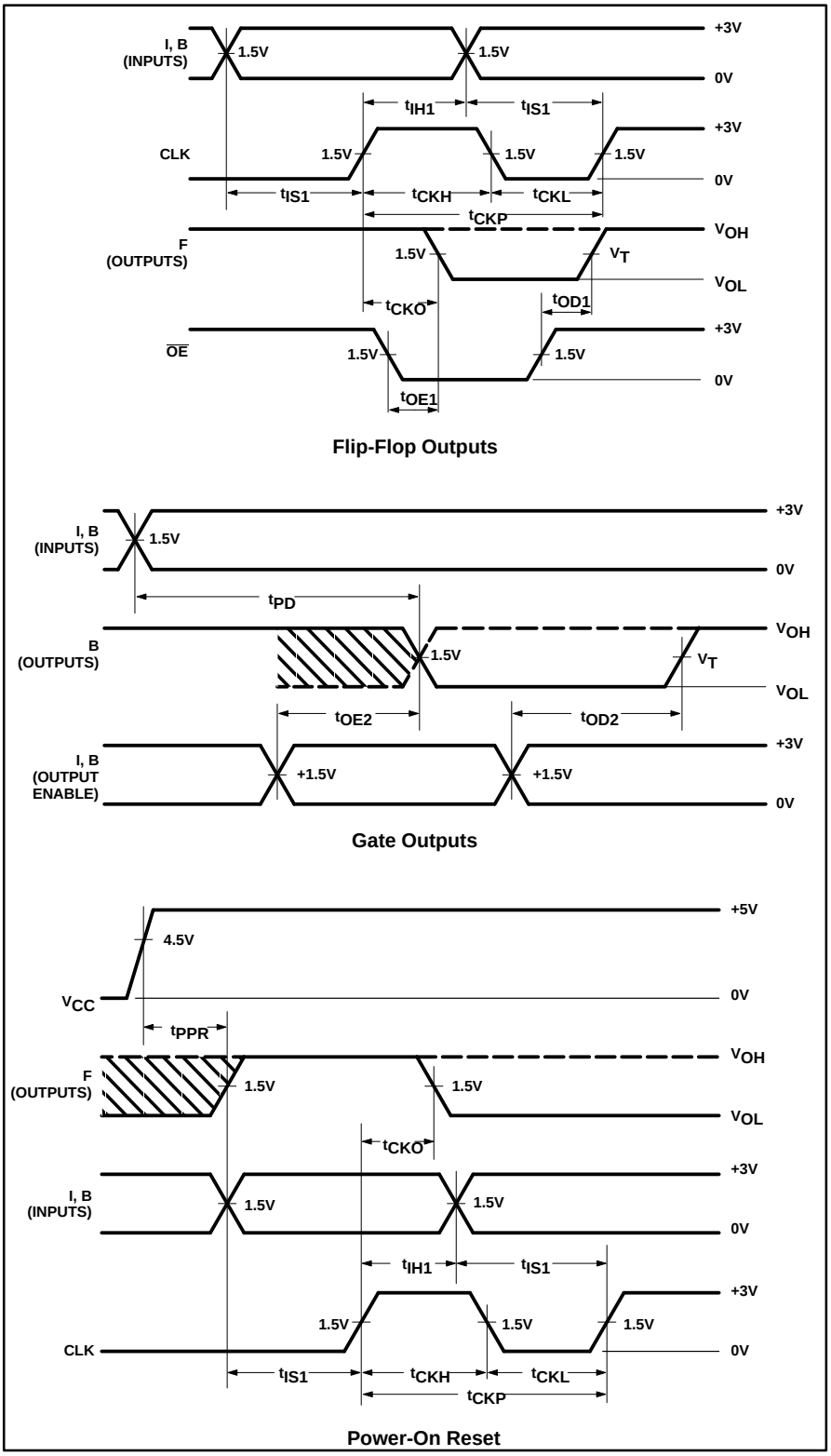



**NOTE:**
$C_1$ and $C_2$ are to bypass $V_{CC}$ to GND.

# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

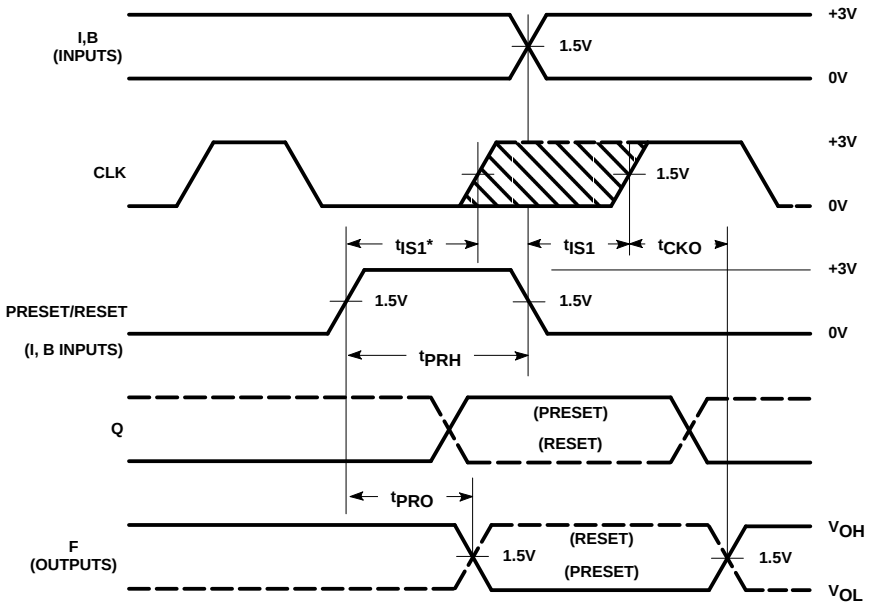
## TIMING DIAGRAMS




## TIMING DEFINITIONS

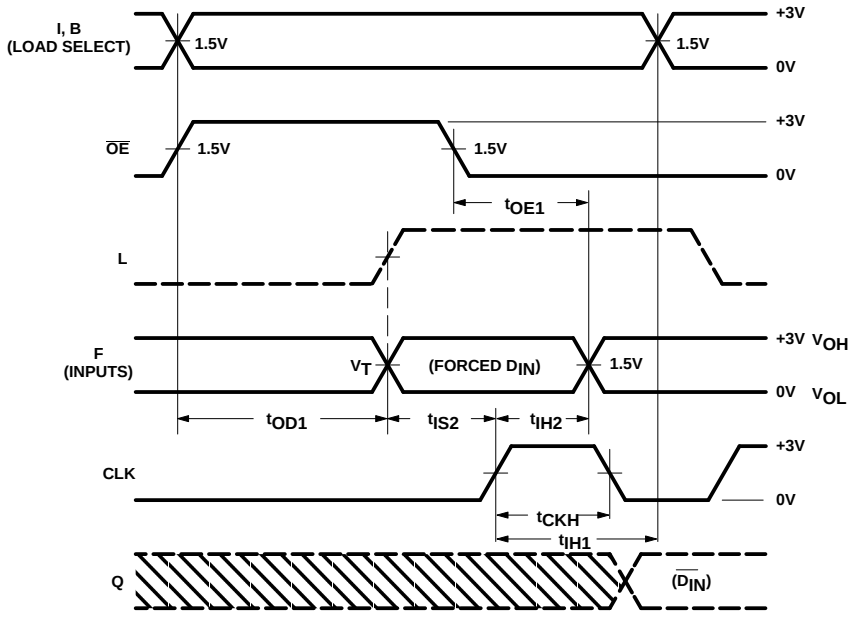
| SYMBOL | PARAMETER |
|---|---|
| $t_{CKH}$ | Width of input clock pulse. |
| $t_{CKL}$ | Interval between clock pulses. |
| $t_{CKP}$ | Clock period. |
| $t_{PRH}$ | Width of preset input pulse. |
| $t_{IS1}$ | Required delay between beginning of valid input and positive transition of clock. |
| $t_{IS2}$ | Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock. |
| $t_{IH1}$ | Required delay between positive transition of clock and end of valid input data. |
| $t_{IH2}$ | Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins. |
| $t_{CKO}$ | Delay between positive transition of clock and when outputs become valid (with $\overline{OE}$ Low). |
| $t_{OE1}$ | Delay between beginning of Output Enable Low and when outputs become valid. |
| $t_{OD1}$ | Delay between beginning of Output Enable High and when outputs are in the OFF-State. |
| $t_{PPR}$ | Delay between $V_{CC}$ (after power-on) and when flip-flop outputs become preset at “1” (internal Q outputs at “0”). |
| $t_{PD}$ | Propagation delay between combinational inputs and outputs. |
| $t_{OE2}$ | Delay between predefined Output Enable High, and when combinational outputs become valid. |
| $t_{OD2}$ | Delay between predefined Output Enable Low and when combinational outputs are in the OFF-State. |
| $t_{PRO}$ | Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid. |

**TIMING DIAGRAMS** (Continued)




* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if $t_{IS1}$ cannot be guaranteed by the user.

**Asynchronous Preset/Reset**




**Flip-Flop Input Mode**

# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

## LOGIC PROGRAMMING

The PLS159A is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

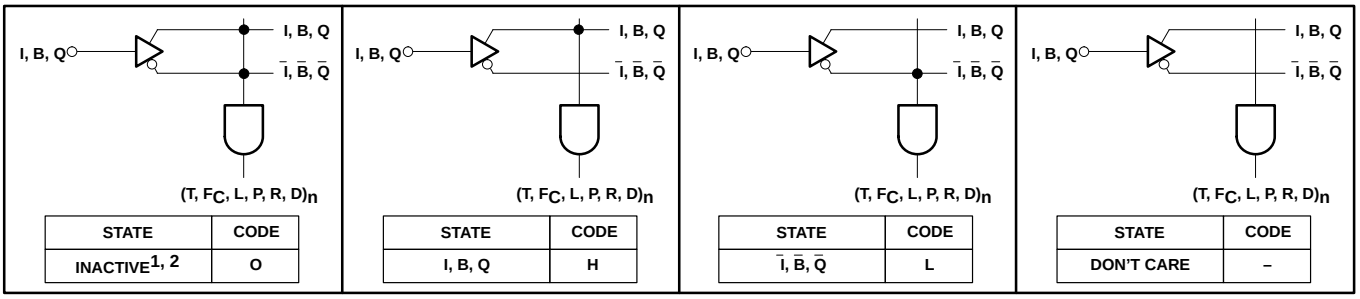
PLS159A logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

## PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* of this data handbook for additional information.

### "AND" ARRAY – (I), (B), (Qp)



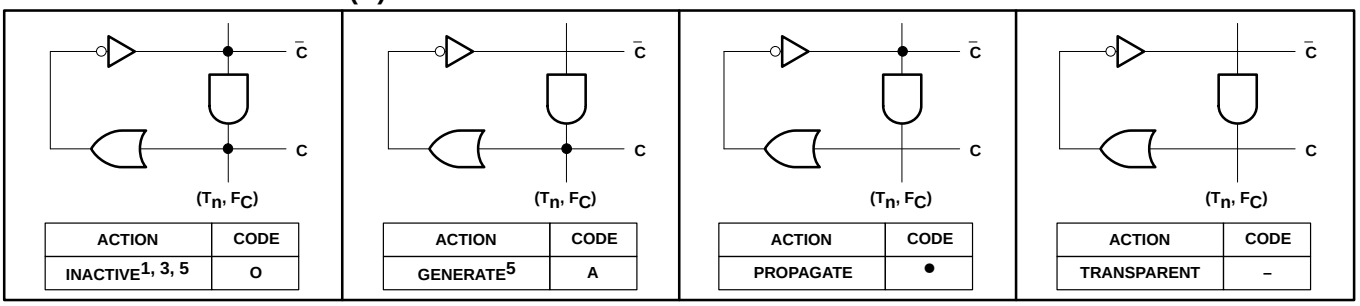

| STATE | CODE |
|---|---|
| INACTIVE[1, 2] | O |

| STATE | CODE |
|---|---|
| I, B, Q | H |

| STATE | CODE |
|---|---|
| $\overline{I}$, $\overline{B}$, $\overline{Q}$ | L |

| STATE | CODE |
|---|---|
| DON'T CARE | – |

### "COMPLEMENT" ARRAY – (C)



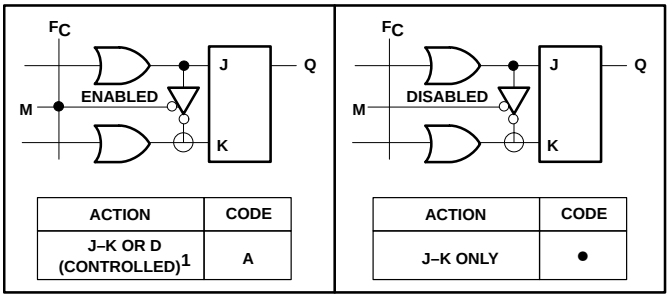

| ACTION | CODE |
|---|---|
| INACTIVE[1, 3, 5] | O |

| ACTION | CODE |
|---|---|
| GENERATE[5] | A |

| ACTION | CODE |
|---|---|
| PROPAGATE | • |

| ACTION | CODE |
|---|---|
| TRANSPARENT | – |

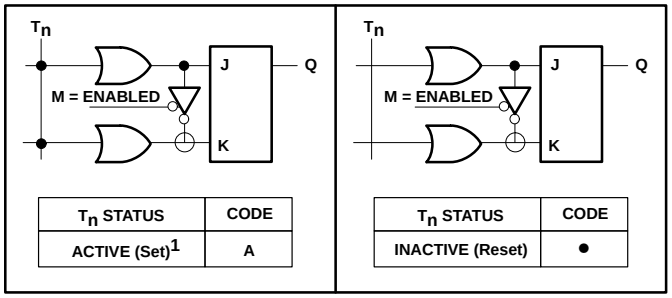
### "OR" ARRAY – (F-F CONTROL MODE)




| ACTION | CODE |
|---|---|
| J–K OR D (CONTROLLED)[1] | A |

| ACTION | CODE |
|---|---|
| J–K ONLY | • |

### "OR" ARRAY – ($Q_n$ = D-Type)




| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE (Set)[1] | A |

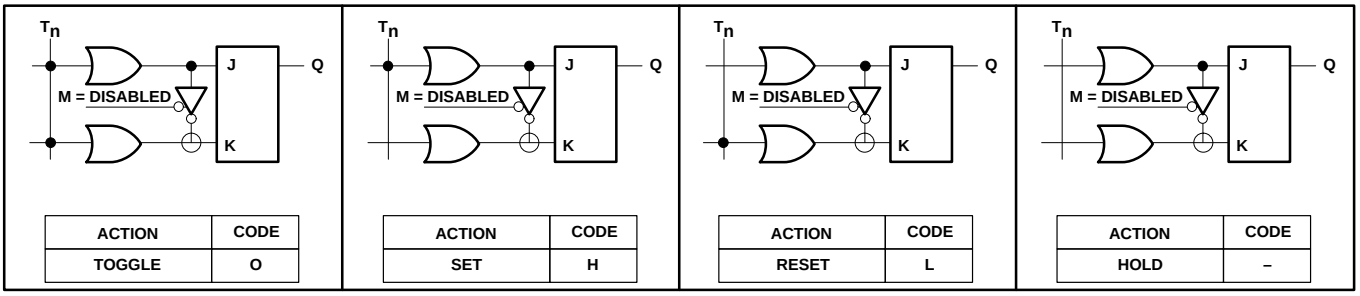
| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE (Reset) | • |

Notes on following page.

**CAUTION:**
THE PLS159A Programming Algorithm is different from the PLS159.

# Programmable logic sequencer ($16 \times 45 \times 12$) PLS159A

## "OR" ARRAY – ($Q_n$ = J-K Type)



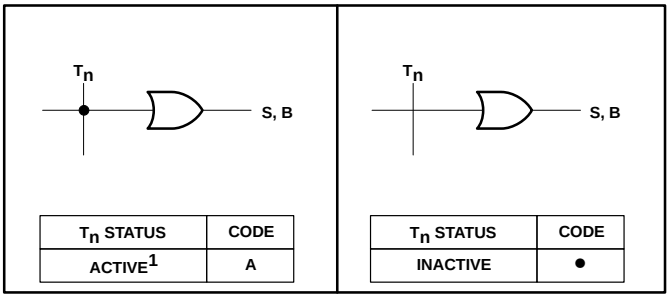

| ACTION | CODE |
|---|---|
| TOGGLE | O |

| ACTION | CODE |
|---|---|
| SET | H |

| ACTION | CODE |
|---|---|
| RESET | L |

| ACTION | CODE |
|---|---|
| HOLD | – |

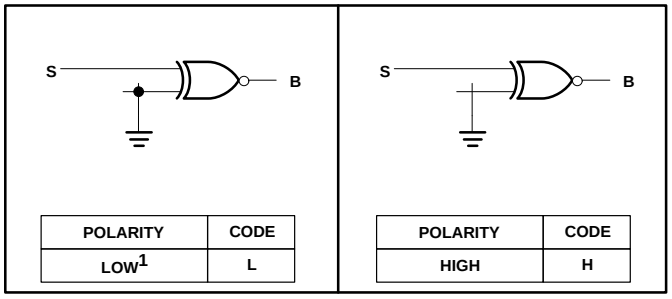
## "OR" ARRAY – (S or B)




| $T_n$ STATUS | CODE |
|---|---|
| ACTIVE[1] | A |

| $T_n$ STATUS | CODE |
|---|---|
| INACTIVE | • |

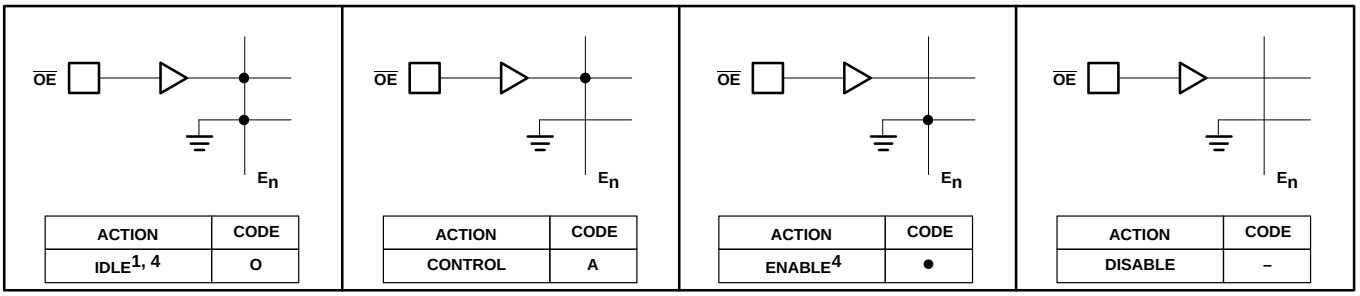
## "EX-OR" ARRAY – (B)




| POLARITY | CODE |
|---|---|
| LOW[1] | L |

| POLARITY | CODE |
|---|---|
| HIGH | H |

## "$\overline{OE}$" ARRAY – (E)




| ACTION | CODE |
|---|---|
| IDLE[1, 4] | O |

| ACTION | CODE |
|---|---|
| CONTROL | A |

| ACTION | CODE |
|---|---|
| ENABLE[4] | • |

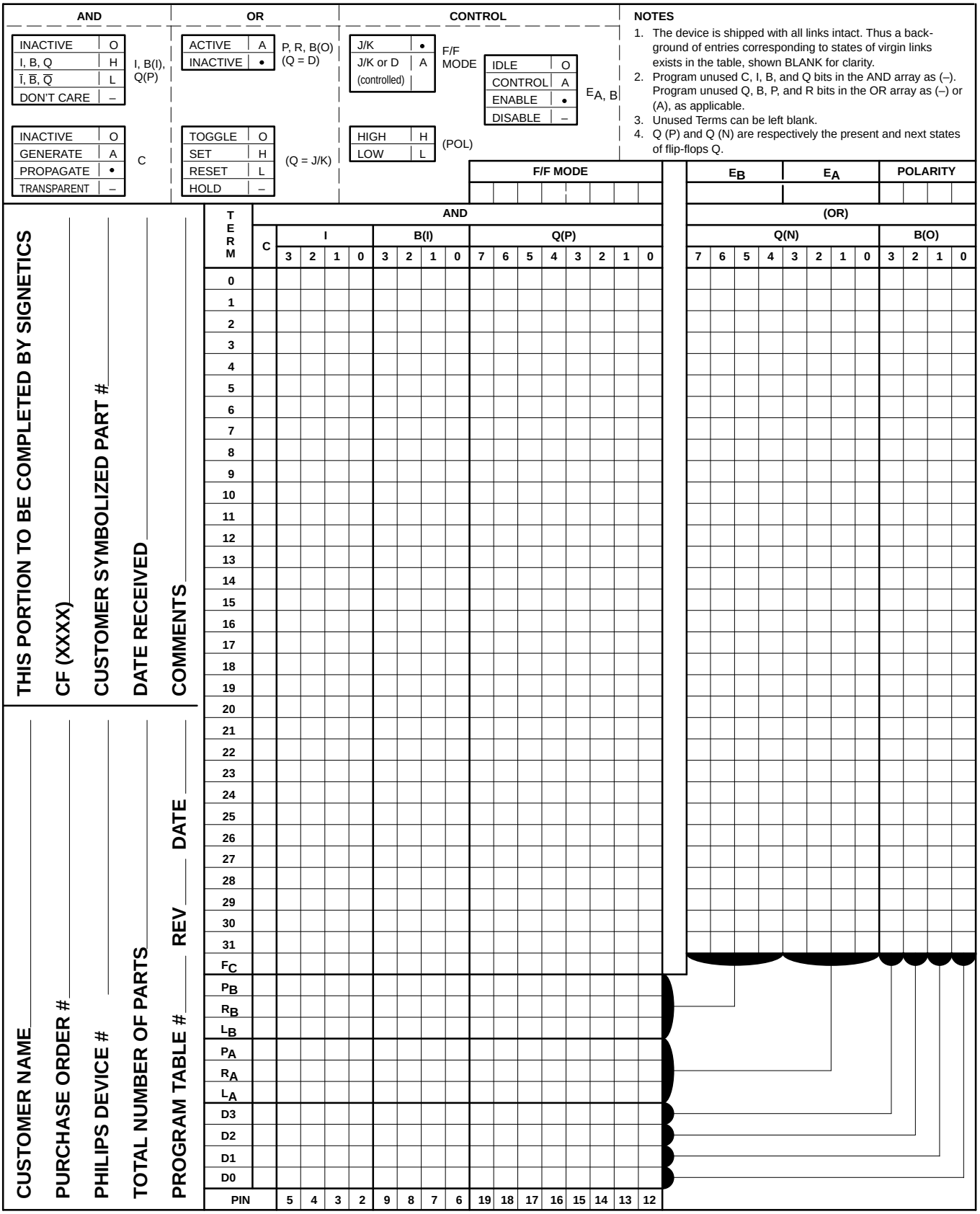
| ACTION | CODE |
|---|---|
| DISABLE | – |

**NOTES:**
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
2. Any gate $(T, F_C, L, P, R, D)_n$ will be unconditionally inhibited if both of the I, B, or Q links are left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates $T_n$, $F_C$.
4. $E_n$ = O and $E_n$ = • are logically equivalent states, since both cause $F_n$ outputs to be unconditionally enabled.
5. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

# Programmable logic sequencer ($16 \times 45 \times 12$)

# PLS159A

## PROGRAM TABLE



# Programmable logic sequencer ($16 \times 45 \times 12$) PLS159A

## SNAP RESOURCE SUMMARY DESIGNATIONS