FAIRCHILD
A Schlumberger Company

# F6850/F68A50/F68B50 Asynchronous Communications Interface Adapter (ACIA)

Microprocessor Product

## Description

The F6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications information to bus-organized systems, such as the F6800 microprocessing unit (MPU).

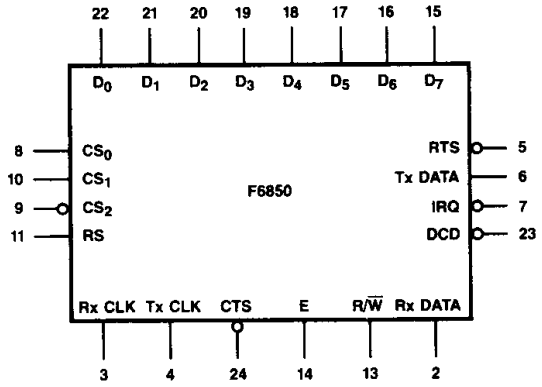
The bus interface of the F6850 includes select, enable read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with a 0-600 bps modem.

- **8- and 9-Bit Transmission**
- **Optional Even and Odd Parity**
- **Parity, Overrun, and Framing Error Checking**
- **Programmable Control Register**
- **Optional ÷1, ÷16, and ÷64 Clock Modes**
- **Up to 1.0 Mbps Transmission**
- **False Start Bit Deletion**
- **Peripheral/Modem Control Functions**
- **Double Buffered**
- **One or Two Stop Bit Operation**

## Pin Functions

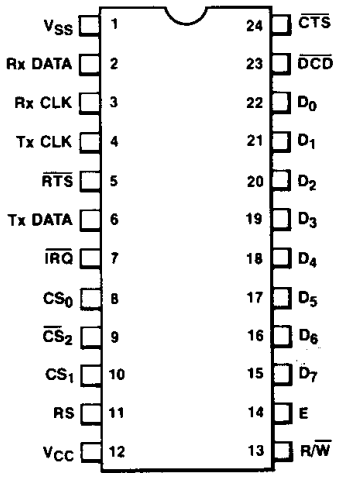
| | |
|---|---|
| $D_0-D_7$ | Bidirectional Data Lines |
| Rx DATA | Receive Data Input |
| Rx CLK | Receive Clock Input |
| Tx CLK | Transmit Clock Input |
| $CS_0$, $CS_1$, $\overline{CS_2}$ | Chip Select Inputs |
| RS | Register Select Input |
| $\overline{CTS}$ | Clear-to-Send Input |
| E | Enable Input |
| R/$\overline{W}$ | Read/Write Input |
| $\overline{RTS}$ | Request-to-Send Output |
| Tx DATA | Transmit Data Output |
| $\overline{IRQ}$ | Interrupt Request Output |
| $\overline{DCD}$ | Data Carrier Detect Output |

## Logic Symbol




$V_{CC}$ = Pin 12
$V_{SS}$ = Pin 1

## Connection Diagram
## 24-Pin DIP




(Top View)

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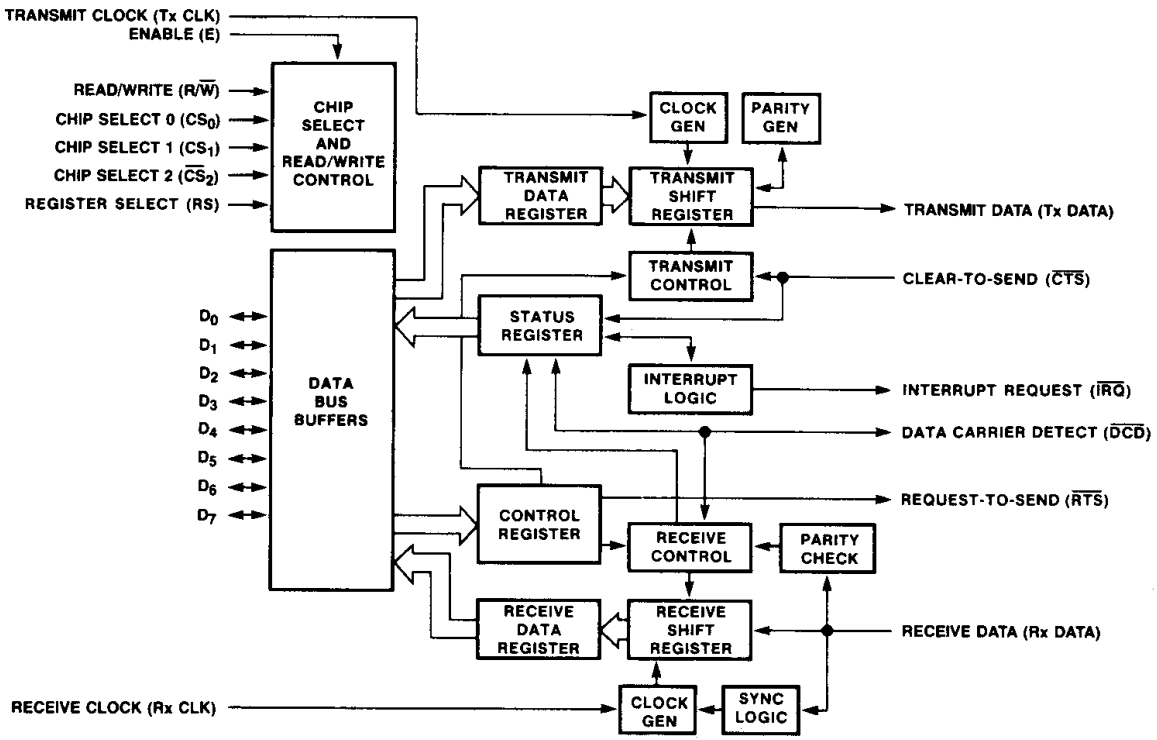
## Block Diagram




### Functional Description

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only. The read-only registers are status and receive data; the write-only registers are control and transmit data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

### Power On/Master Reset

The master reset ($CR_0$, $CR_1$) should be set during system initialization to ensure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. Control bits $CR_5$ and $CR_6$ should also be programmed to define the state of the request-to-send ($\overline{RTS}$) output whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset, which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable control register can be set for a number of options, such as variable clock divider ratios, variable word length, one or two stop bits, and parity (even, odd, or none).

### Transmit

A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in turn in a polling sequence. A character may be written into the transmit data register if the status read operation has indicated that the transmit data register is empty. This character is transferred to a shift register, where it is serialized and transmitted from the transmit data (Tx DATA) output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character, and occurs between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a transmit data register empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character is transferred automatically into the shift register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

### Receive

Data is received from a peripheral by means of the receive data (Rx DATA) input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and -64 ratios are provided for internal synchronization. Bit

synchronization in the divide-by-16 and -64 modes is initiated by the detection of 8 or 32 LOW samples, respectively, on the receive data line. False start bit deletion capability ensures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) is checked and the error indication made available in the status register along with framing error, overrun error, and receive data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receive data is full, the character is placed on the 8-bit ACIA bus when a read data command is received from the MPU. When parity has been selected for an 8-bit word (seven bits plus parity), the receiver strips the parity bit ($D_7 = 0$) so that data alone is transferred to the MPU. This feature reduces MPU programming. The status register can be read again to determine when another character is available in the receive data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

**Input/Output Functions**
The ACIA interfaces to the F6800 MPU through an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals, in conjunction with F6800 VMA output, permit the MPU to have complete control over the ACIA.

**ACIA Bidirectional Data ($D_0 - D_7$)**
The bidirectional data lines ($D_0 - D_7$) allow for data transfer between the ACIA and the MPU. The data bus output drivers are 3-state devices that remain in the high-impedance (OFF) state except when the MPU performs an ACIA read operation.

**ACIA Enable (E)**
The enable signal (E) is a high-impedance, TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal normally is a derivative of the F6800 $\phi 2$ clock.

**Read/Write (R/$\overline{W}$)**
The read/write line is a high-impedance input that is TTL-compatible and is used to control the direction of data flow through the ACIA input/output data bus interface. When R/$\overline{W}$ is HIGH (MPU read cycle), ACIA output drivers are turned on and a selected register is read. When it is LOW, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the R/$\overline{W}$ signal is used to select read-only or write-only registers within the ACIA.

**Chip Select ($CS_0$, $CS_1$, $\overline{CS_2}$)**
These three high-impedance, TTL-compatible input lines are used to address the ACIA. The ACIA is selected when $CS_0$ and $CS_1$ are HIGH and $\overline{CS_2}$ is LOW. Transfers of data to and from the ACIA are then performed under the control of the E, R/$\overline{W}$, and RS signals.

**Register Select (RS)**
The register select line is a high-impedance input that is TTL-compatible. A HIGH level is used to select the transmit/receive data registers and a LOW level the control/status registers. The R/$\overline{W}$ signal line is used in conjunction with RS to select the read-only or write-only register in each register pair.

**Interrupt Request ($\overline{IRQ}$)**
Interrupt request is a TTL-compatible, open-drain (no internal pull-up), active-LOW output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains LOW as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The IRQ status bit, when HIGH, indicates that the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the transmitter interrupt enabled condition is selected ($CR_5 \cdot \overline{CR_6}$), and the transmit data register empty (TDRE) status bit is HIGH. The TDRE status bit indicates the current status of the transmitter data register except when inhibited by the $\overline{CTS}$ line being HIGH or the ACIA being maintained in the reset condition. The interrupt is cleared by writing data into the transmit data register. The interrupt is masked by disabling the transmitter interrupt via $CR_5$ or $\overline{CR_6}$, or by the loss of $\overline{CTS}$, which inhibits the TDRE status bit. The receiver section causes an interrupt when the receiver interrupt enable is set and the receive data register full (RDRF) status bit is HIGH, an overrun has occurred, or the data carrier detect ($\overline{DCD}$) line has gone HIGH. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the receive data register or resetting the ACIA. The receiver interrupt is masked by resetting the receiver interrupt enable.

**Clock Inputs**
Separate high-impedance, TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

**Transmit Clock (Tx CLK)**
The transmit clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

**Receive Clock (Rx CLK)**
The receive clock input is used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

**Serial Input/Output Lines**

**Receive Data (Rx DATA)**
The receive data line is a high-impedance, TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

**Transmit Data (Tx DATA)**
The transmit data output line transfers serial data to a modem or other peripheral.

**Peripheral/Modem Control**
The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are clear-to-send, request-to-send and data carrier detect.

**Clear-to-Send ($\overline{CTS}$)**
This high-impedance, TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem clear-to-send active-LOW output by inhibiting the transmit data register empty (TDRE) status bit.

**Request-to-Send ($\overline{RTS}$)**
The request-to-send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of control register bits $CR_5$ and $CR_6$. When $CR_6 = 0$ or both $CR_5$ and $CR_6 = 1$, the $\overline{RTS}$ output is LOW (the active state.) This output can also be used for data terminal ready ($\overline{DTR}$).

**Data Carrier Detect ($\overline{DCD}$)**
This high-impedance, TTL-compatible input provides automatic control, such as in the receiving end of a communications link, by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when HIGH. A LOW-to-HIGH transition of $\overline{DCD}$ initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the receive interrupt enable bit is set. The RxCLK must be running for proper $\overline{DCD}$ operation.

**ACIA Registers**
The block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in *Table 1*.

**Transmit Data Register (TDR)**
Data is written into the transmit data register during the negative transition of the E (Enable) pulse when the ACIA has been addressed with RS HIGH and R/$\overline{W}$ LOW. Writing data into the register causes the TDRE bit in the status register to go LOW. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, the transfer takes place within one bit time of the trailing edge of the write command. If a character is being transmitted, the new data character commences as soon as the previous character is complete. The transfer of data causes the TDRE bit to indicate empty.

**Receive Data Register (RDR)**
Data is automatically transferred to the empty receive data register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the receive data register full (RDRF) bit in the status buffer to go HIGH (full). Data may then be read through the bus by addressing the ACIA and selecting the RDR with RS and R/$\overline{W}$ HIGH when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by the RDRF bit to indicate whether or not the data is current. When the receive data register is full, the automatic transfer of data from the receiver shift register to the data register is inhibited and the RDR contents remain valid, with its current status stored in the status register.

**Control Register**
The ACIA control register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are LOW. This register controls the function of the receiver, transmitter, interrupt enables, and the request-to-send peripheral/modem control output.

**Counter Divide Select Bits ($CR_0$ and $CR_1$)**
The counter divide select bits ($CR_0$ and $CR_1$) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA that clears the status register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other control register bits. Note that after power-on or a power fail/start, these bits must be set HIGH to reset the ACIA. After resetting, the clock divide ratio may be selected.

**Table 1 Definition of ACIA Register Contents**

| Data Bus Line Number | Buffer Address | | | |
|---|---|---|---|---|
| | RS • R/$\overline{W}$ Transmit Data Register (Write Only) | RS • R/$\overline{W}$ Receive Data Register (Read Only) | $\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only) | $\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only) |
| 0 | Data Bit 0* | Data Bit 0 | Counter Divide Select 1 ($CR_0$) | Receive Data Register Full (RDRF) |
| 1 | Data Bit 1 | Data Bit 1 | Counter Divide Select 2 ($CR_1$) | Transmit Data Register Empty (TDRE) |
| 2 | Data Bit 2 | Data Bit 2 | Word Select 1 ($CR_2$) | Data Carrier Detect ($\overline{DCD}$) |
| 3 | Data Bit 3 | Data Bit 3 | Word Select 2 ($CR_3$) | Clear-to-Send ($\overline{CTS}$) |
| 4 | Data Bit 4 | Data Bit 4 | Word Select 3 ($CR_4$) | Framing Error (FE) |
| 5 | Data Bit 5 | Data Bit 5 | Transmit Control 1 ($CR_5$) | Receiver Overrun (OVRN) |
| 6 | Data Bit 6 | Data Bit 6 | Transmit Control 2 ($CR_6$) | Parity Error (PE) |
| 7 | Data Bit 7*** | Data Bit 7** | Receive Interrupt Enable ($CR_7$) | Interrupt Request ($\overline{IRQ}$) |

*Leading bit = LSB = Bit 0 **Data bit is zero in 7-bit plus parity modes. ***Data bit is "don't care" in 7-bit plus parity modes.



These counter select bits provide for the following clock divide ratios:

| $CR_1$ | $CR_0$ | Function |
|---|---|---|
| 0 | 0 | ÷1 |
| 0 | | ÷16 |
| 1 | 0 | ÷64 |
| 1 | 1 | Master Reset |

**Word Select Bits ($CR_2$, $CR_3$ and $CR_4$)**
The word select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

| $CR_4$ | $CR_3$ | $CR_2$ | Function |
|---|---|---|---|
| 0 | 0 | 0 | 7 Bits + Even Parity + 2 Stop Bits |
| 0 | 0 | 1 | 7 Bits + Odd Parity + 2 Stop Bits |
| 0 | 1 | 0 | 7 Bits + Even Parity + 1 Stop Bit |
| 0 | 1 | 1 | 7 Bits + Odd Parity + 1 Stop Bit |
| 1 | 0 | 0 | 8 Bits + 2 Stop Bits |
| 1 | 0 | 1 | 8 Bits + 1 Stop Bit |
| 1 | 1 | 0 | 8 Bits + Even Parity + 1 Stop Bit |
| 1 | 1 | 1 | 8 Bits + Odd Parity + 1 Stop Bit |

Word length, parity select, and stop bit changes are not buffered and therefore become effective immediately.

**Transmitter Control Bits ($CR_5$ and $CR_6$)**
Two transmitter control bits provide for the control of the interrupt from the transmit data register empty condition, the request-to-send ($\overline{RTS}$) output, and the transmission of a break level (space). The following encoding format is used:

| $CR_6$ | $CR_5$ | Function |
|---|---|---|
| 0 | 0 | $\overline{RTS}$ = LOW, Transmitting Interrupt Disabled |
| 0 | 1 | $\overline{RTS}$ = LOW, Transmitting Interrupt Enabled |
| 1 | 0 | $\overline{RTS}$ = HIGH, Transmitting Interrupt Disabled |
| 1 | 1 | $\overline{RTS}$ = LOW, Transmits a Break Level on the Transmit Data Output. Transmitting Interrupt Disabled. |

**Receive Interrupt Enable Bit ($CR_7$)**
The following interrupts are enabled by a HIGH level in bit position 7 of the control register ($CR_7$): receive data register full, overrun, or a LOW-to-HIGH transition on the data carrier detect ($\overline{DCD}$) signal line.

**Status Register**
Information on the status of the ACIA is available to the MPU by reading the ACIA status register. This read-only register is selected when RS is LOW and R/$\overline{W}$ is HIGH. Information stored in this register indicates the status of the transmit data register, the receive data register and error logic, and the peripheral/modem status inputs of the ACIA.

**Receive Data Register Full (RDRF), Bit 0**
Receive data register full indicates that received data has been transferred to the receive data register. The RDRF bit is cleared after an MPU read of the receive data register or by a master reset. The cleared or empty state indicates that the

contents of the receive data register are not current. Data carrier detect being HIGH also causes RDRF to indicate empty.

**Transmit Data Register Empty (TDRE), Bit 1**
The transmit data register empty bit being set HIGH indicates that the transmit data register contents have been transferred and that new data may be entered. The LOW state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

**Data Carrier Detect ($\overline{DCD}$), Bit 2**
The data carrier detect bit is HIGH when the $\overline{DCD}$ input from a modem has gone HIGH to indicate that a carrier is not present. This bit going HIGH causes an interrupt request to be generated when the receive interrupt enable is set. It remains HIGH after the $\overline{DCD}$ input is returned LOW until cleared by reading first the status register and then the data register, or until a master reset occurs. If the $\overline{DCD}$ input remains HIGH after read status and read data or master reset has occurred, the interrupt is cleared, and the $\overline{DCD}$ status bit remains HIGH and will follow the $\overline{DCD}$ input.

**Clear-to-Send ($\overline{CTS}$), Bit 3**
The clear-to-send bit indicates the state of the clear-to-send input from a modem. A LOW $\overline{CTS}$ indicates that there is a clear-to-send from the modem. In the HIGH state, the transmit data register empty bit is inhibited and the clear-to-send status bit is HIGH. Master reset does not affect the clear-to-send status bit.

**Framing Error (FE), Bit 4**
Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

**Receiver Overrun (OVRN), Bit 5**
Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the receive data register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The overrun does not occur in the status register until the valid character prior to overrun has been read. The RDRF bit remains set until the overrun is reset. Character synchronization is maintained during the overrun condition. The overrun indication is reset after the reading of data from the receive data register or by a master reset.

**Parity Error (PE), Bit 6**
The parity error flag indicates that the number of HIGHs (1's) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication is present as long as the data character is in the RDR. If no parity is selected, both the transmitter parity generator output and the receiver parity check results are inhibited.

**Interrupt Request (IRQ), Bit 7**
The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable is indicated in this status bit. Any time the $\overline{IRQ}$ output is LOW, the IRQ bit is HIGH to indicate the interrupt or service request status. The IRQ bit is cleared by a read operation to the receive data register or a write operation to the transmit data register.

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage | −0.3 V, +7.0 V |
| Input Voltage | −0.3 V, +7.0 V |
| Operating Temperature − $T_L$, $T_H$ | |
| F6850, F68A50, F68B50 | 0°C, +70°C |
| F6850C, F68A50C | −40°C, +85°C |
| F6850DL | −55°C, +85°C |
| F6850DM | −55°C, +125°C |
| Storage Temperature Range | −55°C, +150°C |
| Thermal Resistance | |
| Ceramic | 60°C/W |
| Plastic | 120°C/W |

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

**DC Characteristics** $V_{CC}$ = 5.0 V ±5%, $V_{SS}$ = 0, $T_A$ = $T_L$ to $T_H$, unless otherwise noted

| Symbol | Characteristic | Signal | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$ | V | |
| $V_{IL}$ | Input LOW Voltage | | −0.3 | | 0.8 | V | |
| $I_{IN}$ | Input Leakage Current | R/$\overline{W}$, $CS_0$, $CS_1$, $\overline{CS_2}$, RS, Rx DATA, Rx CLK, $\overline{CTS}$, $\overline{DCD}$ | | 1.0 | 2.5 | μA | $V_{IN}$ = 0 to 5.25 V |
| $I_{TSI}$ | 3-State Input Current (OFF State) | $D_0$-$D_7$ | | 2.0 | 10 | μA | $V_{IN}$ = 0.4 to 2.4 V |
| $V_{OH}$ | Output HIGH Voltage | $D_0$-$D_7$ | 2.4 | | | V | $I_{Load}$ = −205 μA, Enable Pulse Width < 25 μs |
| | | Tx DATA, $\overline{RTS}$ | 2.4 | | | | $I_{Load}$ = −100 μA, Enable Pulse Width < 25 μs |
| $V_{OL}$ | Output LOW Voltage | | | | 0.4 | V | $I_{Load}$ = 1.6 mA, Enable Pulse Width < 25 μs |
| $I_{LOH}$ | Output Leakage Current | $\overline{IRQ}$ | | 1.0 | 10 | μA | $V_{OH}$ = 2.4 V |
| $P_D$ | Power Dissipation | | | 300 | 525 | mW | |
| $C_{IN}$ | Input Capacitance | $D_0$-$D_7$ | | 10 | 12.5 | pF | $V_{IN}$ = 0, $T_A$ = 25°C, f = 1.0 MHz |
| | | E, Tx CLK, Rx CLK, R/$\overline{W}$, RS, Rx DATA, $CS_0$, $CS_1$, $\overline{CS_2}$, $\overline{CTS}$, $\overline{DCD}$ | | 7.0 | 7.5 | | |
| $C_{OUT}$ | Output Capacitance | $\overline{RTS}$, Tx DATA | | | 10 | pF | $V_{IN}$ = 0, $T_A$ = 25°C, f = 1.0 MHz |
| | | $\overline{IRQ}$ | | | 5.0 | | |

**AC Characteristics** $V_{CC}$ = 5.0 V ±5%, $V_{SS}$ = 0, $T_A = T_L$ to $T_H$, unless otherwise noted

| Symbol | Characteristic | F6850 | | F68A50 | | F68B50 | | Unit | Condition |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $PW_{CL}$ | Minimum Clock Pulse Width, LOW ÷16, ÷64 Modes | 600 | | 450 | | 280 | | ns | *Figure 1* |
| $PW_{CH}$ | Minimum Clock Pulse Width, HIGH ÷16, ÷64 Modes | 600 | | 450 | | 280 | | ns | *Figure 2* |
| $f_C$ | Clock Frequency ÷1 Mode<br>÷16, ÷64 Modes | | 500<br>800 | | 750<br>1000 | | 1000<br>1500 | kHz | |
| $t_{TDD}$ | Clock-to-Data Delay for Transmitter | | 600 | | 540 | | 460 | ns | *Figure 3* |
| $t_{RDS}$ | Receive Data Set-up Time ÷1 Mode | 250 | | 100 | | 30 | | ns | *Figure 4* |
| $t_{RDH}$ | Receive Data Hold Time ÷1 Mode | 250 | | 100 | | 30 | | ns | *Figure 5* |
| $t_{IR}$ | Interrupt Request Release Time | | 1.2 | | 0.9 | | 0.7 | μs | *Figure 6* |
| $t_{RTS}$ | Request-to-Send Delay Time | | 560 | | 480 | | 400 | ns | *Figure 6* |
| $t_r$, $t_f$ | Input Transition Times (Except Enable) | | 1.0 | | 0.5 | | 0.25 | μs | Note |

**Note**
1.0 μs or 10% of the pulse width, whichever is smaller

**Bus Timing Characteristics**
**Read** *(Figures 7 and 9)*

| Symbol | Characteristic | F6850 | | F68A50 | | F68B50 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{cyc}E$ | Enable Cycle Time | 1.0 | | 0.666 | | 0.500 | | μs |
| $PW_{EH}$ | Enable Pulse Width, HIGH | 0.45 | 25 | 0.28 | 25 | 0.22 | 25 | μs |
| $PW_{EL}$ | Enable Pulse Width, LOW | 0.43 | | 0.28 | | 0.21 | | μs |
| $t_{AS}$ | Set-up Time, Address, and R/$\overline{W}$ Valid to Enable Positive Transition | 160 | | 140 | | 70 | | ns |
| $t_{DDR}$ | Data Delay Time | | 320 | | 220 | | 180 | ns |
| $t_H$ | Data Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{AH}$ | Address Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{Er}$, $t_{Ef}$ | Rise and Fall Time for Enable Input | | 25 | | 25 | | 25 | ns |
| **Write** *(Figures 8 and 9)* | | | | | | | | |
| $t_{cyc}E$ | Enable Cycle Time | 1.0 | | 0.666 | | 0.500 | | μs |
| $PW_{EH}$ | Enable Pulse Width, HIGH | 0.45 | 25 | 0.28 | 25 | 0.22 | 25 | μs |
| $PW_{EL}$ | Enable Pulse Width, LOW | 0.43 | | 0.28 | | 0.21 | | μs |
| $t_{AS}$ | Set-up Time, Address, and R/$\overline{W}$ Valid to Enable Positive Transition | 160 | | 140 | | 70 | | ns |
| $t_{DSW}$ | Data Set-up Time | 100 | | 80 | | 60 | | ns |
| $t_H$ | Data Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{AH}$ | Address Hold Time | 10 | | 10 | | 10 | | ns |
| $t_{Er}$, $t_{Ef}$ | Rise and Fall Time for Enable Input | | 25 | | 25 | | 25 | ns |

**Fig. 1 Clock Pulse Width, LOW State**

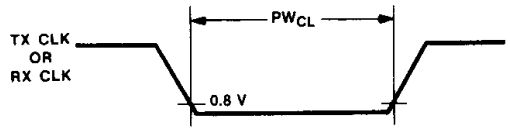



**Fig. 2 Clock Pulse Width, HIGH State**

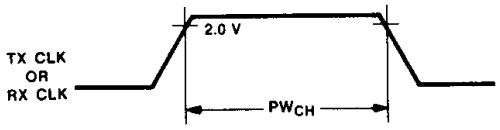



**Fig. 3 Transmit Data Output Delay**

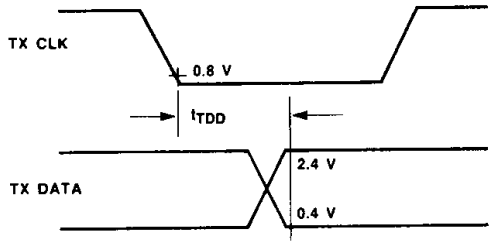



**Fig. 4 Receive Data Set-up Time (÷1 Mode)**

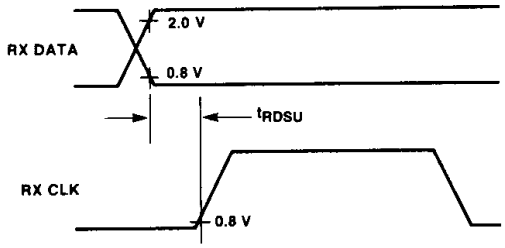



**Fig. 5 Receive Data Hold Time (÷1 Mode)**

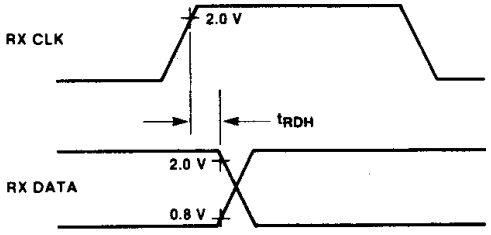



**Fig. 6 Request-to-Send Delay and Interrupt Request Release Times**

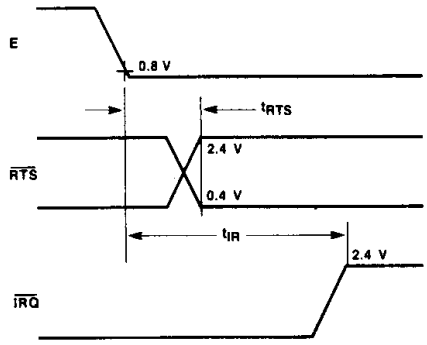



**Fig. 7 Bus Read Timing Characteristics (Read Information from ACIA)**

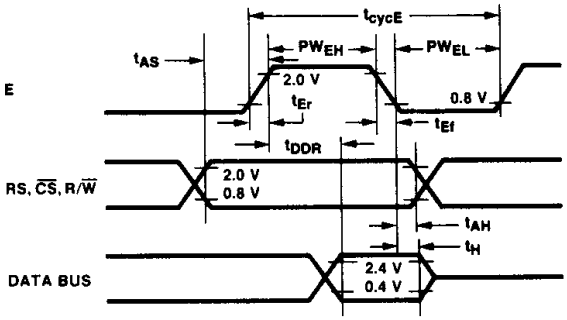



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**Fig. 8 Bus Write Timing Characteristics (Write Information into ACIA)**

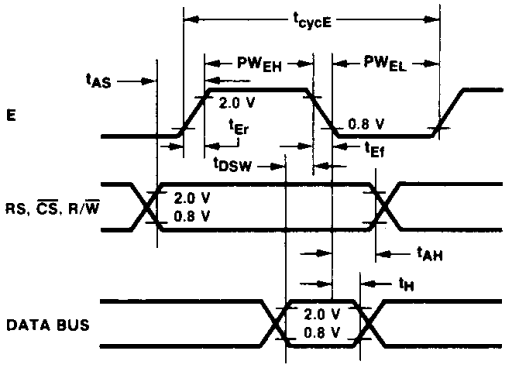
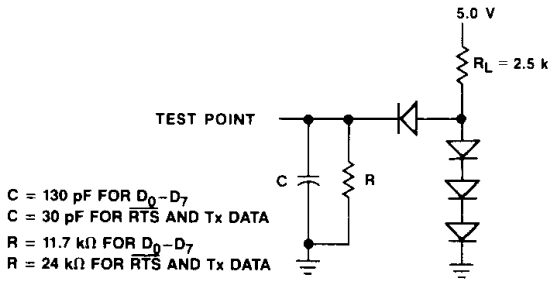
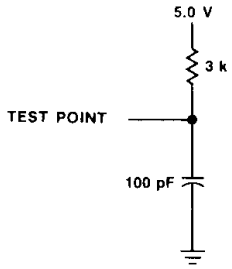



**Fig. 9 Bus Timing Test Loads**

**Load A ($D_0$–$D_7$, $\overline{RTS}$, Tx DATA)**




**Load B ($\overline{IRQ}$ Only)**



## Ordering Information

| Speed | Order Code | Temperature Range |
|---|---|---|
| 1.0 MHz | F6850P,S | 0°C to 70°C |
| | F6850CP,CS | −40°C to +85°C |
| | F6850DL | −55°C to +85°C |
| | F6850DM | −55°C to +125°C |
| 1.5 MHz | F68A50P,S | 0°C to +70°C |
| | F68A50CP,CS | −40°C to +85°C |
| 2.0 MHz | F68B50DM | −55°C to +125°C |
| | F68B50P,S | 0°C to +70°C |

P = Plastic package, S = Ceramic package

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