Dual High-Efficiency 1.5MHz 1A PWM Step-Down DC-DC Converter

DESCRIPTION

The EUP3020 contains two independent 1.5MHz constant frequency, current mode, PWM step-down converters. Each converter integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. The EUP3020 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery. Each converter can supply 1A of load current from a 2.5V to 5.5V input voltage. The output voltage can be regulated as low as 0.6V. The EUP3020 can also run at 100% duty cycle for low dropout applications.

EUP3020 is available in an adjustable output or fixed output 1.2V, 1.8V and 3.3V.

FEATURES

- Up to 96% Efficiency
- 1.5MHz Constant Switching Frequency
- 1A Load Current on Each Channel
- 2.5V to 5.5V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Operation
- Short Circuit Protection
- Thermal Fault Protection
- <1μA Shutdown Current
- Soft Start Function
- Space Saving 3mm×3mm 12-Pin TDFN Package
- RoHS Compliant and 100% Lead(Pb)-Free

APPLICATIONS

- Cellular and Smart Phones
- Microprocessors and DSP Core Supplies
- PDAs and Portable Media Players
- Wireless and DSL Modems
- Digital Still and Video Cameras

Typical Application Circuit

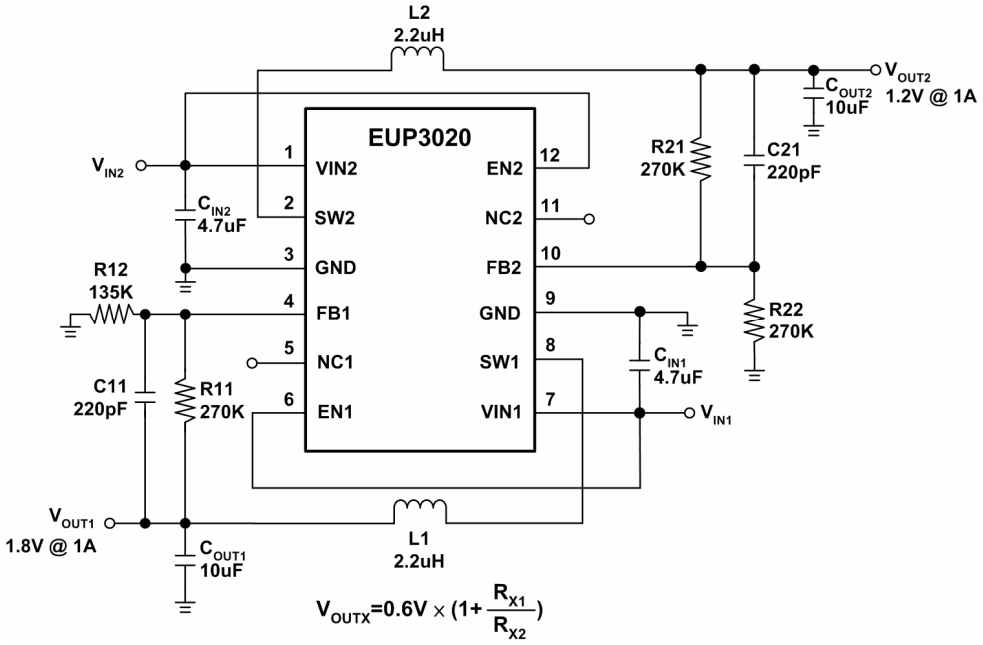


Figure 1. Adjustable Output Regulators

Typical Application Circuit (continued)

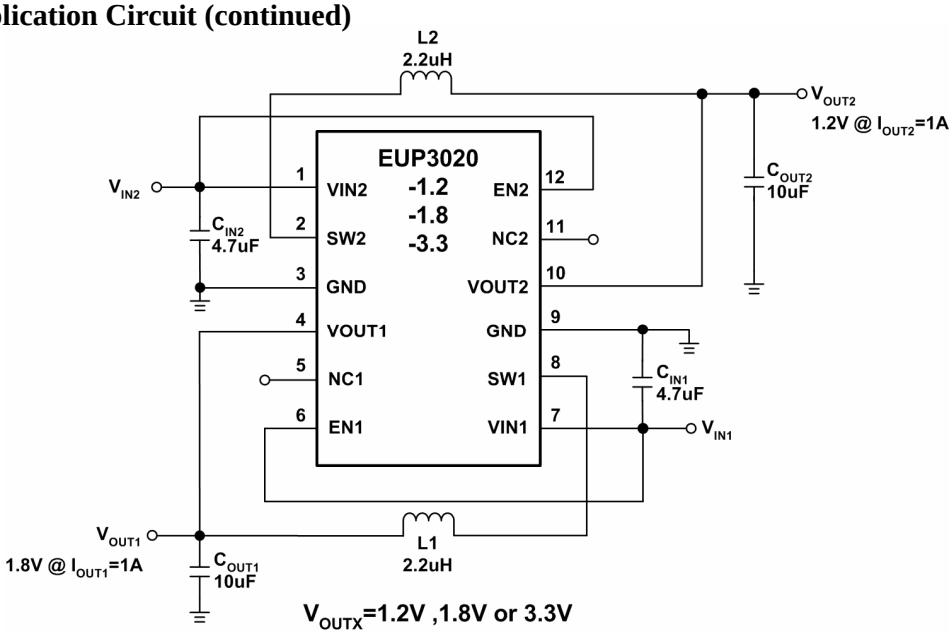
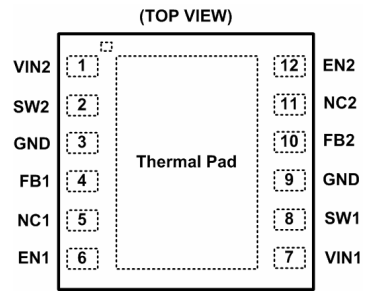
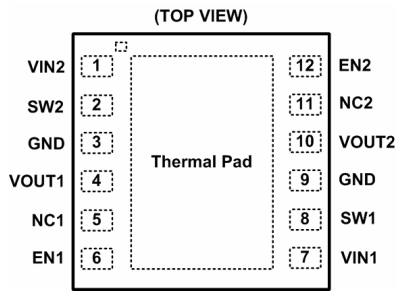


Figure 2. Fixed Output Regulators

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
TDFN-12 ADJ Voltage		TDFN-12 Fixed Voltage	

Pin Description

PIN	Pin	DESCRIPTION
VIN2	1	Power Input of Channel 2.
SW2	2	Pin for Switching of Channel 2.
GND	3,9	Ground.
FB1/VOUT1	4	Feedback/Output Voltage Pin of Channel 1.
NC1,NC2	5,11	No Connection or Connect to V_{IN}.
EN1	6	Chip Enable of Channel 1 (Active High).$V_{EN1} \leq V_{IN1}$.
VIN1	7	Power Input of Channel 1.
SW1	8	Pin for Switching of Channel1.
FB2/VOUT2	10	Feedback/Output Voltage Pin of Channel 2.
EN2	12	Chip Enable of Channel 2 (Active High).$V_{EN2} \leq V_{IN2}$.

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUP3020-1.8/1.2JIR1	TDFN-12	xxxxx P3020 BK	-40 °C to +85°C
EUP3020-3.3/1.2JIR1	TDFN-12	xxxxx P3020 BN	-40 °C to +85°C
EUP3020-3.3/1.8JIR1	TDFN-12	xxxxx P3020 BL	-40 °C to +85°C
EUP3020JIR1	TDFN-12	xxxxx P3020 1A	-40 °C to +85°C

EUP3020-☐☐/☐☐ ☐ ☐ ☐ ☐

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: TDFN

Output Voltage Option
*EUP3020-VOUT1/VOUT2 JIR1
Blank: Adjustable

Block Diagram

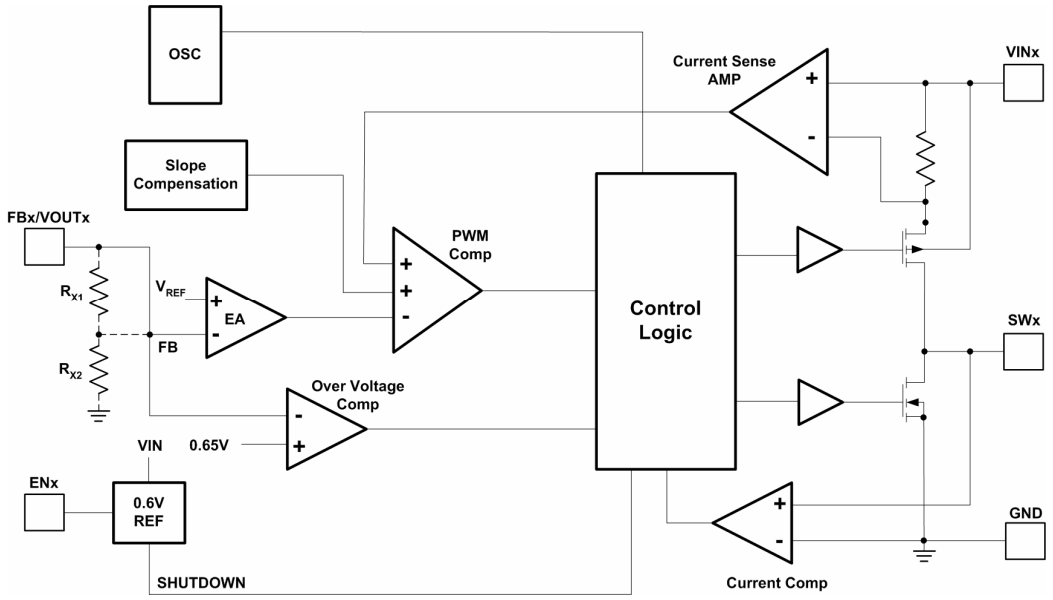


Figure 3.

Absolute Maximum Ratings (1)

- $V_{IN1/IN2}$ to GND ---------- -0.3V to 6V
- $V_{SW1/SW2}$ to GND ---------- -0.3V to V_{IN}+0.3V
- $V_{FB1/FB2}$,$V_{EN1/EN2}$ to GND ---------- -0.3V to VIN
- Junction Temperature ---------- 125°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp (Soldering, 10sec) ---------- 260°C

Recommended Operating Conditions (2)

- Supply Voltage, $V_{IN1/IN2}$ ---------- 2.5V to 5.5V
- Output Voltage, $V_{OUT1/OUT2}$ ---------- 0.6V to 5V
- Operating Temperature ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

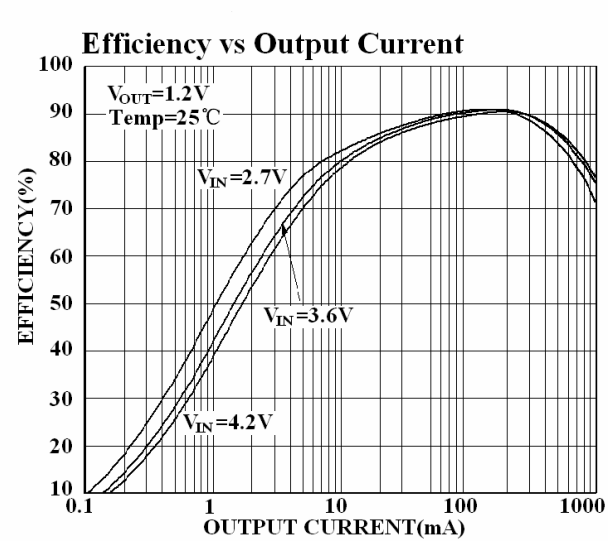
Electrical Characteristics

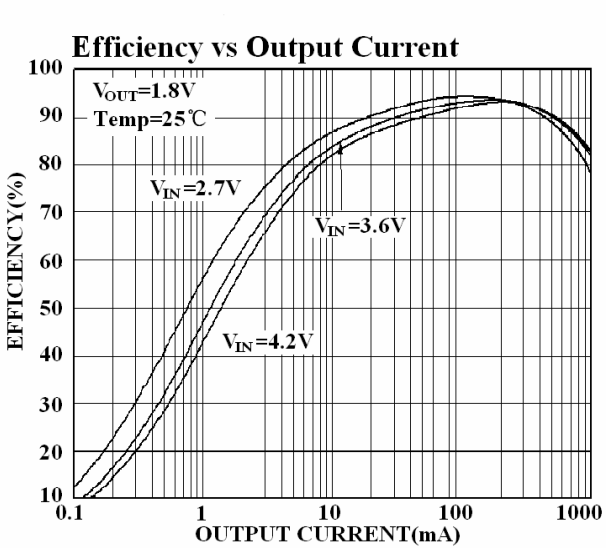
$V_{IN1/IN2}$ =$V_{EN1/EN2}$ =3.6V, T_A=+25°C, Unless otherwise specified.

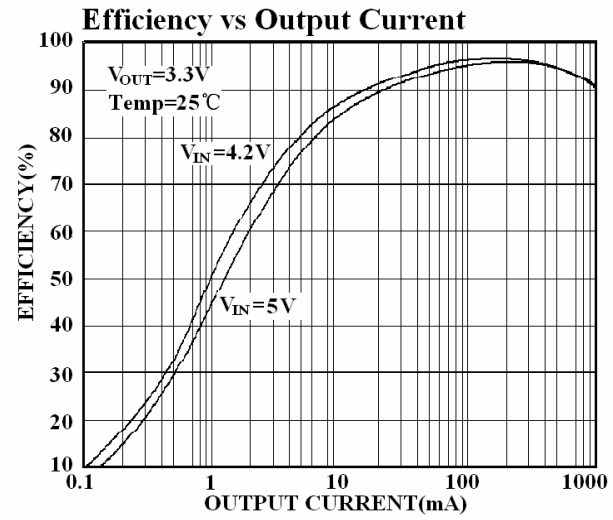
Symbol	Parameter	Conditions	EUP3020			Unit
			Min	Typ	Max.	
V_{IN}	Input Voltage Range		2.5		5.5	V
I_{FB}	Feedback Current			±30		nA
I_Q	Each converter Supply Current	$V_{FB1/FB2}$=0.5V, SW1/SW2 Open		270	370	μA
I_{SHDN}	Each converter Shutdown Current	$V_{EN1/EN2}$=0V, $V_{IN1/IN2}$=4.2V			1	μA
I_{PK}	Peak Inductor Current	$V_{IN1/IN2}$=3V,$V_{FB1/FB2}$=0.5V	1.2	1.5		A
V_{FB}	Regulator Feedback Voltage (Note 3)	T_A=+25℃	0.588	0.6	0.612	V
		-40℃≤ T_A≤ +85℃	0.585	0.6	0.615	
V_{OUT}	Regulation Output Voltage	I_{OUT}=200mA	-3		3	%
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN}=2.5V to 5.5V, I_{LOAD}=0		0.25	0.4	%/V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN}=2.5V to 5.5V		0.25	0.4	%/V
$\Delta V_{LOADREG}$	Output Voltage Load Regulation	I_{LOAD}=0 to 1A		0.5		%
f_{OSC}	Each converter Oscillator Frequency	$V_{FB1/FB2}$=0.6V	1.2	1.5	1.8	MHz
		$V_{FB1/FB2}$=0		0.7		
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	$I_{SW1/SW2}$=200mA		0.28	0.4	Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	$I_{SW1/SW2}$= -200mA		0.3	0.4	Ω
I_{LSW}	SW Leakage Current	$V_{EN1/EN2}$=0V, $V_{SW1/SW2}$=0 or 5V, $V_{IN1/IN2}$=5V			±1	μA
V_{EN}	EN Threshold	-40℃≤ T_A≤ +85℃	0.3	1.0	1.5	V

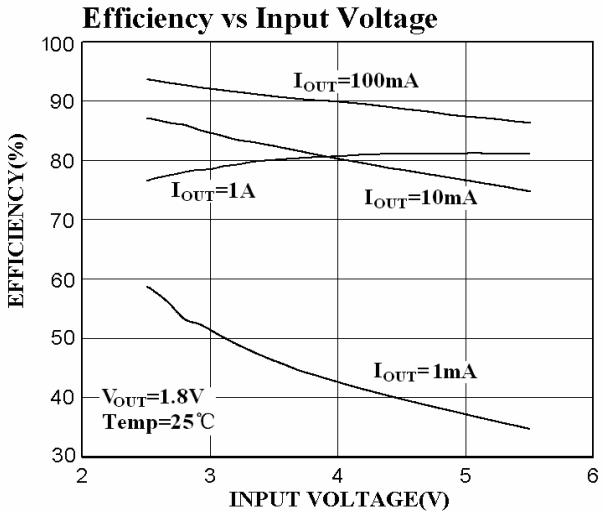
Note (3): The EUP3020 is tested in a proprietary test mode that connects FB1/FB2 to the output of the error amplifier.

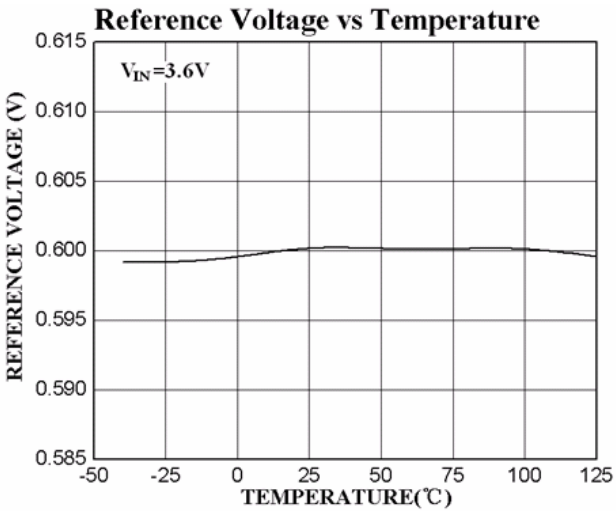
Typical Operating Characteristics

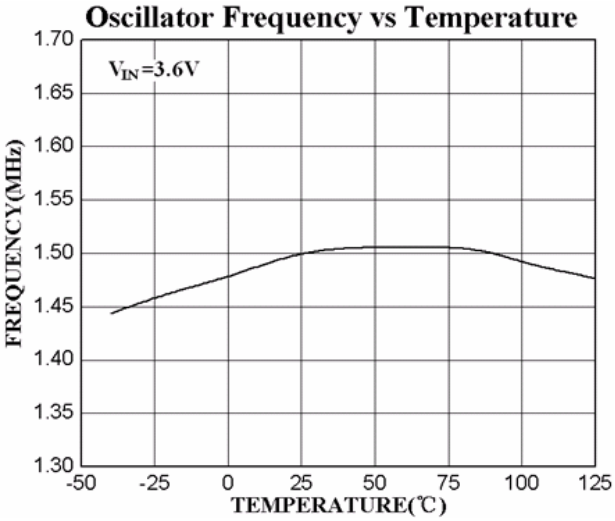


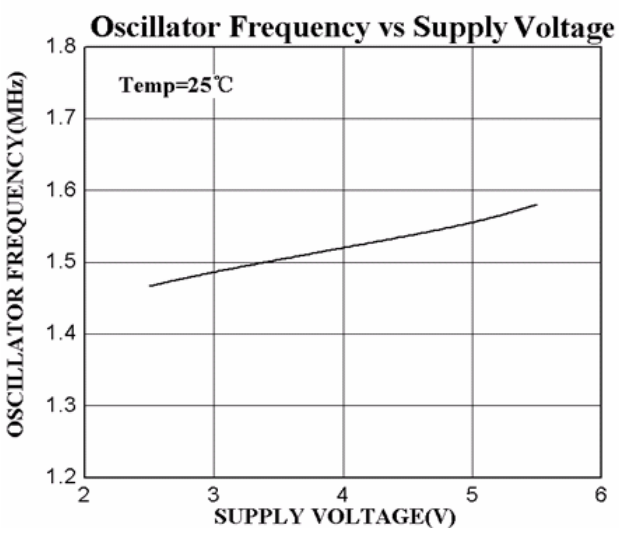


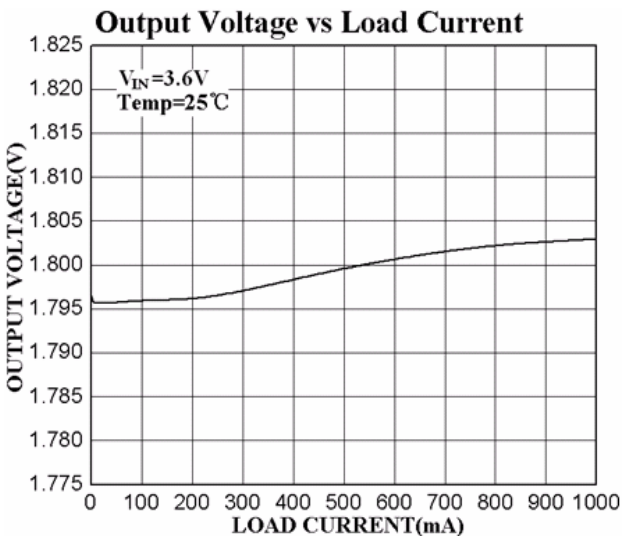


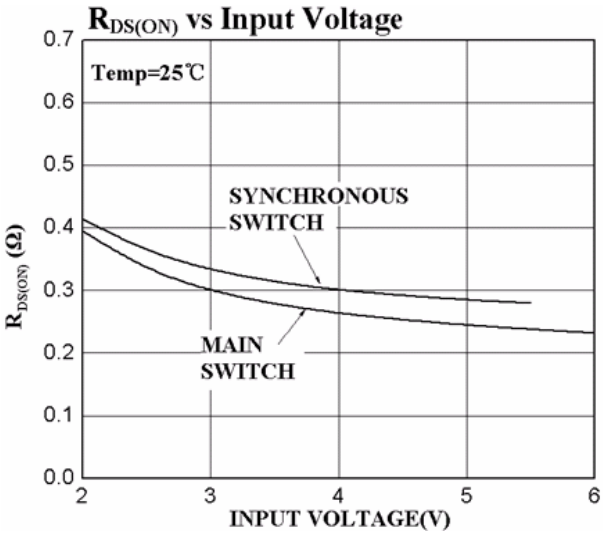


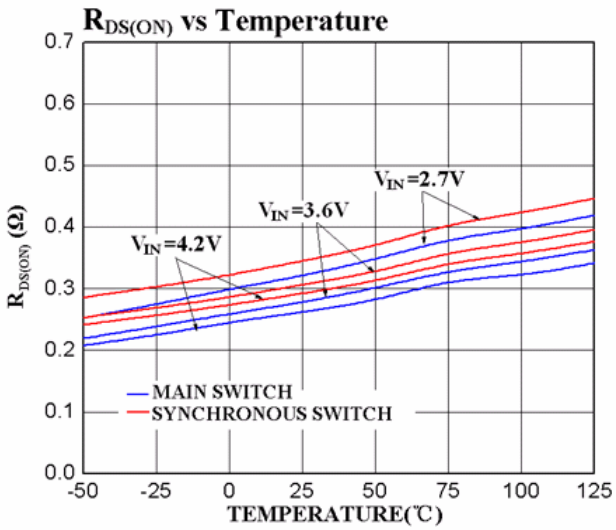


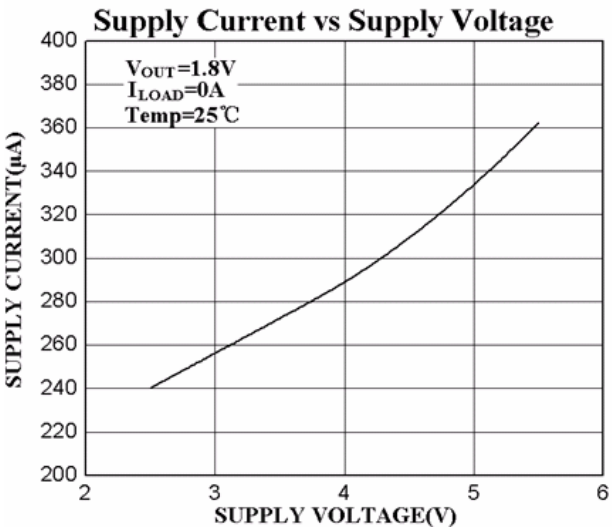


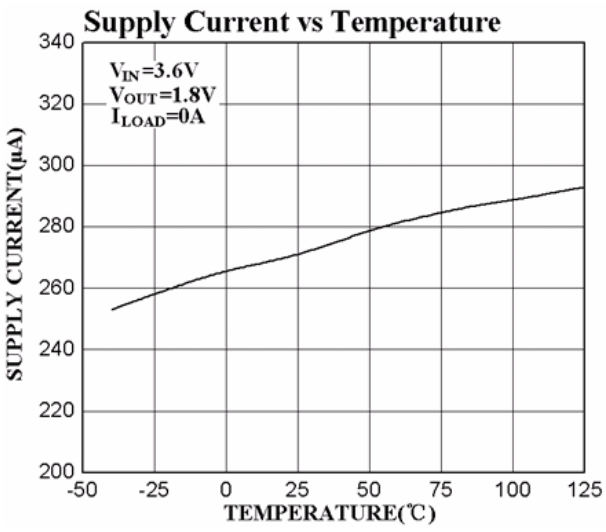




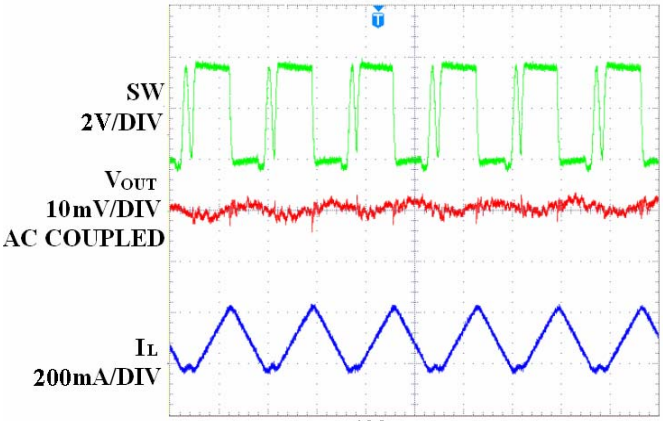






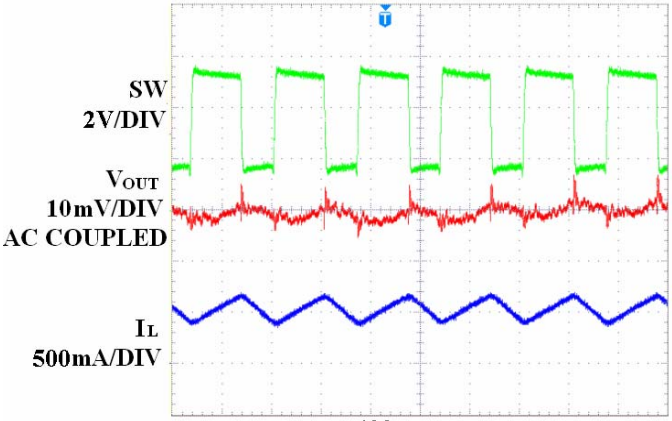


Discontinuous Operation



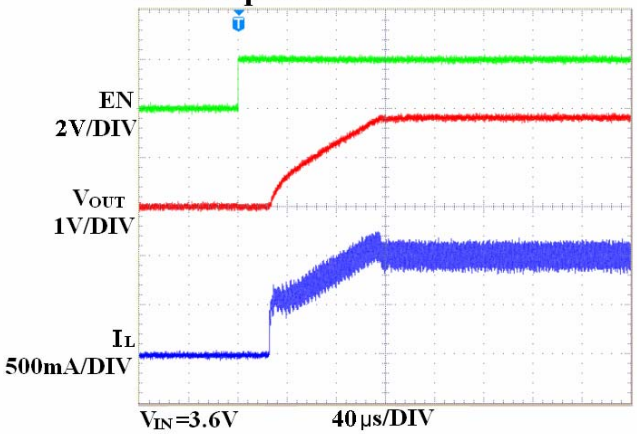
VIN=3.6V 400ns/DIV
VOUT=1.8V
ILOAD=100mA

Normal Operation



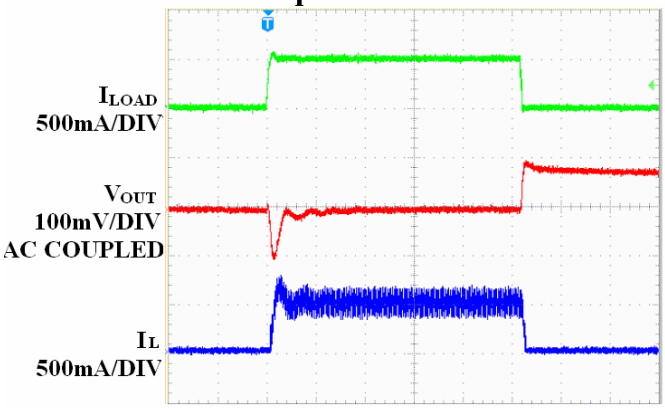
VIN=3.6V 400ns/DIV
VOUT=1.8V
ILOAD=1A

Start-Up from Shutdown



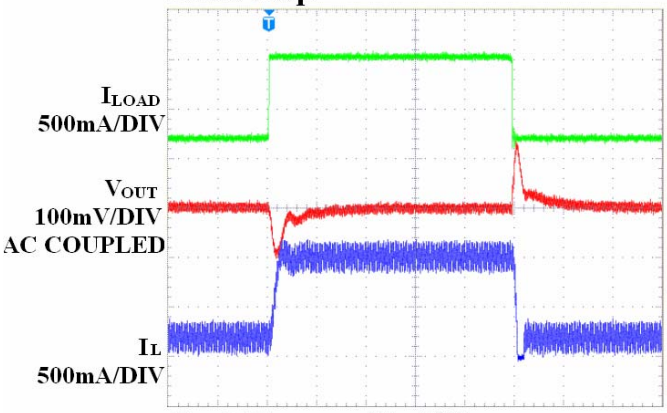
VIN=3.6V 40µs/DIV
VOUT=1.8V
ILOAD=1A(LOAD:1.8Ω RESISTOR)

Load Step



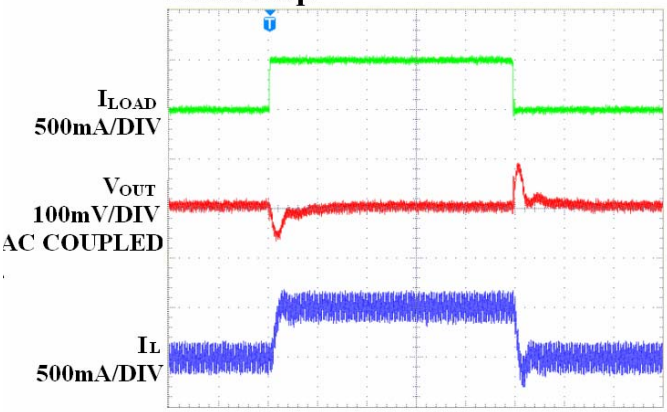
VIN=3.6V 20µs/DIV
VOUT=1.8V
ILOAD=0mA TO 500mA

Load Step



VIN=3.6V 20µs/DIV
VOUT=1.8V
ILOAD=200mA TO 1A

Load Step



VIN=3.6V 20µs/DIV
VOUT=1.8V
ILOAD=500mA TO 1A

Operation

The EUP3020 has dual independent constant frequency current mode PWM step-down converters. The EUP3020 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. The EUP3020 uses resistor dividers to set two output voltages independently from 0.6V to 5V. The device integrates both main switches and synchronous rectifiers, which provides high efficiency and eliminates the need for an external Schottky diode. The EUP3020 can achieve 100% duty cycle. The duty cycle D of each step-down converter is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% = \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time, f_{OSC} is the oscillator frequency (1.5MHz), V_{OUT} is the output voltage and V_{IN} is the input voltage.

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response and protection of the internal main switch and synchronous rectifier. Each channel switches at a constant frequency (1.5MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is reached. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until the next cycle starts or the inductor current starts to reverse.

Dropout Operation

Each channel of the EUP3020 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the PFET current limit. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor.

Short Circuit Protection

The EUP3020 has short circuit protection. When any output is shorted to ground, the own oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

Maximum Load Current

The EUP3020 can operate down to 2.5V input voltage, however the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.

Application Information

Inductor Selection

The output inductor is selected to limit the ripple current to some predetermined value, typically 20%~40% of the full load current at the maximum input voltage. Large value inductors lower ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is ΔI_L=400mA (40% of 1A).

$$\Delta I_L = \frac{1}{(f)(L)} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 1.2A rated inductor should be enough for most applications (1A+200mA). For better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3020. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical value is around 4.7µF.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The output capacitor C_{OUT} has a strong effect on loop stability.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).

ESR is a direct function of the volume of the capacitor; that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \times \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

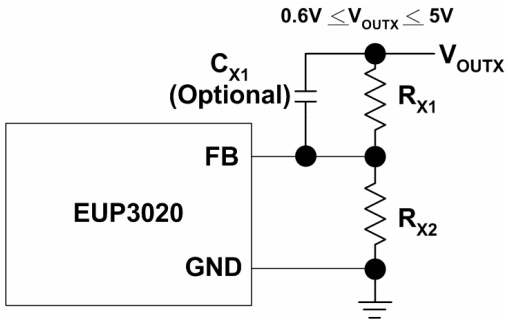
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUTX} = 0.6V \times \left(1 + \frac{R_{X1}}{R_{X2}}\right)$$

For adjustable voltage package, the external resistive divider is connected to the output, allowing remote voltage sensing as shown in below figure.



C_{X1} is a feedforward cap which can speed loop response and reduce output ripple during load transient. Choose C_{X1} value between 220pF and 680pF for most applications.

Thermal Dissipation

To avoid the EUP3020 from exceeding the maximum junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (P_D)(\theta_{JA})$$

Where $P_D = I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator ; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

Where T_A is the ambient temperature.

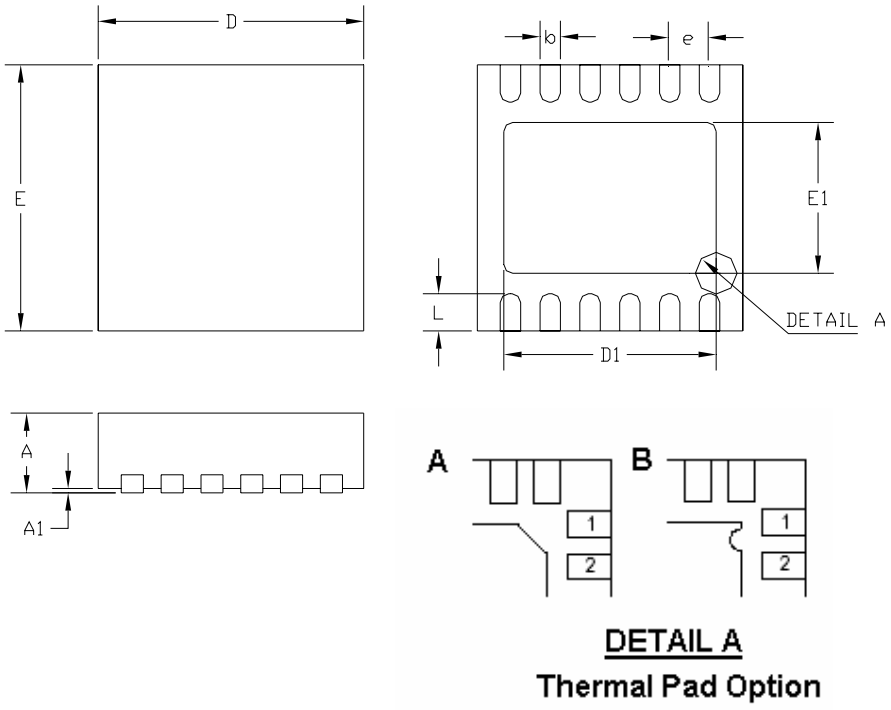
T_J should be below the maximum junction temperature of 125°C.

PC Board Layout

The high current paths (GND1/GND2, VIN1/VIN2 and SW1/SW2) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective VIN and GND pins. For adjustable voltage package, the external feedback resistors shall be placed next to the FB pins. Keep the switching nodes SW1/SW2 short and away from the feedback network.

Packaging Information

TDFN-12



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	2.40		0.094	
E1	1.70		0.067	
e	0.45		0.018	
L	0.30	0.50	0.012	0.020