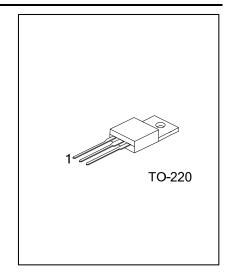
UF1404 Preliminary Power MOSFET

# 162A, 40V N-CHANNEL POWER MOSFET

#### DESCRIPTION

The UTC **UF1404** is a N-channel enhancement power MOSFET using UTC's advanced technology to provide the customers with perfect  $R_{DS(ON)}$  and high switching speed.

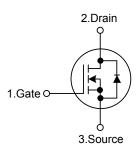
The UTC **UF1404** is suitable for all commercial-industrial applications at power dissipation levels to approximately 50 watts, etc.



### **■ FEATURES**

- \*  $R_{DS(ON)}$ = 4m $\Omega$  @  $V_{GS}$ =10V,  $I_D$ =95A
- \* High Switching Speed

#### ■ SYMBOL



#### **■ ORDERING INFORMATION**

Ordering	Dankana	Pin	Daaldaa				
Lead Free	Halogen Free	Package	1	2	3	Packing	
UF1404L-TA3-T	UF1404G-TA3-T	TO-220	G	D	S	Tube	

Note: Pin Assignment: G: Gate D: Drain S: Source

UF1404L-TA3-T (1)Packing Type (1) T: Tube

(2)Package Type (2) TA3: TO-220

(3) Lead Free (3) G: Halogen Free, L: Lead Free

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# ■ **ABSOLUTE MAXIMUM RATINGS** (T<sub>J</sub>=25°C, unless otherwise specified)

PARAMETER				SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{ extsf{DSS}}$	40	V		
Gate-Source Voltage		$V_{GSS}$	±20	٧		
Drain Current	Continu	Continuous (V <sub>GS</sub> =10V)			162 (Note 5)	Α
	Contini	ious (V <sub>GS</sub> -10V)	T <sub>C</sub> =100°C	I <sub>D</sub>	115 (Note 5)	Α
	Pulsed	(Note 2)	T <sub>C</sub> =25°C	$I_{DM}$	650	Α
Avalanche Current (Note 2)		$I_{AR}$	95	Α		
Avalanche Energy		Single Pulsed	(Note 3)	E <sub>AS</sub>	519	mJ
		Repetitive (Note 2)		$E_{AR}$	20	mJ
Peak Diode Recovery dv/dt (Note 3)		dv/dt	5.0	V/ns		
Power Dissipation (T <sub>C</sub> =25°C)		$P_D$	200	W		
Junction Temperature		$T_J$	+150	°C		
Storage Temperature		$T_{STG}$	-55~+150	Ĉ		

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive rating: pulse width limited by maximum junction temperature
- 3. Starting  $T_J {=} 25^{\circ}C,\, L {=} 0.12mH,\, R_G {=} 25\Omega,\, I_{AS} {=} 95A$
- 4.  $I_{SD} \le 95A$ ,  $di/dt \le 150A/\mu s$ ,  $V_{DD} \le BV_{DSS}$ ,  $T_J \le 175^{\circ}C$
- Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

#### **■ THERMAL CHARACTERISTICS**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62	°C/W
Junction to Case	$\theta_{JC}$	0.625	°C/W

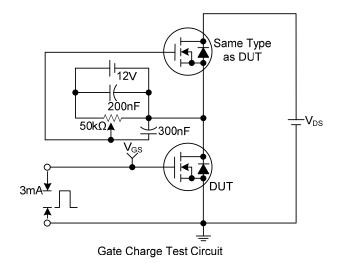
# ■ ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C, unless otherwise specified)

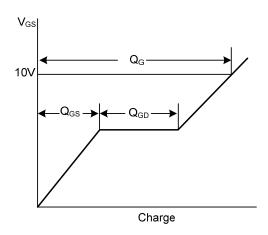
PARAMETER	SYMBOL	MBOL TEST CONDITIONS			TYP	MAX	UNIT
OFF CHARACTERISTICS				,		1	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA		40			V
Breakdown Voltage Temperature Coefficient					0.036		V/°C
Danier Courses I calcare Coursest		V <sub>DS</sub> =40V, V <sub>GS</sub> =0V				20	μΑ
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C				250	μΑ
Coto Source Lookers Current Forward		V <sub>GS</sub> =+20V				+200	nA
Gate- Source Leakage Current Reverse	I <sub>GSS</sub>	V <sub>GS</sub> =-20V				-200	nA
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$ , $I_D=250\mu A$		2.0		4.0	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =95A (Note 2)			3,5	4	mΩ
DYNAMIC PARAMETERS							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz			7.36		nF
Output Capacitance	Coss				1.68		nF
Reverse Transfer Capacitance	C <sub>RSS</sub>				0.24		nF
SWITCHING PARAMETERS							
Total Gate Charge	$Q_{G}$	1 -054 \/ -32\/ \/ -10\	.1		160	200	nC
Gate to Source Charge	$Q_{GS}$	I <sub>D</sub> =95A, V <sub>DS</sub> =32V, V <sub>GS</sub> =10V (Note 2)			35		nC
Gate to Drain Charge	$Q_{GD}$				42	60	nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	$V_{DD}$ =20V, $I_{D}$ =95A, $R_{G}$ =2.5 $\Omega$ , $R_{D}$ =0.21 $\Omega$ (Note 2)			17		ns
Rise Time	$t_R$				140		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>				72		ns
Fall-Time	$t_{\scriptscriptstyle{F}}$				26		ns
SOURCE- DRAIN DIODE RATINGS AND C	HARACTERI	STICS					
Internal Drain Inductance	$L_D$	Between lead. 6 mm	D		4.5		nΗ
Internal Source Inductance	L <sub>S</sub>	(0.25in.) from package and center of die contact	G		7.5		nH
Maximum Body-Diode Continuous Current (Note 4)	Is	MOSFET symbol showing	D			162	Α
Maximum Body-Diode Pulsed Current (Note 1)	I <sub>SM</sub>	the integral reverse p-n junction diode.	G			650	Α
Drain-Source Diode Forward Voltage	$V_{SD}$	I <sub>S</sub> =95A, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C (Note 2)				1.3	V
Body Diode Reverse Recovery Time	t <sub>RR</sub>	I <sub>F</sub> =95A, di/dt=100A/μs,			71	110	ns
Body Diode Reverse Recovery Charge	$Q_{RR}$	T <sub>J</sub> =25°C (Note 2)			180	270	μC

Notes: 1. Repetitive rating: pulse width limited by maximum junction temperature

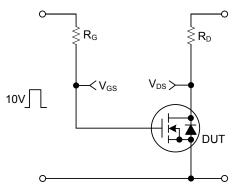
- 2. Pulse width≤300µs, Duty cycle≤2%
- 3.  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- 4. Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

# ■ TEST CIRCUITS AND WAVEFORMS

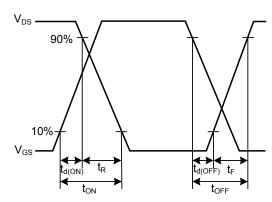




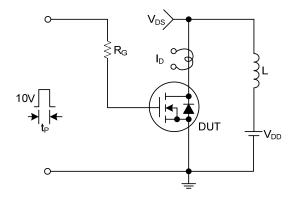
Gate Charge Waveforms



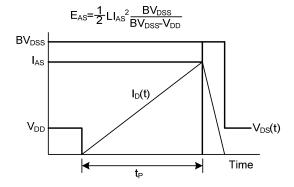




Resistive Switching Waveforms

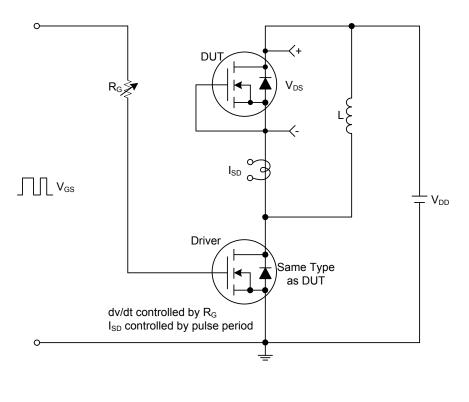


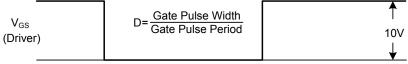
Unclamped Inductive Switching Test Circuit

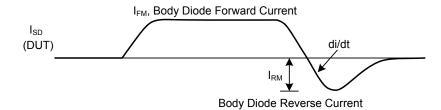


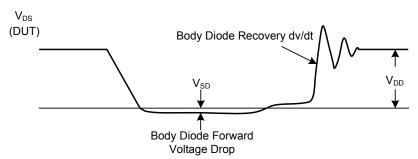
**Unclamped Inductive Switching Waveforms** 

# ■ TEST CIRCUITS AND WAVEFORMS(Cont.)









Peak Diode Recovery dv/dt Test Circuit and Waveforms

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