Z86L88/81/86/87/89/73

IR/LOW-VOLTAGE MICROCONTROLLER

FEATURES

Device	ROM (KB)	RAM* (Bytes)	I/O Lines	Voltage Range
Z86L88	16	237	23	2.0V to 3.9V
Z86L81	24	237	23	2.0V to 3.9V
Z86L86	32	237	23	2.0V to 3.9V
Z86L87	16	236	31	2.0V to 3.9V
Z86L89	24	236	31	2.0V to 3.9V
Z86L73	32	236	31	2.0V to 3.9V

Note: *General-Purpose

- Low Power Consumption - 40 mW (Typical)
- Three Standby Modes
  - STOP
  - HALT
  - Low Voltage
- Special Architecture to Automate Both Generation and Reception of Complex Pulses or Signals:
  - One Programmable 8-Bit Counter/Timer with Two Capture Registers
  - One Programmable 16-Bit Counter/Timer with One 16-Bit Capture Register
  - Programmable Input Glitch Filter for Pulse Reception
- Five Priority Interrupts
  - Three External
  - Two Assigned to Counter/Timers
- Low Voltage Detection and Standby Mode
- Programmable Watch-Dog/Power-On Reset Circuits
- Two Independent Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC (Mask Option), or External Clock Drive
- Mask Selectable 200 kOhms Pull-Ups on Ports 0, 2, 3
  - All Eight Port 2 Bits at One Time or Not
  - Pull-Ups Automatically Disabled Upon Selecting Individual Pins as Outputs.
- Maskable Mouse/Trackball Interface on P00 Through P03.
- 32 kHz Oscillator Mask Option

GENERAL DESCRIPTION

The Z86LXX family of IR (Infrared) CCP™ (Consumer Controller Processor) Controllers are ROM/ROMless-based members of the Z8® single-chip microcontroller family with 256 bytes of internal RAM. The differentiating factor between these devices is the availability of ROM, and package options. For the 40 and 44-pin devices the use of external memory enables these Z8 microcontrollers to be used where code flexibility is required. Zilog's CMOS microcontrollers offers fast executing, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up resistors. The Z86LXX product line offers easy hardware/software system expansion cost-effective and low power consumption.

The Z86LXX architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many

GENERAL DESCRIPTION (Continued)

consumer, automotive, computer peripheral, and battery operated hand-held applications.

There are four basic address spaces available to support a wide range of configurations: Program Memory, Register File, Expanded Register File, and External Memory. The register file is composed of 256 bytes of RAM. It includes four I/O port registers, 16 control and status registers and the rest are General Purpose registers. The Expanded Register File consists of two additional register groups (F and D). External Memory is not available on 28-pin versions.

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86LXX family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes, and two on-board comparators to process analog signals with separate reference voltages (Figure 2).

Notes: All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

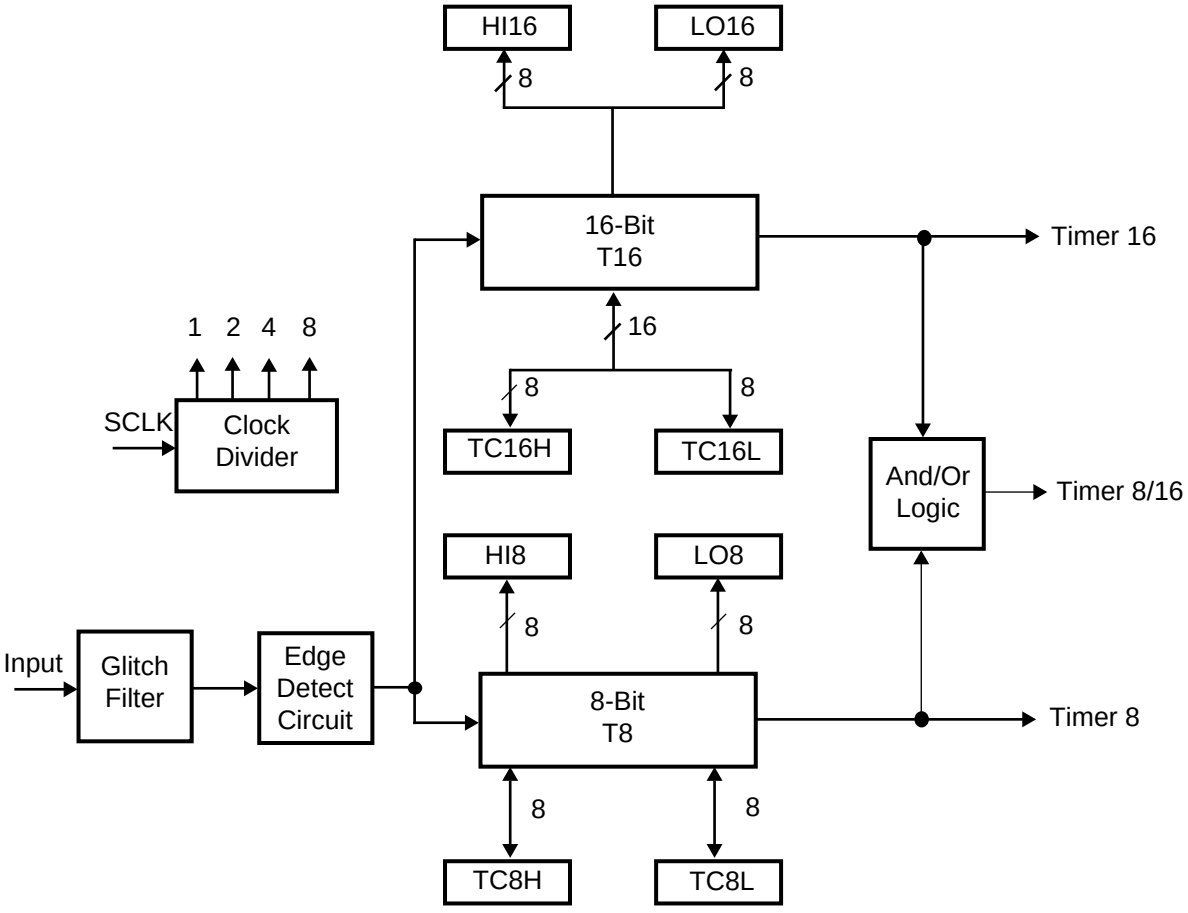


Figure 1. Counter/Timers Diagram

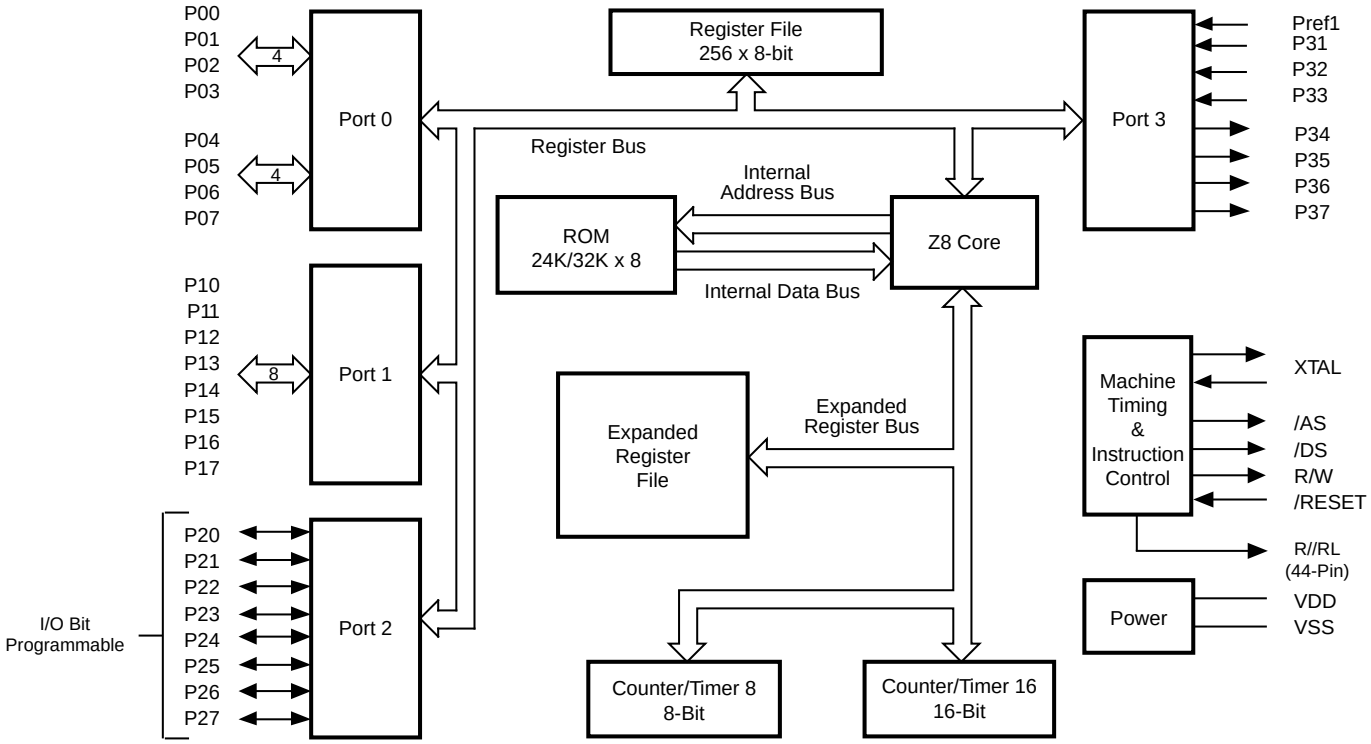


Figure 2. Functional Block Diagram

PIN DESCRIPTION

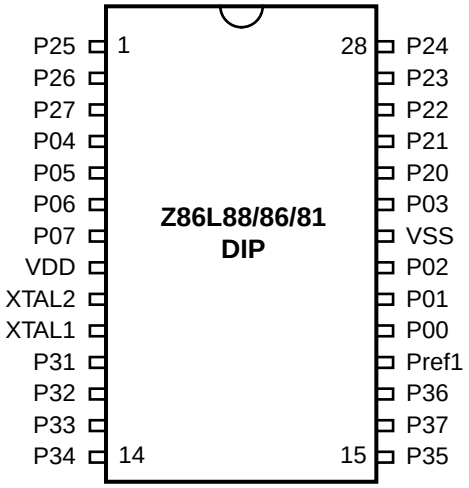


Figure 3. 28-Pin DIP Pin Assignments

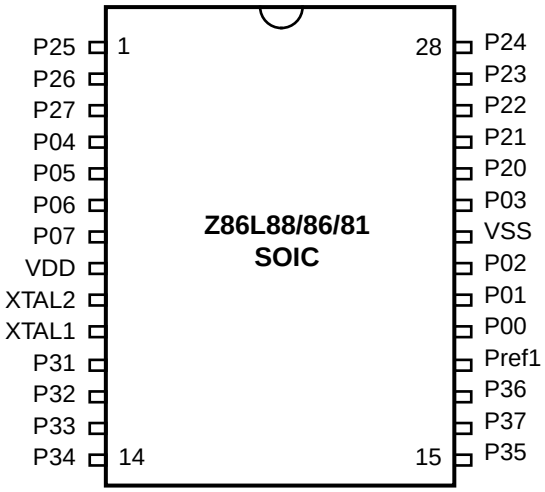


Figure 4. 28-Pin SOIC Pin Assignments

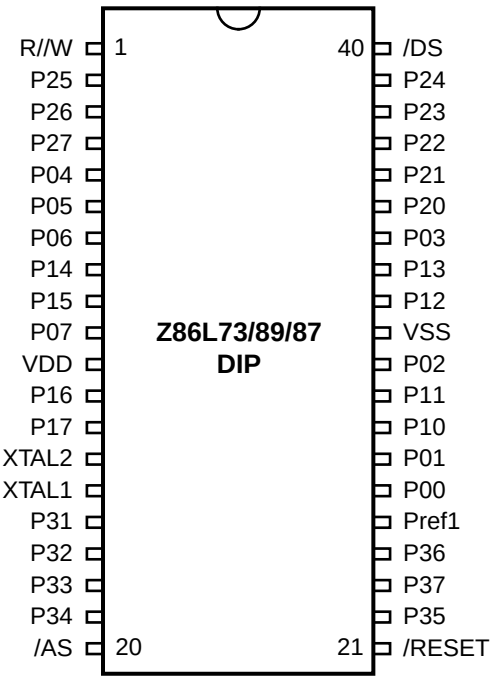


Figure 5. 40-Pin DIP
Pin Assignments

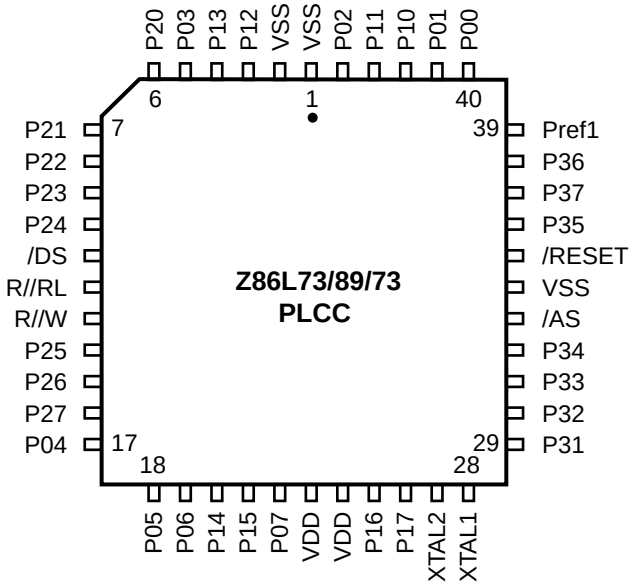


Figure 6. 44-Pin PLCC
Pin Assignments

PIN DESCRIPTION (Continued)

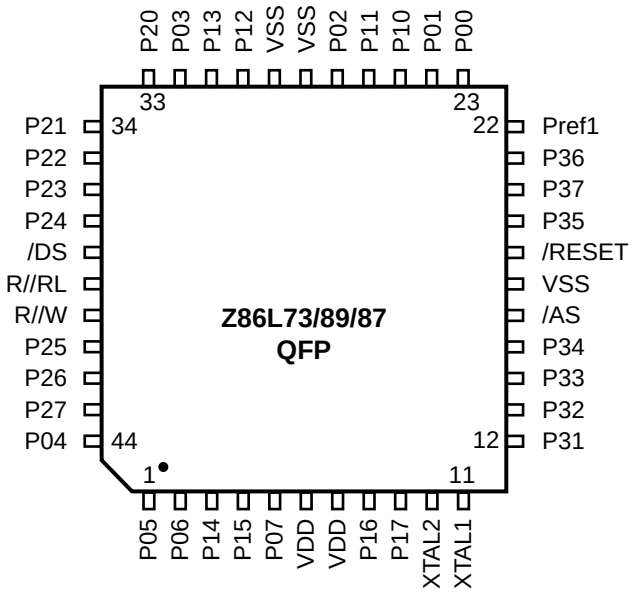


Figure 7. 44-Pin QFP Pin Assignments

Table 1. Pin Identification

40-Pin DIP #	44-Pin PLCC #	44-Pin QFP #	Symbol	Direction	Description
26	40	23	P00	Input/Output	Port 0 is Nibble Programmable.
27	41	24	P01	Input/Output	Port 0 can be configured as
30	44	27	P02	Input/Output	A15-A8 external program
34	5	32	P03	Input/Output	ROM Address Bus.
5	17	44	P04	Input/Output	Port 0 can be configured as a
6	18	1	P05	Input/Output	mouse/trackball input.
7	19	2	P06	Input/Output	
10	22	5	P07	Input/Output	
28	42	25	P10	Input/Output	Port 1 is byte programmable.
29	43	26	P11	Input/Output	Port 1 can be configured as
32	3	30	P12	Input/Output	multiplexed A7-A0/D7-D0
33	4	31	P13	Input/Output	external program ROM
8	20	3	P14	Input/Output	Address/Data Bus.
9	21	4	P15	Input/Output	
12	25	8	P16	Input/Output	
13	26	9	P17	Input/Output	
35	6	33	P20	Input/Output	Port 2 pins are individually
36	7	34	P21	Input/Output	configurable as input or output.
37	8	35	P22	Input/Output	
38	9	36	P23	Input/Output	
39	10	37	P24	Input/Output	
2	14	41	P25	Input/Output	
3	15	42	P26	Input/Output	
4	16	43	P27	Input/Output	
16	29	12	P31	Input	IRQ2/Modulator input
17	30	13	P32	Input	IRQ0
18	31	14	P33	Input	IRQ1
19	32	15	P34	Output	T8 output
22	36	19	P35	Output	T16 output
24	38	21	P36	Output	T8/T16 output
23	37	20	P37	Output	
20	33	16	/AS	Output	Address Strobe
40	11	38	/DS	Output	Data Strobe
1	13	40	R//W	Output	Read/Write
21	35	18	/RESET	Input	Reset
15	28	11	XTAL1	Input	Crystal, Oscillator Clock
14	27	10	XTAL2	Output	Crystal, Oscillator Clock
11	23,24	6,7	V_{DD}		Power Supply
31	1,2, 34	17,28,29	V_{SS}		Ground
25	39	22	Pref1	Input	Comparator 1 Reference
	12	39	R//RL	Input	ROM/ROMless

PIN DESCRIPTION (Continued)

Table 2. Pin Identification

28-Pin DIP & SOIC	Symbol	Direction	Description
19	P00	Input/Output	Port 0 is Nibble Programmable
20	P01	Input/Output	Port 0 can be configured as
21	P02	Input/Output	A15-A8 external program
23	P03	Input/Output	ROM Address Bus.
4	P04	Input/Output	
5	P05	Input/Output	Port 0 can be configured as a mouse/trackball input.
6	P06	Input/Output	
7	P07	Input/Output	
24	P20	Input/Output	Port 2 pins are individually
25	P21	Input/Output	configurable as input or output.
26	P22	Input/Output	
27	P23	Input/Output	
28	P24	Input/Output	
1	P25	Input/Output	
2	P26	Input/Output	
3	P27	Input/Output	
18	Pref1	Input	Analog Ref Input
11	P31	Input	IRQ2/Modulator input
12	P32	Input	IRQ0
13	P33	Input	IRQ1
14	P34	Output	T8 output
15	P35	Output	T16 output
17	P36	Output	T8/T16 output
16	P37	Output	
10	XTAL1	Input	Crystal, Oscillator Clock
9	XTAL2	Output	Crystal, Oscillator Clock
8	V_{DD}		Power Supply
22	V_{SS}		Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp.	–65°	+150°	C
T_A	Oper. Ambient Temp.		†	C

Notes: :
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 8).

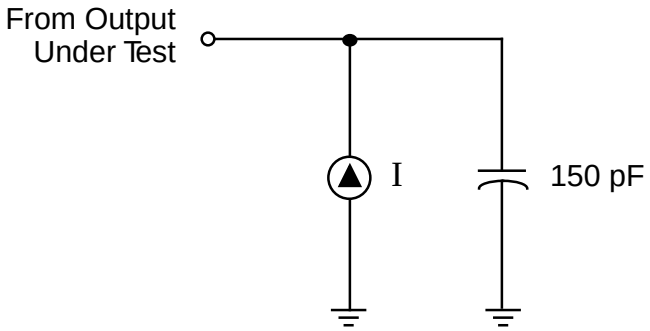


Figure 8. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC CHARACTERISTICS

Preliminary

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes
	Max Input Voltage	2.0V		7		V	I_{IN} <250 µA	
		3.9V		7		V	I_{IN} <250 µA	
V_{CH}	Clock Input High Voltage	2.0V	0.8 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
		3.9V	0.8 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS}– 0.3	0.2 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.7 V_{CC}	V_{CC} + 0.3	0.5V_{CC}	V		
		3.9V	0.7 V_{CC}	V_{CC} + 0.3	0.5V_{CC}	V		
V_{IL}	Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5V_{CC}	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.5V_{CC}	V		
V_{OH1}	Output High Voltage	2.0V	V_{CC} – 0.4		1.7	V	I_{OH} = –0.5 mA	
		3.9V	V_{CC} – 0.4		3.7	V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37,P00, P01)	2.0V	V_{CC} - 0.8			V	I_{OH} = –7 mA	
		3.9V	V_{CC} - 0.8			V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.0V		0.4	0.1	V	I_{OL} = 1.0 mA	
		3.9V		0.4	0.2	V	I_{OL} = 4.0 mA	
V_{OL2*}	Output Low Voltage	2.0V		0.8	0.5	V	I_{OL} = 5.0 mA	
		3.9V		0.8	0.3	V	I_{OL} = 7.0 mA	
V_{OL2}	Output Low Voltage(P36, P37,P00,P01)	2.0V		0.8	0.3	V	I_{OL} = 10 mA	
		3.9V		0.8	0.2	V	I_{OL} = 10 mA	
V_{RH}	Reset Input High Voltage	2.0V	0.8 V_{CC}	V_{CC}	1.5	V		
		3.9V	0.8 V_{CC}	V_{CC}	2.0	V		
V_{RI}	Reset Input Low Voltage	2.0V	V_{SS} – 0.3	0.2 V_{CC}	0.5	V		
		3.9V	V_{SS} – 0.3	0.2 V_{CC}	0.9	V		
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
I_{IL}	Input Leakage	2.0V	-1	1	< 1	µA	V_{IN} = O_V, V_{CC}	
		3.9V	-1	1	< 1	µA	V_{IN} = O_V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1	1	< 1	µA	V_{IN} = O_V, V_{CC}	
		3.9V	–1	1	< 1	µA	V_{IN} = O_V, V_{CC}	
I_{IR}	Reset Input Pull-Up Current	2.0V		–230	-90	µA	V_{IN} = O_V	
		3.9V		–400	–220	µA	V_{IN} = O_V‘	
I_{CC}	Supply Current	2.0V		10	4	mA	@ 8.0 MHz	1,2
		3.9V		15	10	mA	@ 8.0 MHz	1,2
		2.0V		250	100	µA	@ 32 kHz	1,2,7
		3.9V		850	500	µA	@ 32 kHz	1,2,7

Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Typ @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (WDT Off)	2.0V		3	1	mA	HALT Mode $V_{IN} = O_V$, V_{CC} @ 8.0 MHz	1,2
		3.9V		5	4	mA	HALT Mode $V_{IN} = O_V$, V_{CC} @ 8.0 MHz	1,2
		2.0V		2	0.8	mA	Clock Divide-by-16 @ 8.0 MHz	1,2
		3.9V		4	2.5	mA	Clock Divide-by-16 @ 8.0 MHz	1,2
I_{CC2}	Standby Current	2.0V		8	2	µA	STOP Mode $V_{IN} = O_V$, V_{CC} WDT is not Running	3,5
		3.9V		10	3	µA	STOP Mode $V_{IN} = O_V$, V_{CC} WDT is not Running	3,5
		2.0V 3.9V		500 800	310 600	µA µA	STOP Mode $V_{IN} = O_V$, V_{CC} WDT is Running	3,5
T_{POR}	Power-On Reset	2.0V 3.9V	12 5	75 20	18 7	ms ms		
Vram	Static RAM Data Retention Voltage	Vram	0.8		0.5	V		6
V_{LV} (Vbo)	V_{CC} Low Voltage Protection			2.15	1.7	V	8 MHz max Ext. CLK Freq.	4

Notes:	I_{CC1}	Typ	Max	Unit	Frequency
	Crystal/Resonator	3.0 mA	5	mA	8.0 MHz
	External Clock Drive	0.3 mA	5	mA	8.0 MHz

1. All outputs unloaded, inputs at rail.
2. CL1 = CL2 = 100 pF
3. Same as note [4] except inputs at V_{CC}.
4. The V_{LV} increases as the temperature decreases.
5. Oscillator stopped.
6. Oscillator stops when VCC falls below Vlv limit
7. 32 kHz clock driver input.

* All Outputs excluding P00, P01, P36, and P37.

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing Diagram

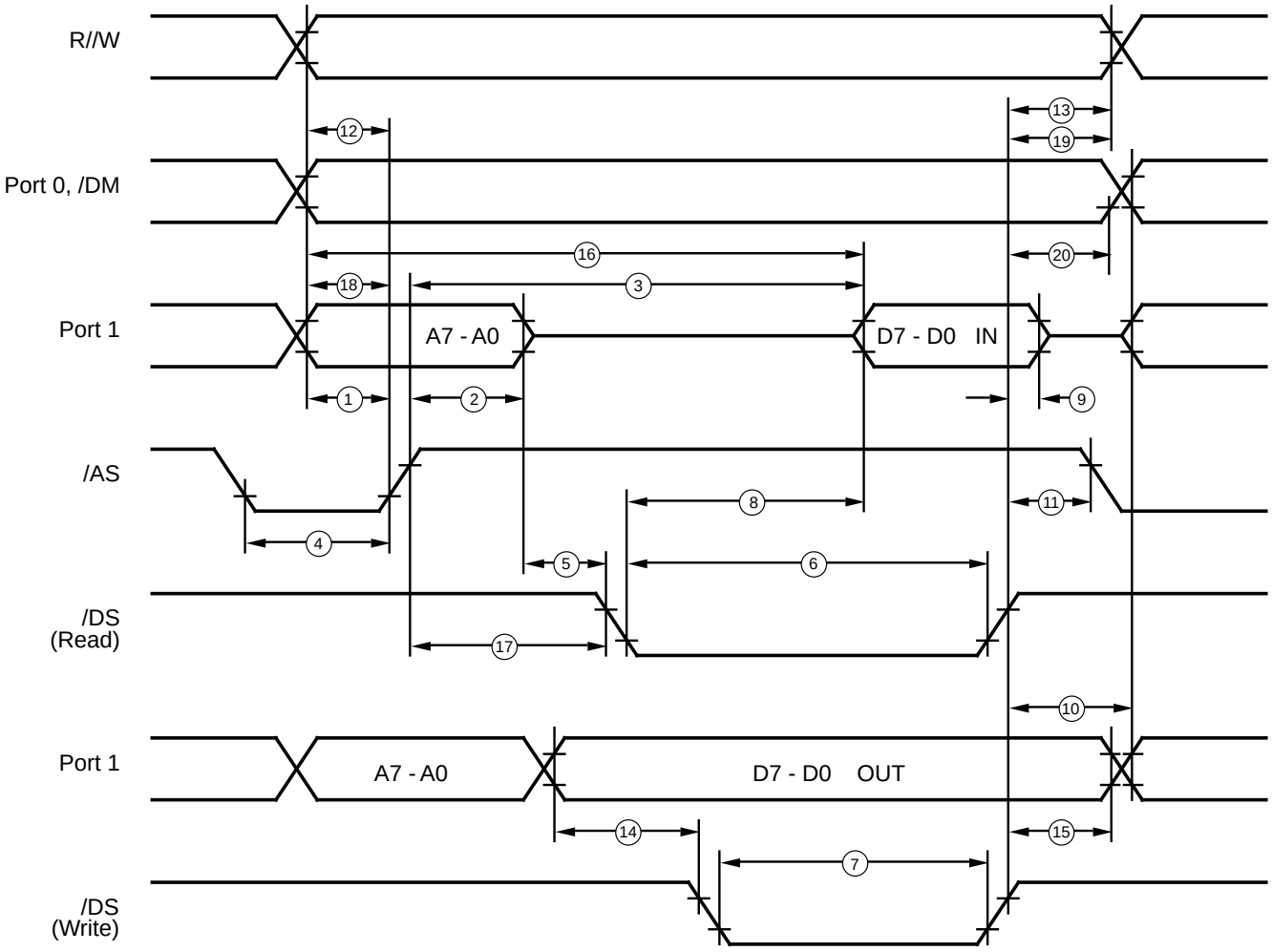


Figure 9. External I/O or Memory Read/Write Timing

AC CHARACTERISTICS

Preliminary

External I/O or Memory Read and Write Timing Table

				T_A = 0°C to +70°C 8.0MHz			
No	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS Rising Delay	2.0V 3.9V	55 55		ns ns	2
2	TdAS(A)	/AS Rising to Address Float Delay	2.0V 3.9V	70 70		ns ns	2 2
3	TdAS(DR)	/AS Rising to Read Data Required Valid	2.0V 3.9V		400 400	ns ns	1,2
4	TwAS	/AS Low Width	2.0V 3.9V	80 80		ns ns	2
5	Td	Address Float to /DS Falling	2.0V 3.9V	0 0		ns ns	
6	TwDSR	/DS (Read) Low Width	2.0V 3.9V	300 300		ns ns	1,2
7	TwDSW	/DS (Write) Low Width	2.0V 3.9V	165 165		ns ns	1,2
8	TdDSR(DR)	/DS Falling to Read Data Required Valid	2.0V 3.9V		260 260	ns ns	1,2
9	ThDR(DS)	Read Data to /DS Rising Hold Time	2.0V 3.9V	0 0		ns ns	2
10	TdDS(A)	/DS Rising to Address Active Delay	2.0V 3.9V	85 95		ns ns	2
11	TdDS(AS)	/DS Rising to /AS Falling Delay	2.0V 3.9V	60 70		ns ns	2
12	TdR/W(AS)	R//W Valid to /AS Rising Delay	2.0V 3.9V	70 70		ns ns	2
13	TdDS(R/W)	/DS Rising to R//W Not Valid	2.0V 3.9V	70 70		ns ns	2
14	TdDW(DSW)	Write Data Valid to /DS Falling (Write) Delay	2.0V 3.9V	80 80		ns ns	2
15	TdDS(DW)	/DS Rising to Write Data Not Valid Delay	2.0V 3.9V	70 80		ns ns	2
16	TdA(DR)	Address Valid to Read Data Required Valid	2.0V 3.9V		475 475	ns ns	1,2
17	TdAS(DS)	/AS Rising to /DS Falling Delay	2.0V 3.9V	100 100		ns ns	2
18	TdDM(AS)	/DM Valid to /AS Falling Delay	2.0V 3.9V	55 55		ns ns	2
19	TdDS(DM)	/DS Rise to /DM Valid Delay	2.0V 3.9V	70 70		ns ns	
20	ThDS(A)	/DS Rise to Address Valid Hold Time	2.0V 3.9V	70 70		ns	

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.

Standard Test Load

All timing references use 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.

AC CHARACTERISTICS

Additional Timing Diagram

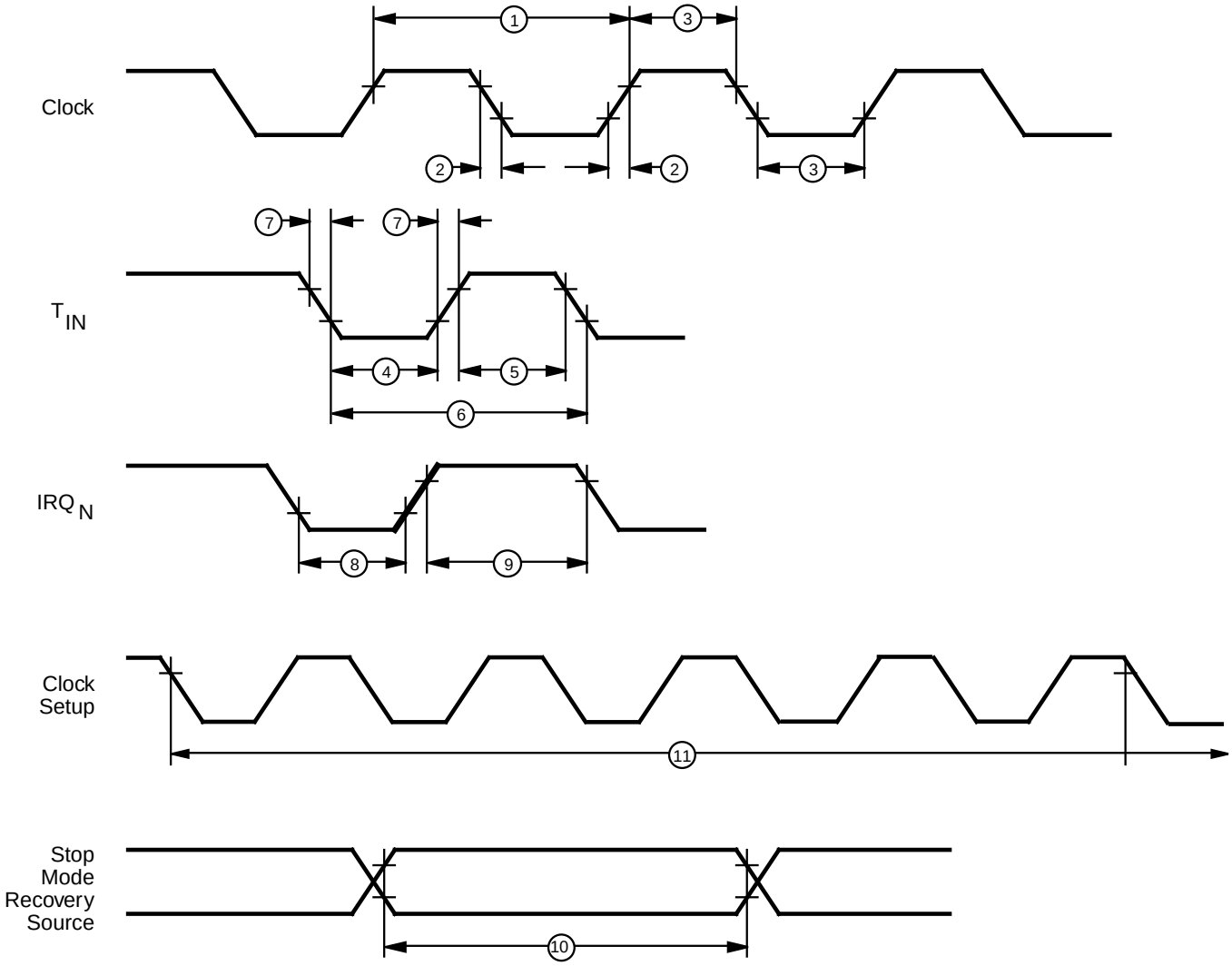


Figure 10. Additional Timing

AC CHARACTERISTICS

Preliminary

Additional Timing Table

				T_A = 0°C to +70°C 8.0MHz			
No	**Sym**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	2.0V	121	DC	ns	1
			3.9V	121	DC	ns	1
2	TrC,TfC	Clock Input Rise	2.0V		25	ns	1
		and Fall Times	3.9V		25	ns	1
3	TwC	Input Clock Width	2.0V	37		ns	1
			3.9V	37		ns	1
4	TwTinL	Timer Input	2.0V	100		ns	1
		Low Width	3.9V	70		ns	1
5	TwTinH	Timer Input	2.0V	3TpC			1
		High Width	3.9V	3TpC			1
6	TpTin	Timer Input	2.0V	8TpC			1
		Period	3.9V	8TpC			1
7	TrTin,TfTin	Timer Input Rise	2.0V		100	ns	1
		and Fall Timers	3.9V		100	ns	1
8A	TwIL	Interrupt Request	2.0V	100		ns	1,2
		Low Time	3.9V	70		ns	1,2
8B	TwIL	Interrupt Request	2.0V	5TpC			1,3
		Low Time	3.9V	5TpC			1,3
9	TwIH	Interrupt Request	2.0V	5TpC			1,2
		Input High Time	3.9V	5TpC			1,2
10	Twsm	Stop-Mode Recovery	2.0V	12		ns	7
		Width Spec	3.9V	12		ns	7
			2.0V	5 TpC		ns	6
			3.9V	5 TpC		ns	6
11	Tost	Oscillator	2.0V		5TpC		4
		Start-Up Time	3.9V		5TpC		4
12	Twdt	Watch-Dog Timer	2.0V	12	75	ms	
		Delay Time (5 ms)	3.9V	5	20	ms	
		(10 ms)	2.0V	25	150	ms	
			3.9V	10	40	ms	
		(20 ms)	2.0V	50	300	ms	
			3.9V	20	80	ms	
		(80 ms)	2.0V	225	1200	ms	
			3.9V	80	320	ms	

Notes:

1. Timing Reference uses 0.9 V_{CC} for a logic 1 and 0.1 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0

AC CHARACTERISTICS

Handshake Timing Diagrams

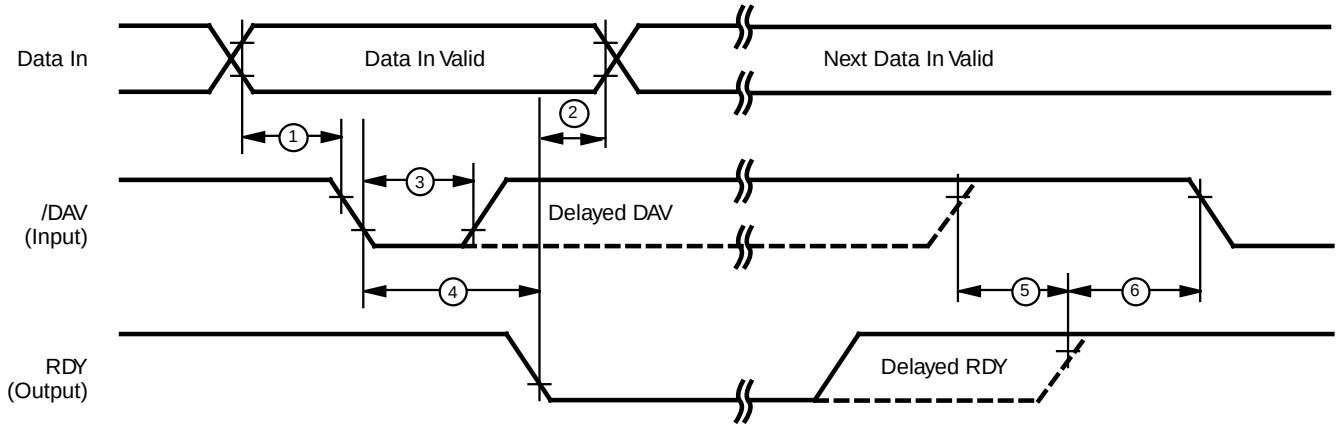


Figure 11. Port Input Handshake Timing

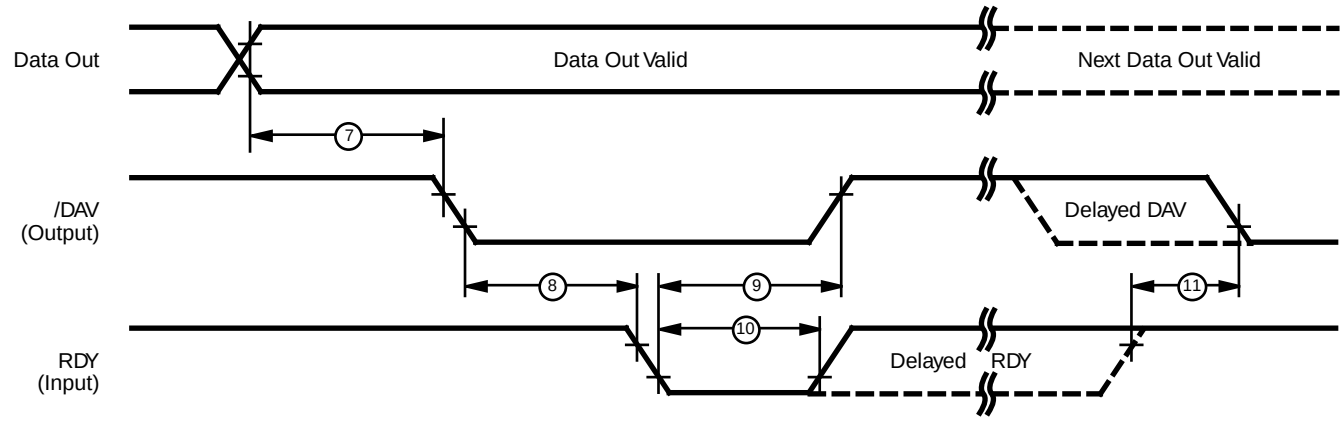


Figure 12. Port Output Handshake Timing

AC CHARACTERISTICS

Preliminary

Handshake Timing Table

No	Sym	Parameter	V_{CC}	T_A = 0°C to +70°C Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	2.0V	0		IN
			3.9V	0		IN
2	ThDI(DAV)	Data In Hold Time	2.0V	0		IN
			3.9V	0		IN
3	TwDAV	Data Available Width	2.0V	155		IN
			3.9V	110		IN
4	TdDAVI(RDY)	DAV Falling to RDY	2.0V		160	IN
		Falling Delay	3.9V		115	IN
5	TdDAVId(RDY)	DAV Rising to RDY	2.0V		120	IN
		Falling Delay	3.9V		80	IN
6	TdRDYO(DAV)	RDY Rising to DAV	2.0V	0		IN
		Falling Delay	3.9V	0		IN
7	TdDO(DAV)	Data Out to DAV	2.0V	63		OUT
		Falling Delay	3.9V	63		OUT
8	TdDAV0(RDY)	DAV Falling to RDY	2.0V	0		OUT
		Falling Delay	3.9V	0		OUT
9	TdRDY0(DAV)	RDY Falling to DAV	2.0V		160	OUT
		Rising Delay	3.9V		115	OUT
10	TwRDY	RDY Width	2.0V	110		OUT
			3.9V	80		OUT
11	TdRDY0d(DAV)	RDY Rising to DAV	2.0V		110	OUT
		Falling Delay	3.9V		80	OUT

PIN FUNCTIONS

/DS (Output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (Output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1 Crystal 1 (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

XTAL2 Crystal 2 (time-based output). This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

R//W Read/Write (output, write Low). The R//W signal is Low when the CCP is writing to the external program or data memory.

R//RL (input). This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8. (Note that, when left unconnected or pulled high to V_{CC}, the part functions normally as a Z8 ROM version.)

Port 0 (P07-P00). Port 0 is an 8-bit, bidirectional, CMOS compatible port. These eight I/O lines are configured under software control as a nibble I/O port, or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 can be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal function is dictated by the I/O direction of the Port 0 upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the high-impedance mode (if selected as an address output) along with Port 1 and the control signals /AS, /DS, and R//W through P3M bits D4 and D3(Figure 13).

A ROM mask option is available to program 0.4 V_{DD} CMOS trip inputs on P00-P03. This allows direct interface to mouse/trackball IR sensors.

An optional 200 kOhms pull-up is available as a mask option on all Port 0 bits with nibble select.

Note: Internal pull-ups are disabled on any given pin or group of port pins when programmed into output mode.

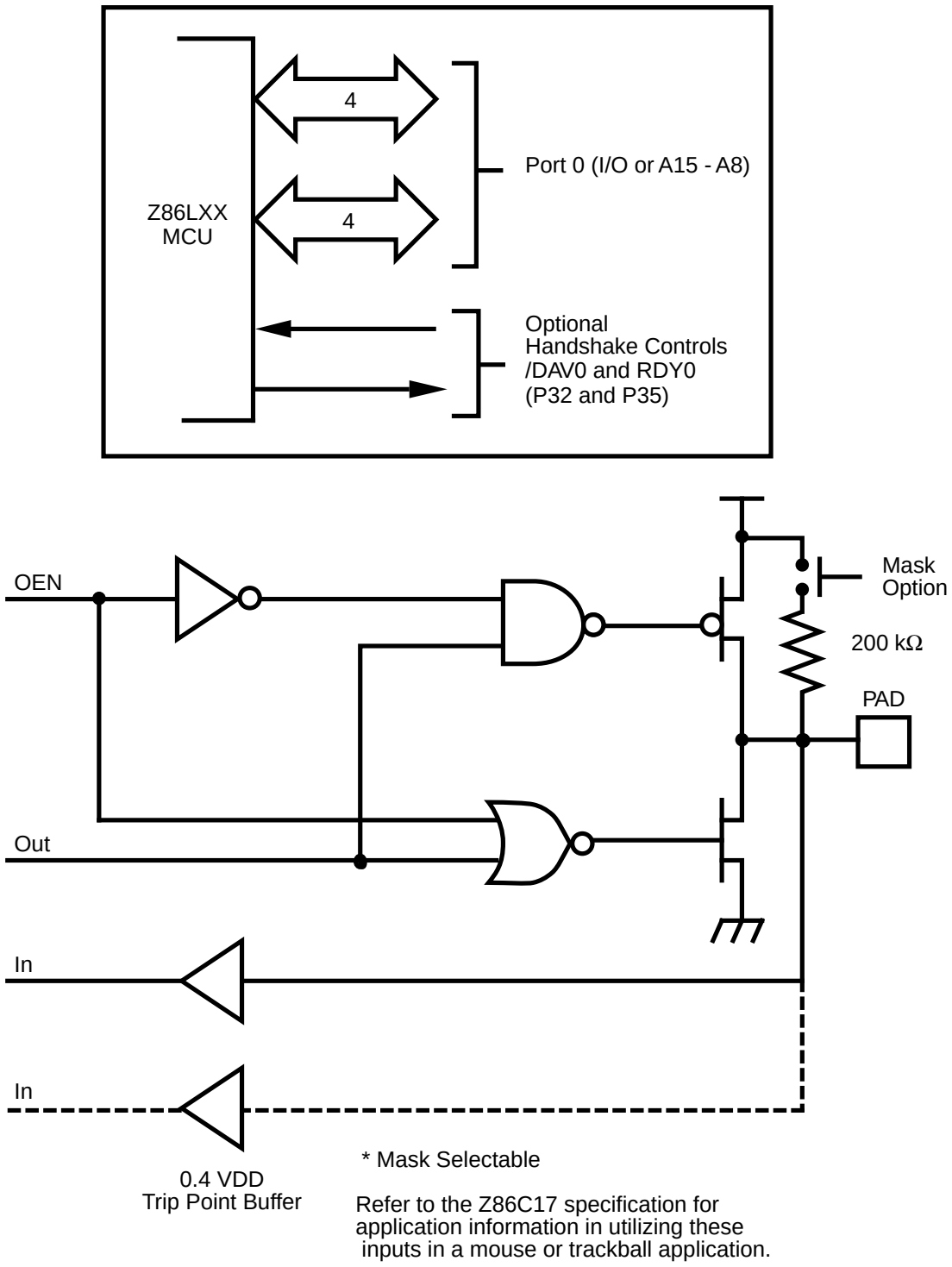


Figure 13. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 1 (P17-P10). Port 1 is a multiplexed Address (A7-A0) and Data (D7-D0), CMOS compatible port. Port 1 is dedicated to the Zilog ZBus®-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (/AS) and Data Strobe (/DS) lines, and by the Read/Write (R//W) and Data Memory (/DM) control lines. Data memory read/write operations are done through this port (Figure 14). If more than 256 external locations are required, Port 0 outputs the additional lines.

Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the Z86LXX to share common resources in multiprocessor and DMA applications. Port1 can also be configured for standard port output mode..

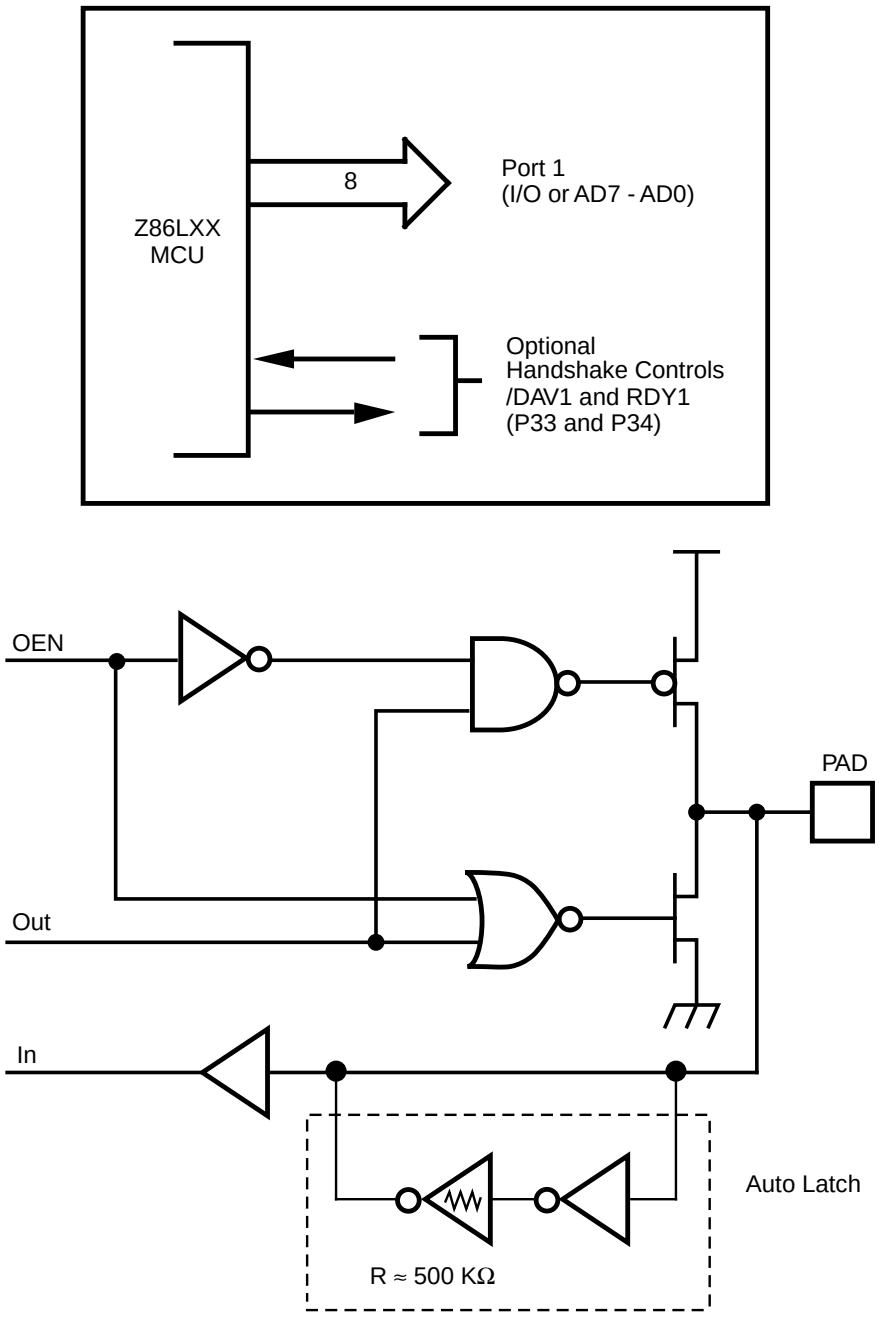


Figure 14. Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 kOhms (±50%) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 may be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2 (Figure 15). The CCP POR resets with the eight bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate which can be used to wake up the part (Figure 41). P20 can be programmed to access the edge selection circuitry (Figure 24).

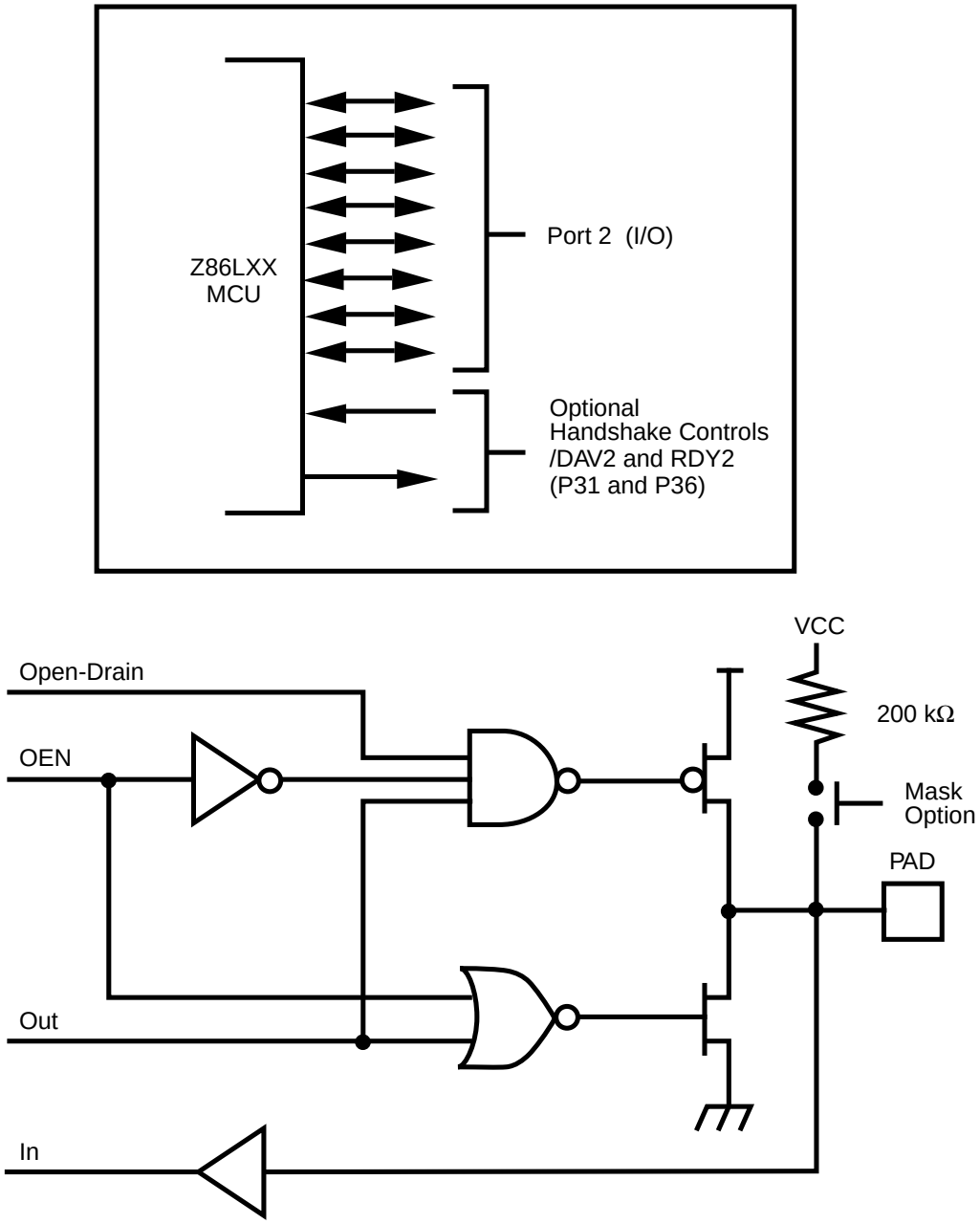


Figure 15. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P31). Port 3 is a 7-bit, CMOS compatible three fixed input and four fixed output port. Port 3 consists of three fixed input (P33-P31) and four fixed output (P37-P34), and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge detection circuit is through P31 or P20 (see CTR1 description). Other edge detect and IRQ modes are described in Tables (3-6). Handshake lines Ports 0, 1, and 2 are available on P31 through P36.

Port 3 provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ2-IRQ0); Data Memory Select (/DM) (Table 3).

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5-D4 of CTR1, bit 0 of CTR0 and bit 0 of CTR2.

Table 3. Pin Assignments

Pin	I/O	C/T	Comp.	Int.	P0 HS	P1 HS	P2 HS	Ext
Pref1	IN		RF1					
P31	IN	IN	AN1	IRQ2			D/R	
P32	IN		AN2	IRQ0	D/R			
P33	IN		RF2	IRQ1		D/R		
P34	OUT	T8	AO1			R/D		DM
P35	OUT	T16			R/D			
P36	OUT	T8/16					R/D	
P37	OUT		AO2					
P20	I/O	IN						

Notes:
D = /DAV
R = RDY
HS = Handshake Signals

Comparator Inputs. In Analog Mode, Port 3 (P31 and P32) have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 is diverted to the SMR sources (excluding P31,P32, and P33) as shown in figure 41. In digital mode, P33 is used as D3 of the Port 3 input register which then generates IRQ1 as shown in Figure 17.

When P31 is used for counter timer input (demodulation mode), input is always taken from the P31 digital input buffer whether or not analog mode is enabled).

Notes: Comparators are powered down by entering STOP mode. For P31-P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs. These may be programmed to be outputted on P34 and P37 through the PCON register (Figures 16,38).

/RESET (Input, active Low). Initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the external reset line should be open-drain in order to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally.

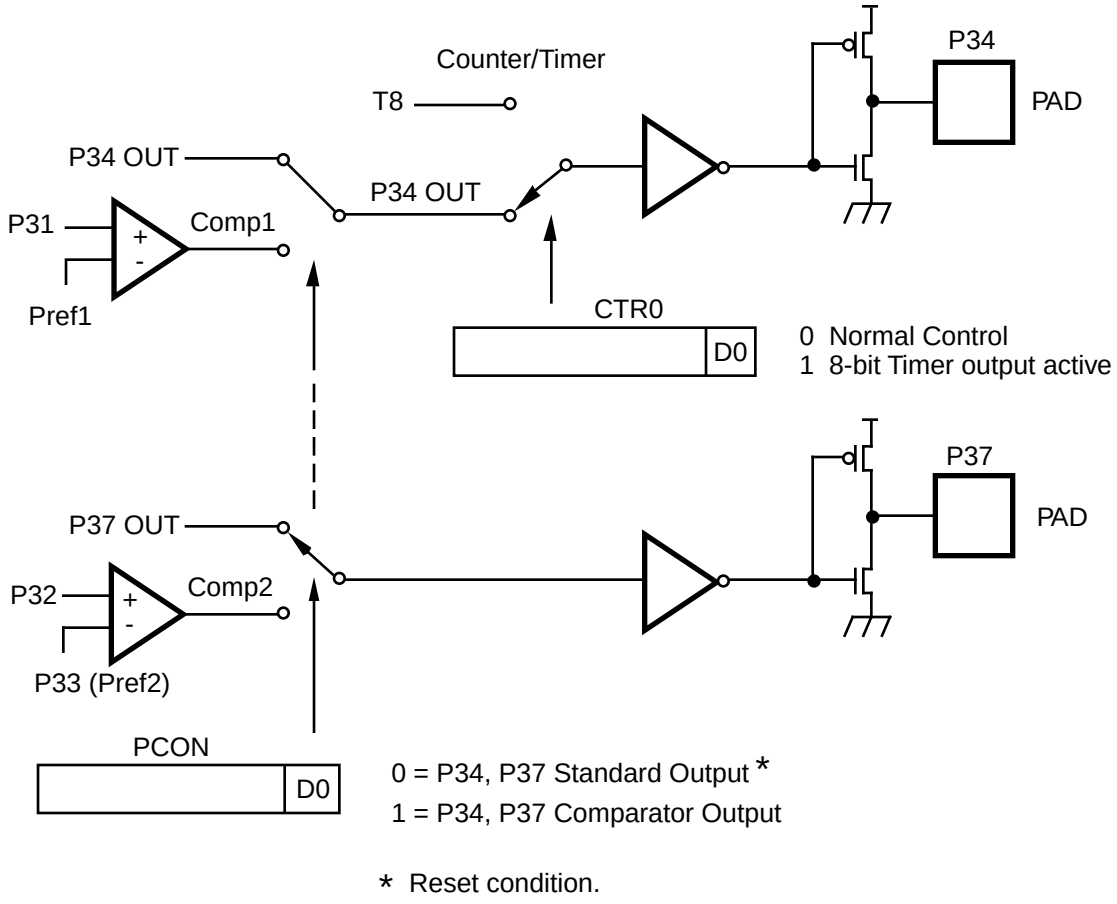


Figure 16. Port 3 Configuration

PIN FUNCTIONS (Continued)

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86LXX is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5-10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms. The Z86LXX does not reset WDTMR, SMR, P2M, or P3M registers on a Stop-Mode Recovery operation. The output states of Port3 and Port2 are also un-affected by a Stop-Mode recovery.

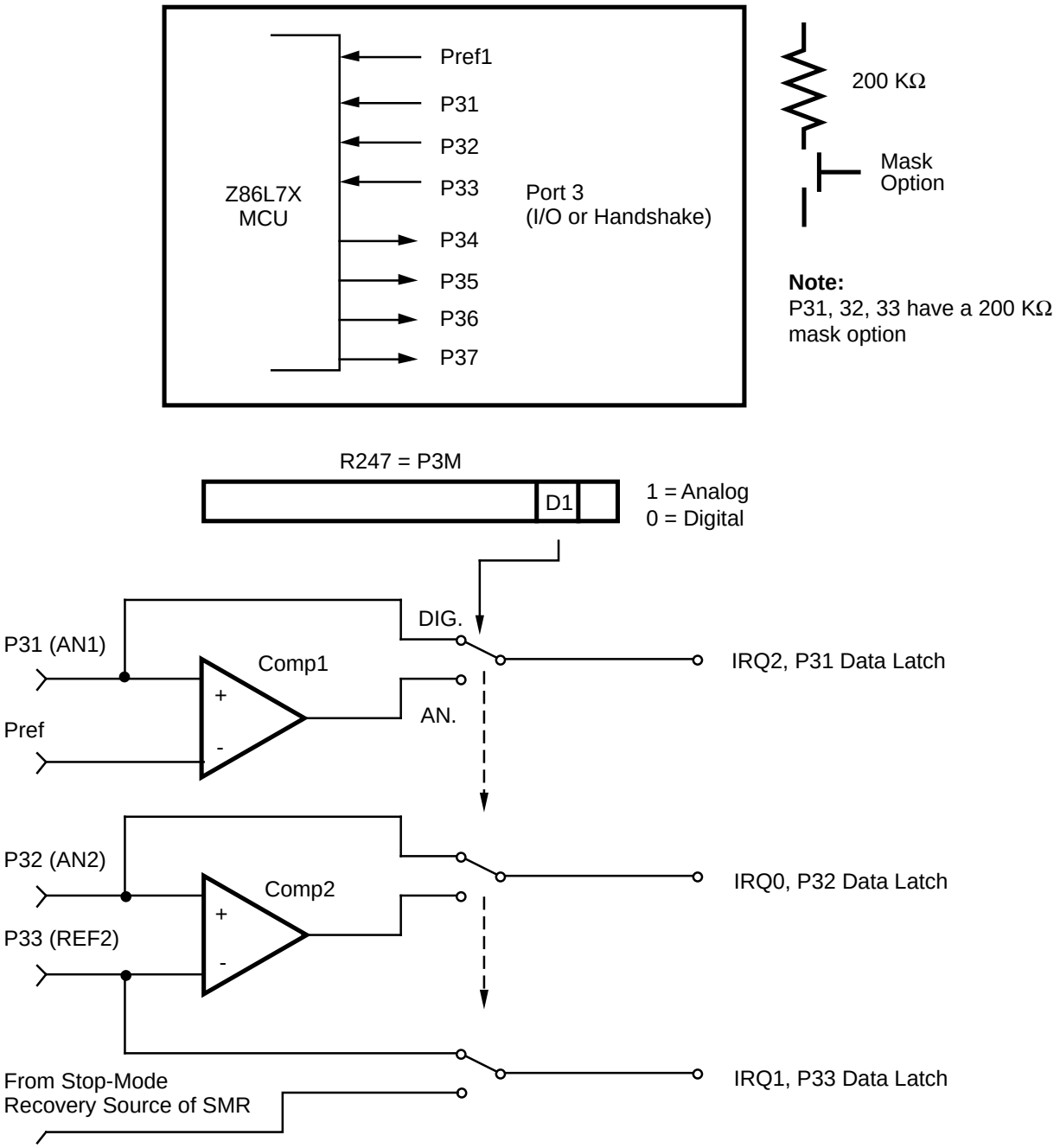


Figure 17. Port 3 Configuration

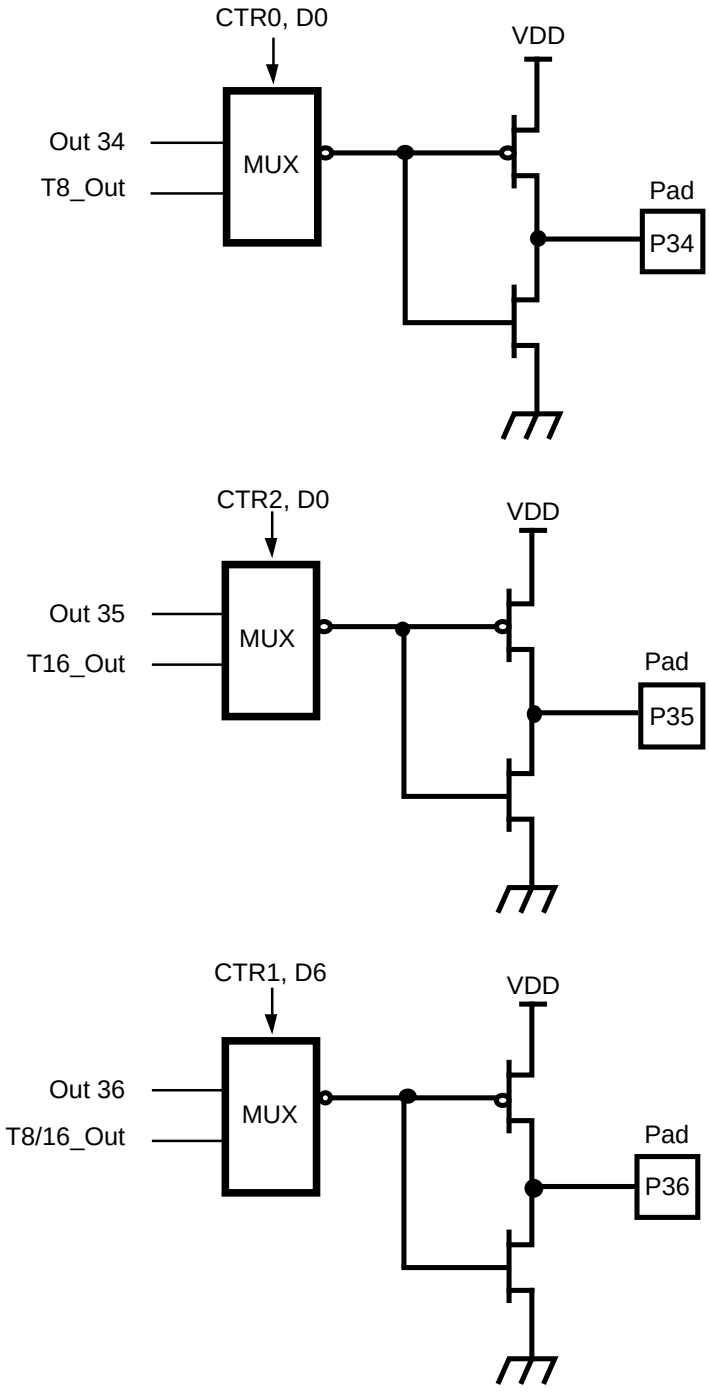


Figure 18. Port 3 Counter Timer Output Configuration

FUNCTIONAL DESCRIPTION

The Z86LXX family of IR CCP incorporates special functions to enhance the Z8's functionality in consumer and battery operated applications.

Program Memory. The Z86LXX family addresses 16/24/32 Kbytes of internal program memory. The first twelve bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors which correspond to the five available interrupts. In all cases, at addresses 32K and greater, external program memory fetches will be executed (provided proper A/D port mode register settings). Refer to external memory timing specifications. In Romless mode, program memory fetches begin at address 000Ch and data memory fetches begin at address 0000h.

RAM. The Z86LXX devices all have 256 bytes of RAM which make up the Register file.

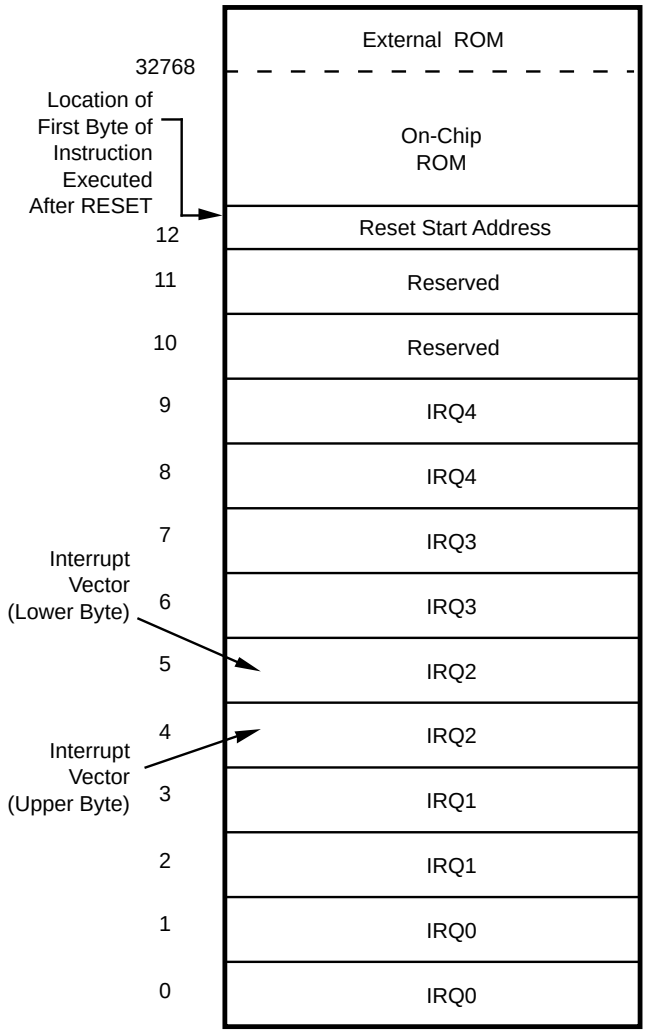


Figure 19. Program Memory Map(32K ROM)

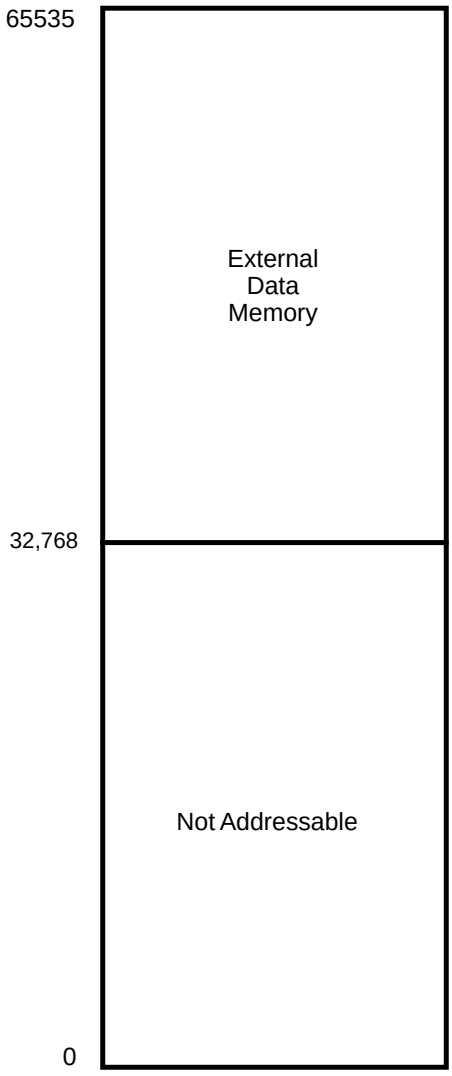


Figure 20. External Memory Map

External Memory (/DM). The Z86LXX addresses up to 32 Kbytes of external memory beginning at address 32768 (Figure 20). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory.

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 banks of 16 registers per bank. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of register RP select the working register group. Bits 3-0 of register RP select the expanded register file bank. Note that expanded register bank is also referred to as expanded register group (Figure 21).

The upper nibble of the register pointer (Figure 23) selects which working register group of 16 bytes in the register file, out of the possible 256, will be accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86LXX family, banks 0, F, and D are implemented. A 0h in the lower nibble will allow the normal register file (bank 0) to be addressed, but any other value from 1h to Fh will exchange the lower 16 registers to an expanded register bank.

For example:

Z86L73: (See Figure 21)

R253 RP = 00h
R0 = Port 0
R1 = Port 1
R2 = Port 2
R3 = Port 3

But if:

R253 RP = 0Dh
R0 = CTRL0
R1 = CTRL1
R2 = CTRL2
R3 = Reserved

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

LD RP, #0Dh Select ERF D for access to bank D (working register group 0)

LD R0,#xx load CTRL0

LD 1, #xx load CTRL1

LD R1, 2 CTRL2 → CTRL1

LD RP, #7Dh Select expanded register bank D and working register group 7 of bank 0 for access .

LD 71h, 2 CTRL2 → register 71h

LD R1, 2 CTRL2 → register 71h

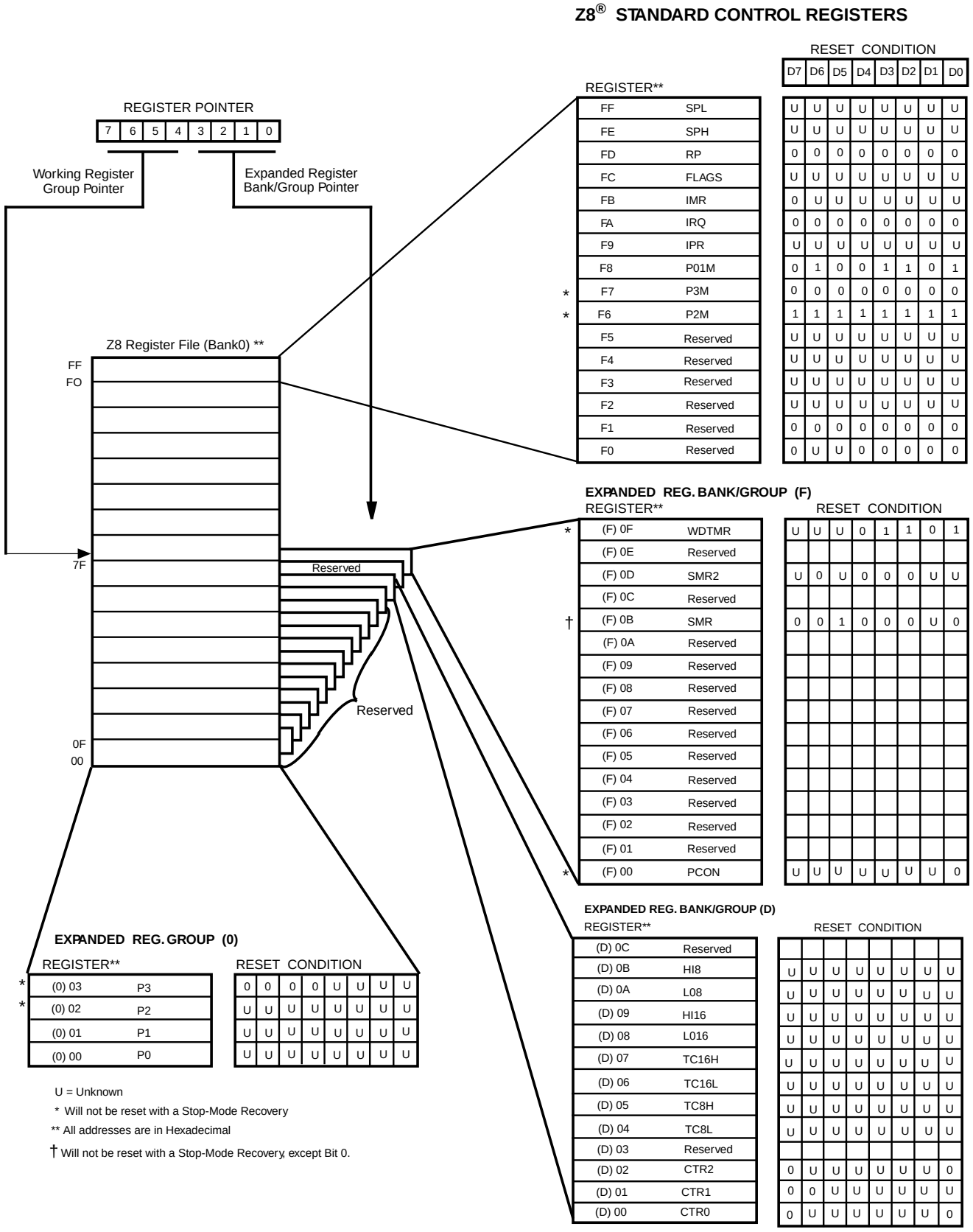


Figure 21. Expanded Register File Architecture

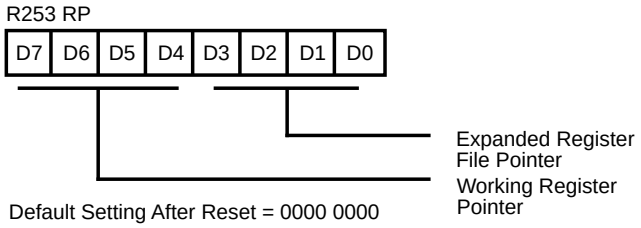


Figure 22. Register Pointer Register

Register File. The register file (bank 0) consists of four I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0-R3, R4-R239, and R240-R255, respectively), Plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the Register Pointer (Figure 23). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Working register group E0-EF can only be accessed through working registers and indirect addressing modes.

Stack. The Z86LXX external data memory or the internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4-R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH will be loaded into Port 0 whenever the internal stack is accessed.

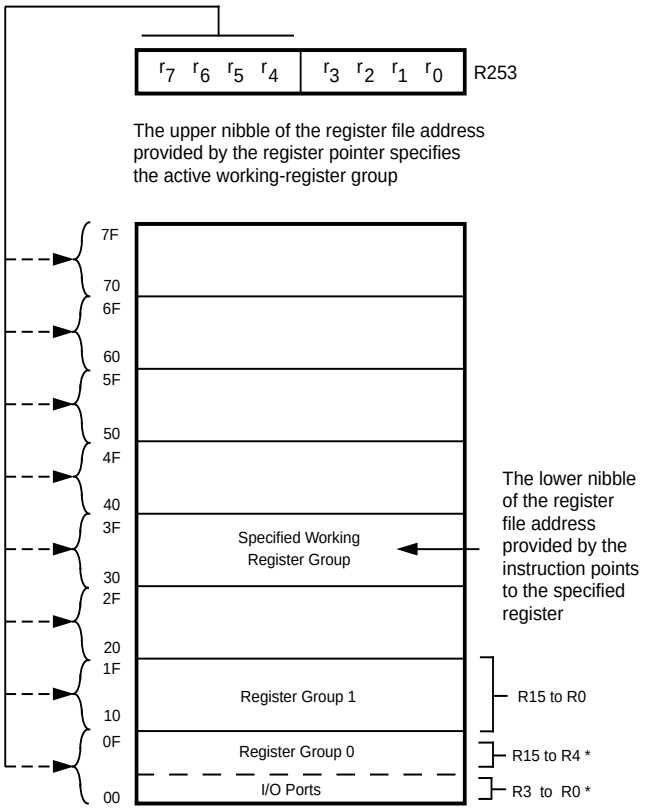


Figure 23. Register Pointer

COUNTER/TIMER REGISTER DESCRIPTION

Table 4. Expanded Register Group D

(D)%0C	Reserved
(D)%0B	HI8
(D)%0A	LO8
(D)%09	HI16
(D)%08	LO16
(D)%07	TC16H
(D)%06	TC16L
(D)%05	TC8H
(D)%04	TC8L
(D)%03	Reserved
(D)%02	CTR2
(D)%01	CTR1
(D)%00	CTR0

Register Description

HI8(D)%0B: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

Field	Bit Position		Description
T8_Capture_HI	76543210	R	Captured Data
		W	No Effect

L08(D)%0A: Holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

Field	Bit Position		Description
T8_Capture_L0	76543210	R	Captured Data
			No Effect
		W	

HI16(D)%09: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)%08: Holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)%07: Counter/Timer2 MS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)%06: Counter/Timer2 LS-Byte Hold Register.

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)%05: Counter/Timer8 High Hold Register.

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)%04: Counter/Timer8 Low Hold Register.

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

CTR0 (D)00: Counter/Timer8 Control Register.

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
			1	Enable Time-Out Int.
P34_Out	-------0	R/W	0*	P34 as Port Output
			1	T8 Output on P34

Note: * Indicates the value upon Power-On Reset.

CTR0: Counter/Timer8 Control Register Description

T8 Enable. This field enables T8 when set (written) to 1.

Single/Modulo-N. When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

Time-Out. This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 should be written to this location. **This is the only way to reset this status condition, therefore, care should be taken to reset this bit prior to using/enabling the counter/timers.**

Note: Care must be taken when utilizing the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (Demodulation Mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers will be ORed or ANDed with the designated value and then written back into the registers. Example: When the status of bit 5 is 1, a timer reset condition will occur.

T8 Clock. Defines the frequency of the input signal to T8.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

Counter_INT_Mask. Set this bit to allow interrupt when T8 has a time out.

P34_Out. This bit defines whether P34 is used as a normal output pin or the T8 output.

CTR1(D)%01: Controls the functions in common with the T8 and T16.

Field	Bit Position		Value	Description
Mode	7-------	R/W	0*	Transmit Mode
				Demodulation Mode
P36_Out/Demodulator _Input	-6------	R/W		Transmit Mode
			0*	Port Output
			1	T8/T16 Output
				Demodulation Mode
			0	P31
			1	P20
T8/T16_Logic/ Edge _Detect	--54----	R/W		Transmit Mode
			00	AND
			01	OR
			10	NOR
			11	NAND
				Demodulation Mode
			00	Falling Edge
			01	Rising Edge
			10	Both Edges
			11	Reserved
Transmit_Submode/ Glitch_Filter	----32--	R/W		Transmit Mode
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	16 SCLK Cycle
Initial_T8_Out/ Rising Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/ Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 Initially
			1	T16_OUT is 1 Initially
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note: *Default upon Power-On Reset

CTR1 Register Description

Mode. If it is 0, the Counter/Timers are in the transmit mode, otherwise they are in the demodulation mode.

P36_Out/Demodulator_Input. In Transmit Mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In Demodulation Mode, this bit defines whether the input signal to the Counter/Timers is from P20 or P31.

T8/T16_Logic/Edge _Detect. In Transmit Mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In Demodulation Mode, this field defines which edge should be detected by the edge detector.

Transmit_Submode/Glitch Filter. In Transmit Mode, this field defines whether T8 and T16 are in the "Ping-Pong" mode or in independent normal operation mode. Setting this field to "Normal Operation Mode" terminates the "Ping-Pong Mode" operation. When set to 10, T16 is immediately forced to a 0; a setting of 11 will force T16 to output a 1.

In Demodulation Mode, this field defines the width of the glitch that should be filtered out.

Initial_T8_Out/Rising_Edge. In Transmit Mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When The counter is not enabled and this bit is set to 1 or 0, T8_OUT will be set to the opposite state of this bit. This insures that when the clock is enabled a transition occurs to the initial state set by CTR1, D1.

In Demodulation Mode, this bit is set to 1 when a rising edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Initial_T16 Out/Falling _Edge. In Transmit Mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2). When the counter is not enabled and this bit is set, T16_OUT will be set to the opposite state of this bit. This insures that when the clock is enabled a transition occurs to the initial state set by CTR1, D0.

In Demodulation Mode, this bit is set to 1 when a falling edge is detected in the input signal. In order to reset it, a 1 should be written to this location.

Note: Modifying CTR1, (D1 or D0) while the counters are enabled will cause un-predictable output from T8/16_OUT.

CTR2 (D)%02: Counter/Timer16 Control Register.

Field	Bit Position		Value	Description
T16_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6------	R/W		Transmit Mode
			0	Modulo-N
			1	Single Pass
				Demodulation Mode
			0	T16 Recognizes Edge
			1	T16 Does Not Recognize Edge
Time_Out	--5-----	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T16 _Clock	---43---	R/W	00	SCLK
			01	SCLK/2
			10	SCLK/4
			11	SCLK/8
Capture_INT_Mask	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.
Counter_INT_Mask	------1-	R/W	0	Disable Time-Out Int.
				Enable Time-Out Int.
P35_Out	-------0	R/W	0*	P35 as Port Output
			1	T16 Output on P35

Note: * Indicates the value upon Power-On Reset.

CTR2 Description

T16_Enable. This field enables T16 when set to 1.

Single/Modulo-N. In Transmit Mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In Demodulation Mode, when set to 0 , T16 captures and reloads on detection of all the edges; when set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see the description of T16 Demodulation Mode.

Time_Out. This bit is set when T16 times out (terminal count reached). In order to reset it, a 1 should be written to this location.

T16_Clock. Defines the frequency of the input signal to Counter/Timer16.

Capture_INT_Mask. Set this bit to allow interrupt when data is captured into LO16 and HI16.

Counter_INT_Mask. Set this bit to allow interrupt when T16 times out.

P35_Out. This bit defines whether P35 is used as a normal output pin or T16 output.

SMR2(F)%0D: Stop-Mode Recovery Register 2.

Field	Bit Position		Value	Description
Reserved	7-------		0	Reserved (Must be 0)
Recovery Level	-6------	W	0*	Low
			1	High
Reserved	--5-----		0	Reserved (Must be 0)
Source	---432--	W	000*	A. POR Only
			001	B. NAND of P23-P20
			010	C. NAND or P27-P20
			011	D. NOR of P33-P31
			100	E. NAND of P33-P31
			101	F. NOR of P33-P31, P00,P07
			110	G. NAND of P33-P31,P00,P07
			111	H. NAND of P33-P31,P22-P20
Reserved	------10		00	Reserved (Must be 0)

Notes:
* Indicates the value upon Power-On Reset
Port pins configured as outputs are ignored as a SMR recovery source.

Counter/Timer Functional Blocks

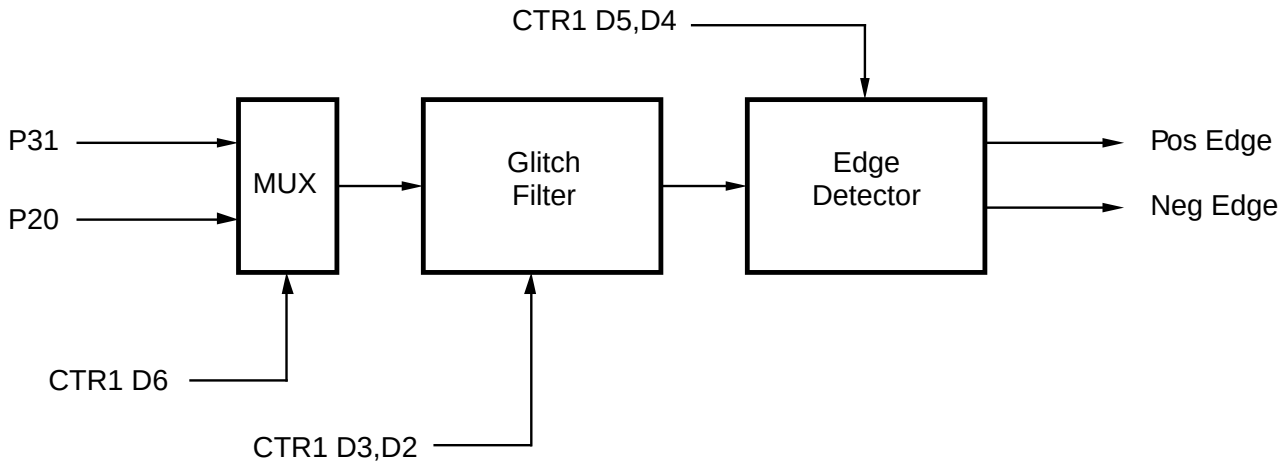


Figure 24. Glitch Filter Circuitry

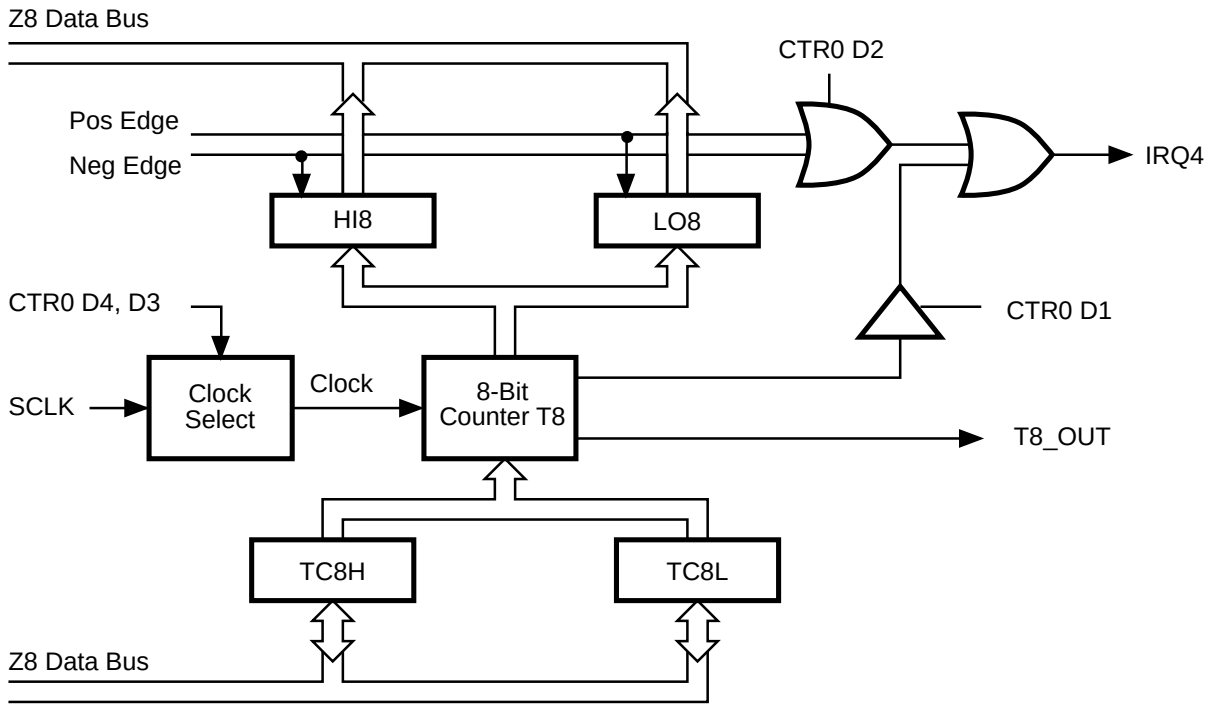


Figure 25. 8-Bit Counter/Timer Circuits

Input Circuit
The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5-D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal which have a width less than specified (CTR1 D3, D2) are filtered out.

T8 Transmit Mode
Before T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8_OUT is 1. If it is 1, T8_OUT is 0.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded, otherwise TC8H is loaded into the counter. In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1) (Figure 26). In Modulo-N Mode, upon reaching terminal count, T8_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, sets the time-out status bit (CTR0 D5) and generates an interrupt if enabled (CTR0 D1) (Figure 27). This completes one cycle. T8 then loads from TC8H or TC8L according to the T8_OUT level, and repeats the cycle.

The user can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Care must be taken not to write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. **An initial count of 1 is not allowed (a non-function will occur).** An initial count of 0 will cause TC8 to count from 0 to %FF to %FE (Note, % is used for hexadecimal values). Transition from 0 to %FF is not a time-out condition.

Note: Using the same instructions for stopping the counter/timers and setting the status bits is not recommended. Two successive commands, first stopping the counter/timers, then resetting the status bits is necessary. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

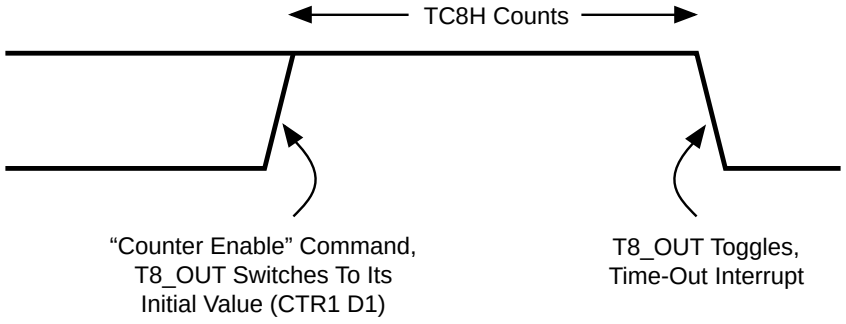


Figure 26. T8_OUT in Single-Pass Mode

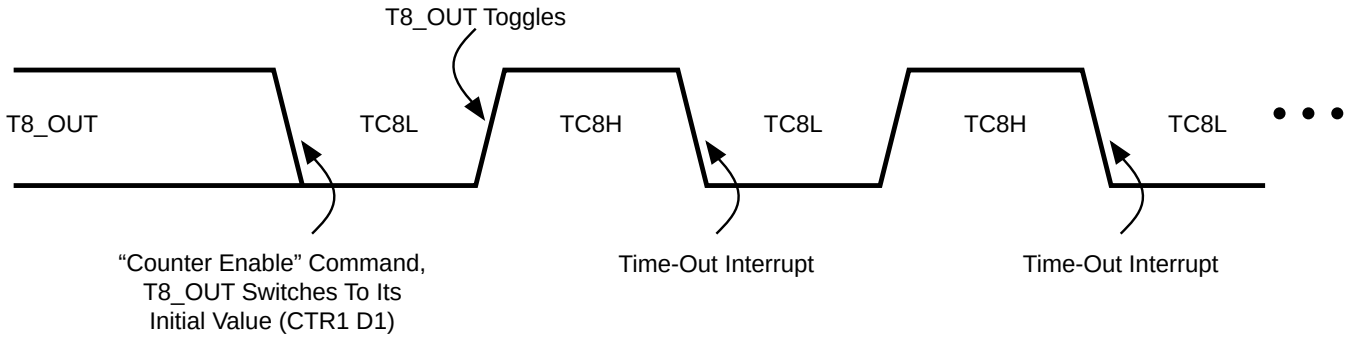


Figure 27. T8_OUT in Modulo-N Mode

T8 Demodulation Mode

The user should program TC8L and TC8H to %FF. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8, if negative edge, HI8. One of the edge detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with %FF and starts counting again. Should T8 reach 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from %FF (Figure 28).

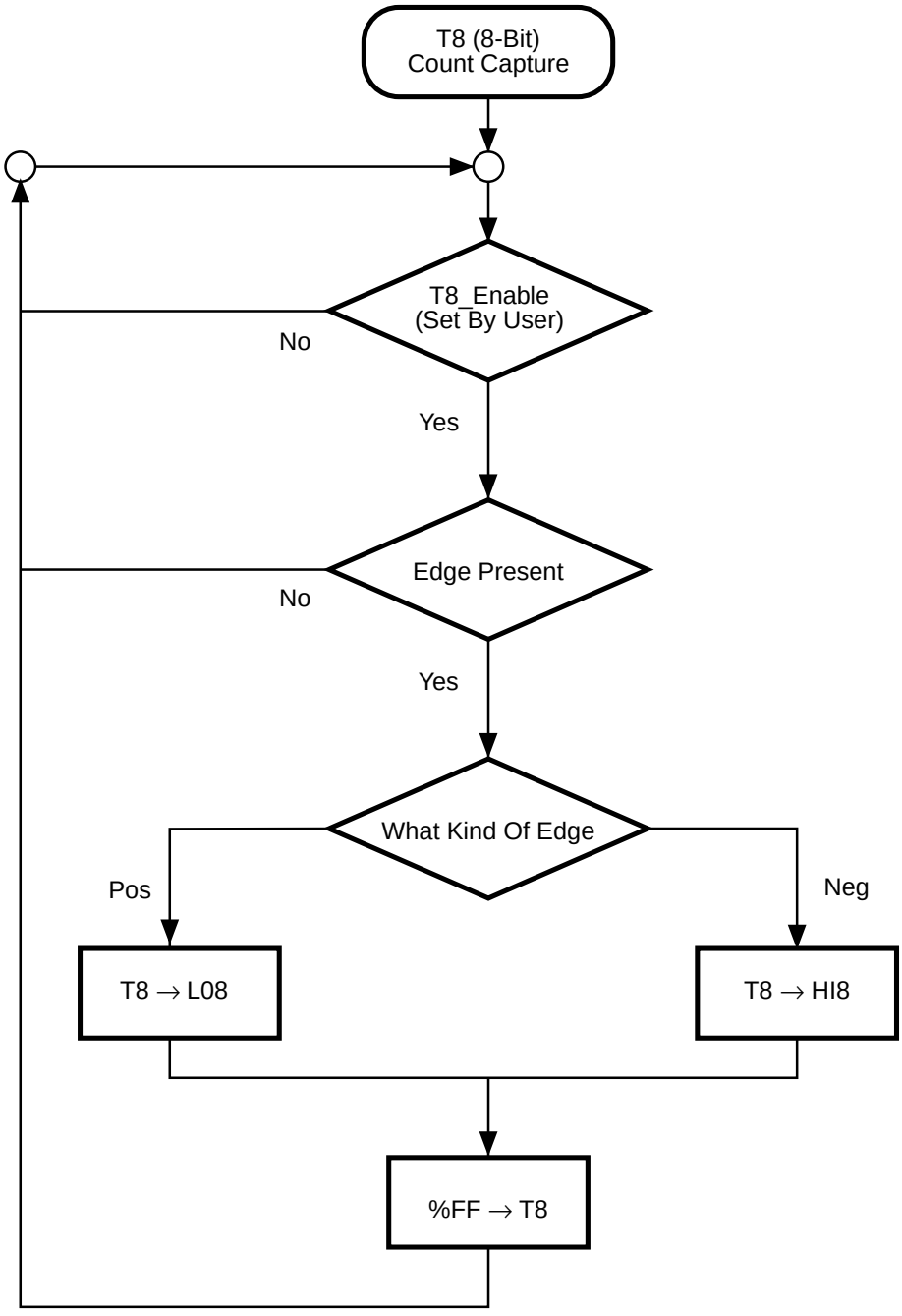


Figure 28. Demodulation Mode Count Capture Flowchart

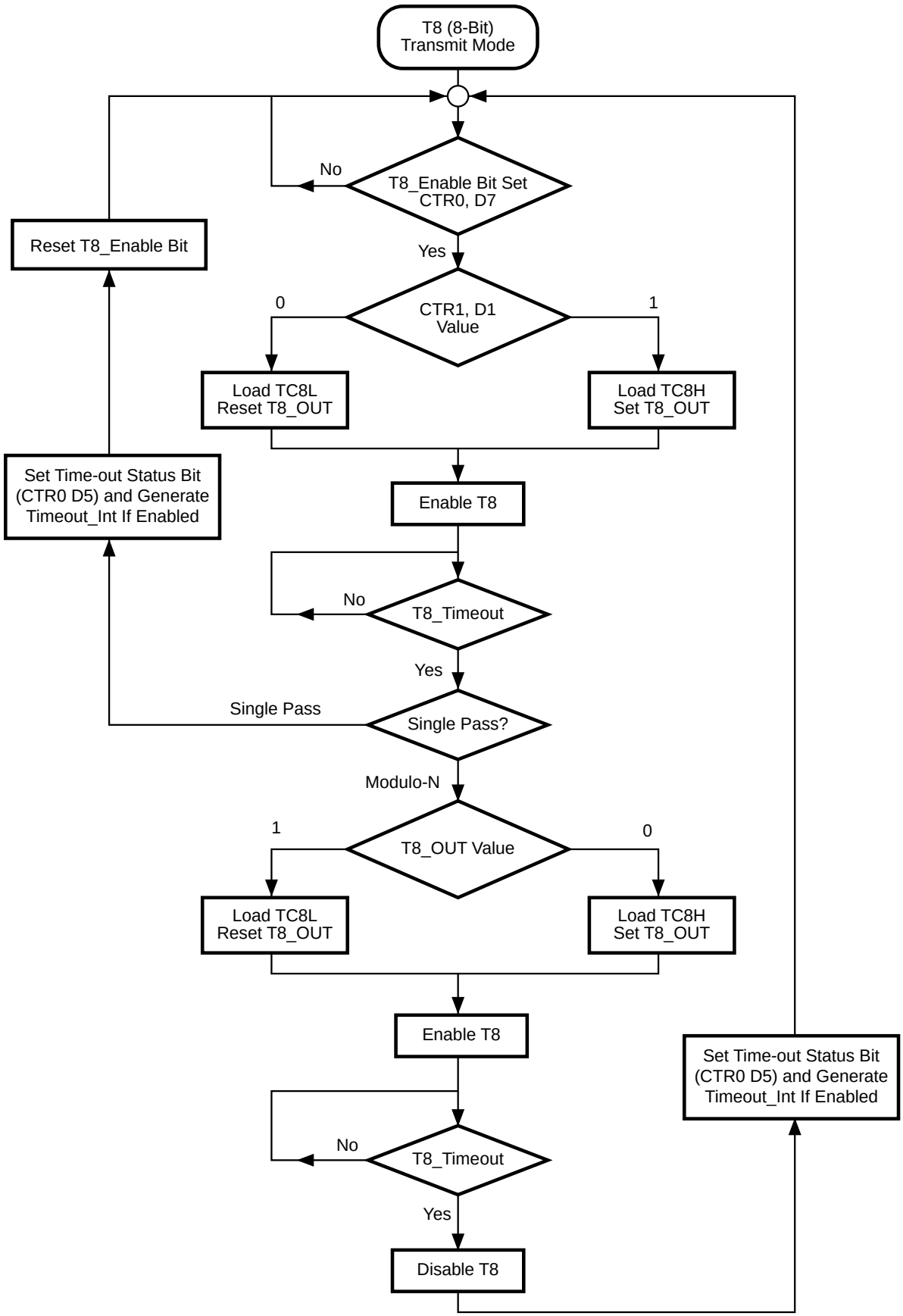


Figure 29. Transmit Mode Flowchart

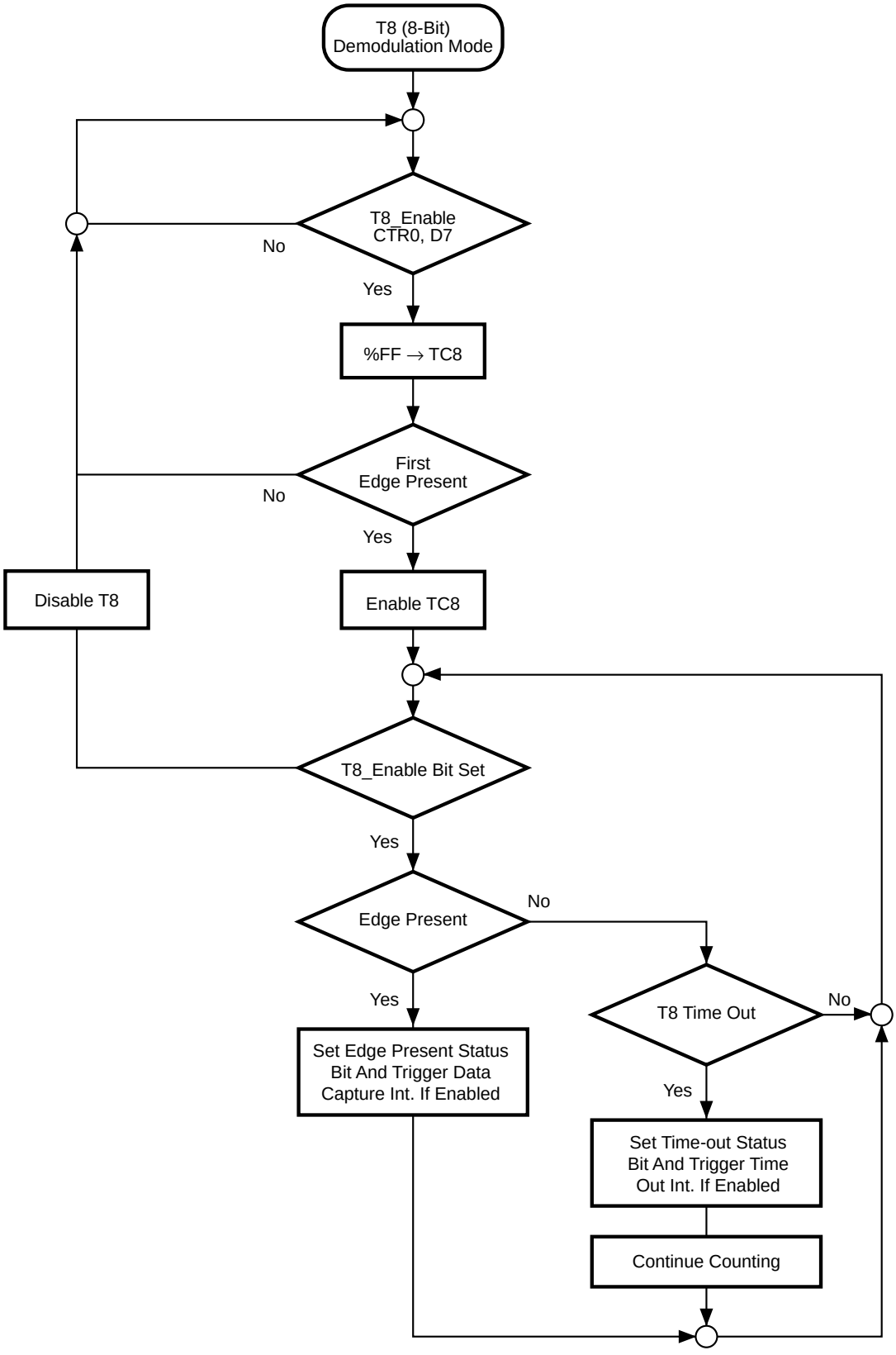


Figure 30. Demodulation Mode Flowchart

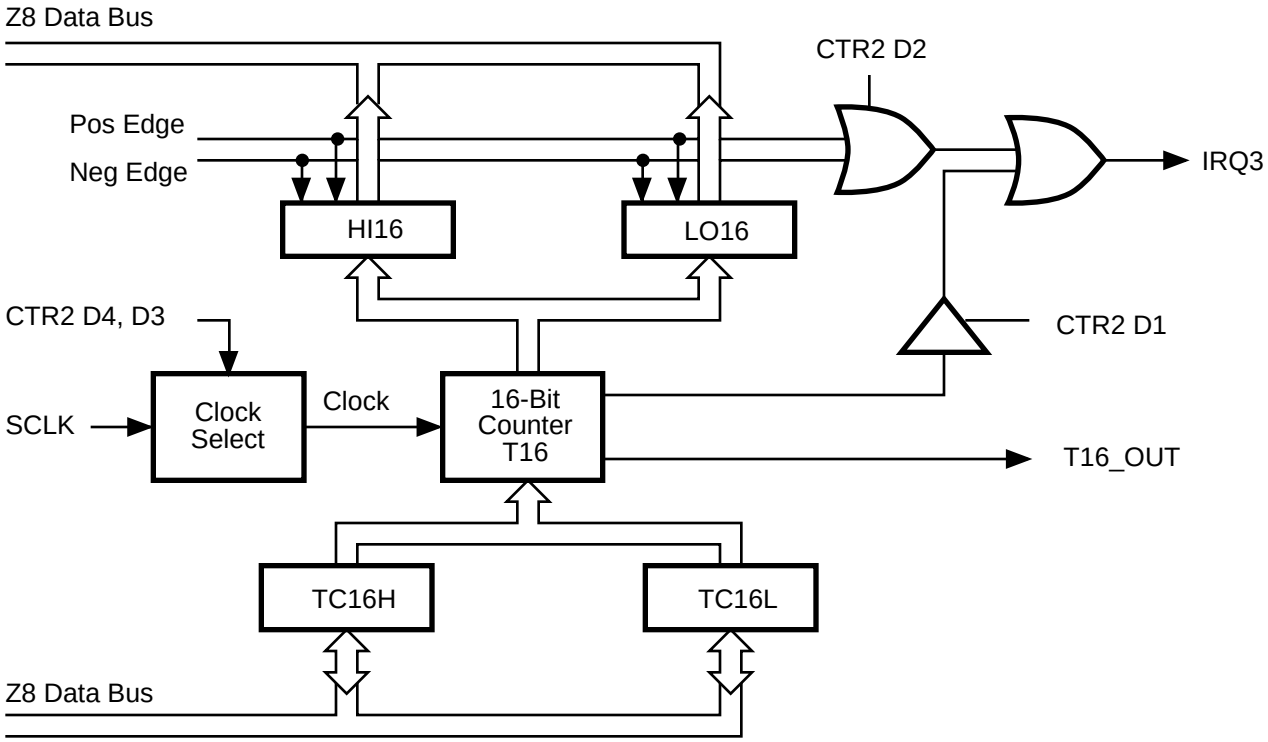


Figure 31. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16 when not enabled is dependent on CTR1, D0. If it is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. The user can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set. Note that global interrupts will override this function as described in the interrupts section. If T16 is in Single-Pass Mode, it is stopped at this point. If it is in Modulo-N Mode, it is loaded with TC16H * 256 + TC16L and the counting continues.

The user can modify the values in TC16H and TC16L at any time. The new values take effect when they are loaded. Care must be taken not to load these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed. An initial count of 0 will cause T16 to count from 0 to %FF FF to %FFFE. Transition from 0 to %FFFF is not a time-out condition.

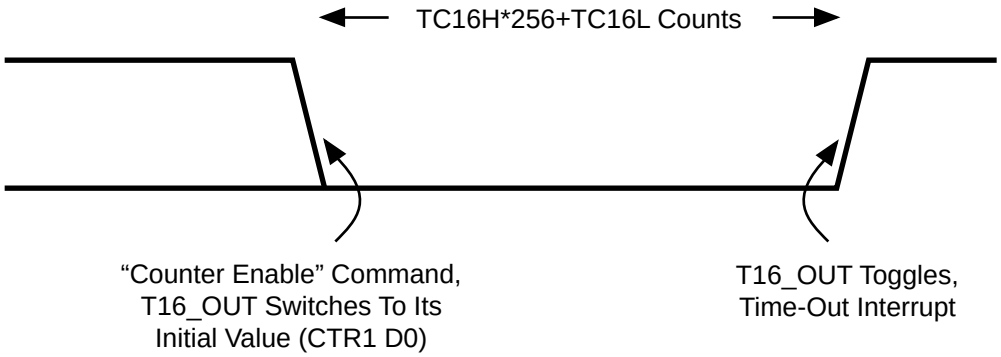


Figure 32. T16_OUT in Single-Pass Mode

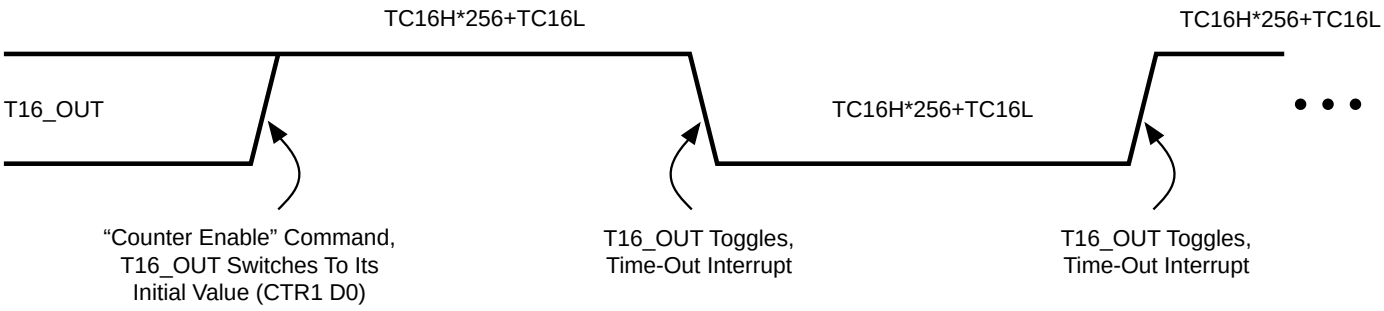


Figure 33. T16_OUT in Modulo-N Mode

T16 Demodulation Mode

The user should program TC16L and TC16H to %FF. After T16 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, T16 captures HI16 and LO16, reloads and begins counting.

If D6 of CTR2 is 0: When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current count in T16 is one's complemented and put into HI16 and LO16. When data is captured, one of the edge detect status bits (CTR1 D1, D0) is set and an interrupt is generated if enabled (CTR2 D2). T16 is loaded with %FFFF and starts again.

This T16 mode is generally used to measure space time; the length of time between bursts of carrier signal(marks).

If D6 of CTR2 is 1: T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 will cause T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 then a 1 to it), T16 will capture and reload on the next edge (rising, falling, or both depending on CTR1 D5, D4) but continue to ignore subsequent edges.

This T16 mode is generally used to measure mark times; the length of an active carrier signal bursts.

Should T16 reach 0, it continues counting from %FFFF; meanwhile, a status bit (CTR2 D5) is set and an interrupt time-out can be generated if enabled (CTR2 D1).

Ping-Pong Mode

This operation mode is only valid in Transmit Mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6) and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. The user can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8_OUT is set to this initial value (CTR1 D1). According to T8_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1.

Note: Enabling Ping-Pong operation while the counter/timers are running may cause intermittent counter/timer function. Disable the counter/timers, then reset the status flags prior to instituting this operation.

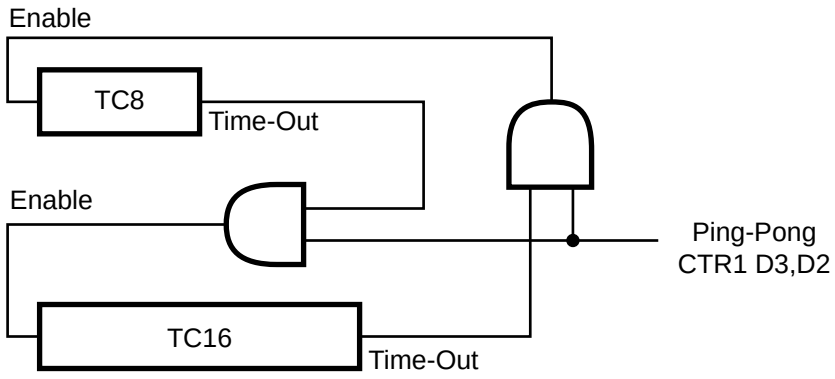


Figure 34. Ping-Pong Mode

To Initiate Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) will be set and cleared alternately by hardware. The time-out bits (CTR0 D5, CTR2 D5) will be set every time the counter/timers reach the terminal count.

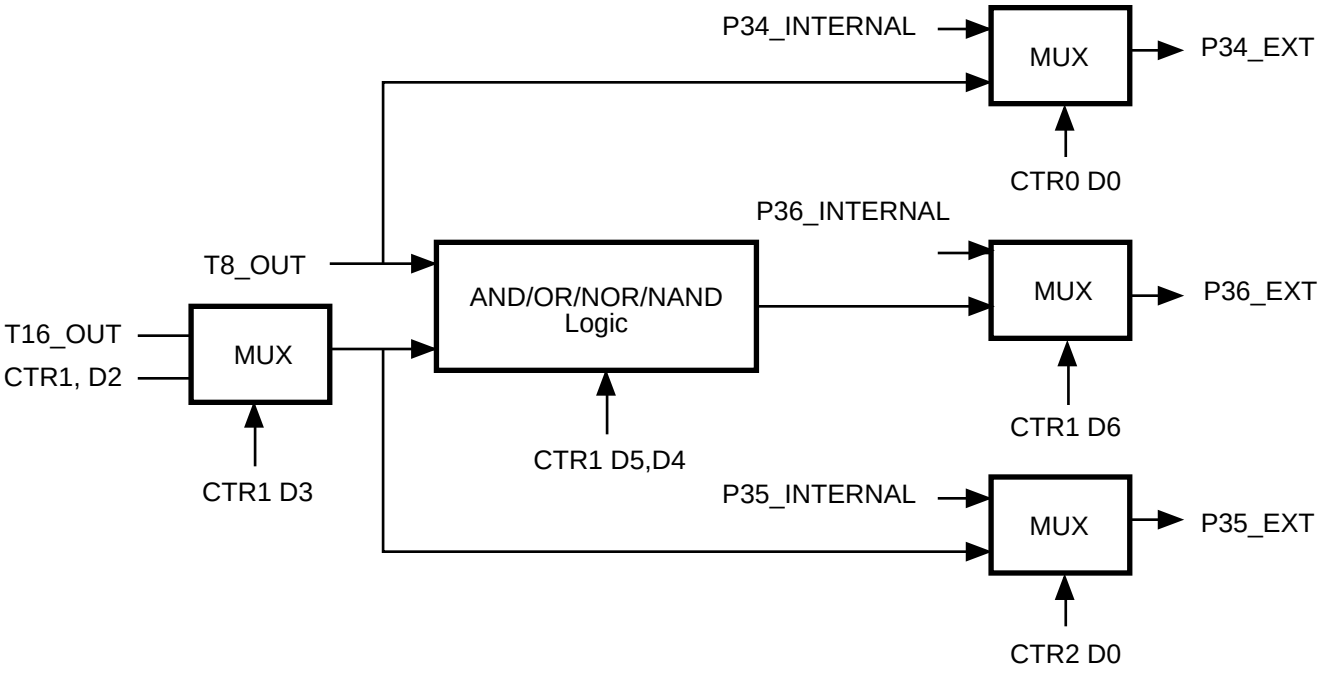


Figure 35. Output Circuit

Interrupts. The Z86LXX has five different interrupts. The interrupts are maskable and prioritized (Figure 36). The five sources are divided as follows: three sources are claimed by Port 3 lines P33-P31, the remaining two by the counter/timers (Table 5). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.

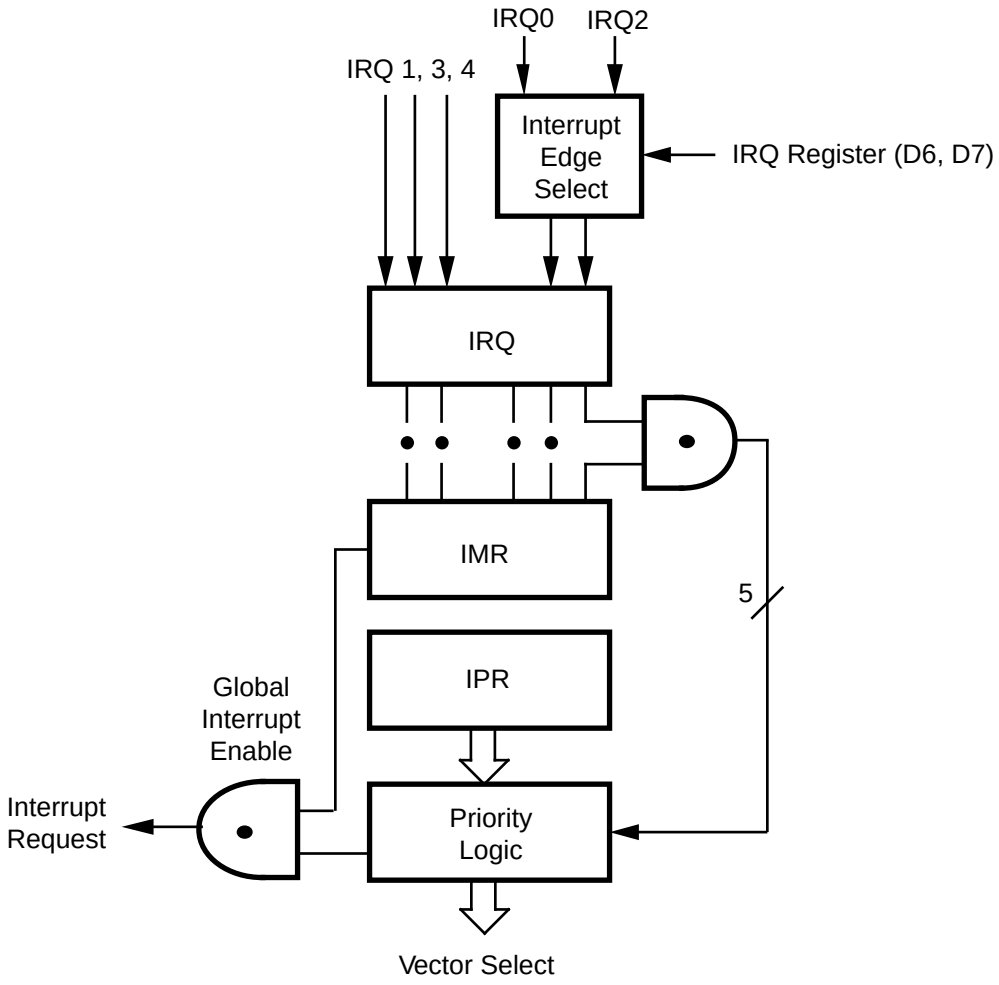


Figure 36. Interrupt Block Diagram

Table 5. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising Falling Edge Triggered
IRQ1,	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, $_{TIN}$	4, 5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6, 7	Internal
IRQ4	T8	8, 9	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86LXX interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling, or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6 . The configuration is shown in Table 6.

Table 6. IRQ Register

IRQ		Interrupt Edge	
D7	D6	IRQ2(P31)	IRQ0 (P32)
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

Clock. The Z86LXX on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86LXX on-chip oscillator may be driven with a low cost RC network or other suitable external clock source.

For 32 kHz crystal operation, an external feedback resistor (Rf) and a serial resistor (Rd) are required. See Figure 37.

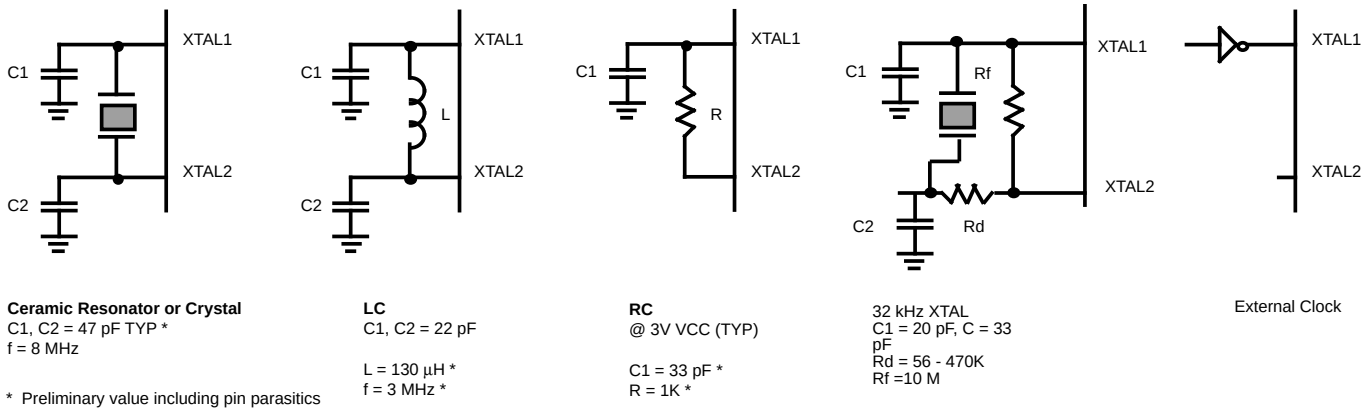
The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 37).

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power Fail to Power OK status including Waking up from (V_{LV} Standby).
2. Stop-Mode Recovery (if D5 of SMR = 1).
3. WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, LC oscillators).



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

* Preliminary value including pin parasitics

LC
C1, C2 = 22 pF

L = 130 µH *
f = 3 MHz *

RC
@ 3V VCC (TYP)

C1 = 33 pF *
R = 1K *

32 kHz XTAL
C1 = 20 pF, C = 33 pF
Rd = 56 - 470K
Rf =10 M

External Clock

Figure 37. Oscillator Configuration

HALT. HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. STOP mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode = FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

Port Configuration Register (PCON). The PCON register configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00 (Figure 38).

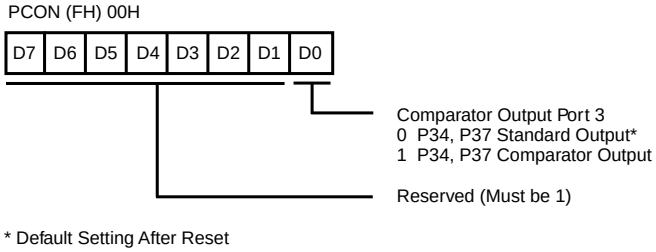


Figure 38. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the Port to its standard I/O configuration.

Stop-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 39). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bits D0 determines determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

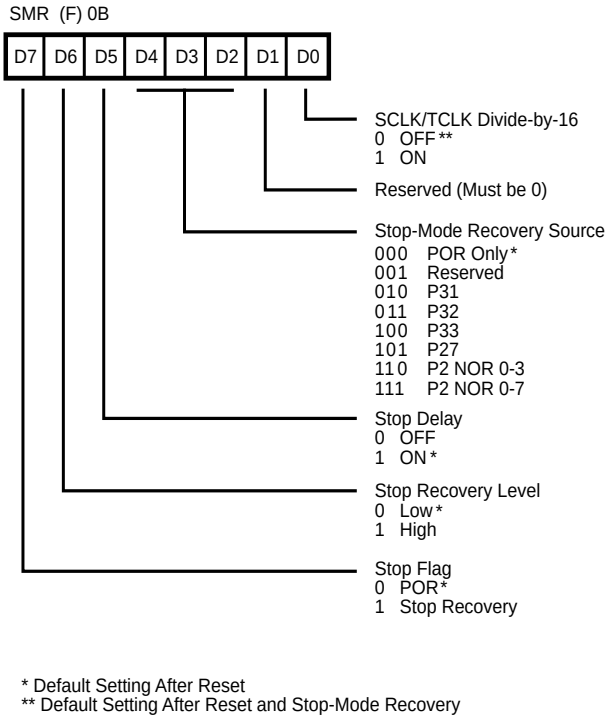


Figure 39. Stop-Mode Recovery Register

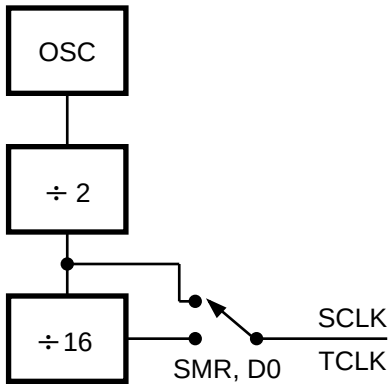


Figure 40. SCLK Circuit

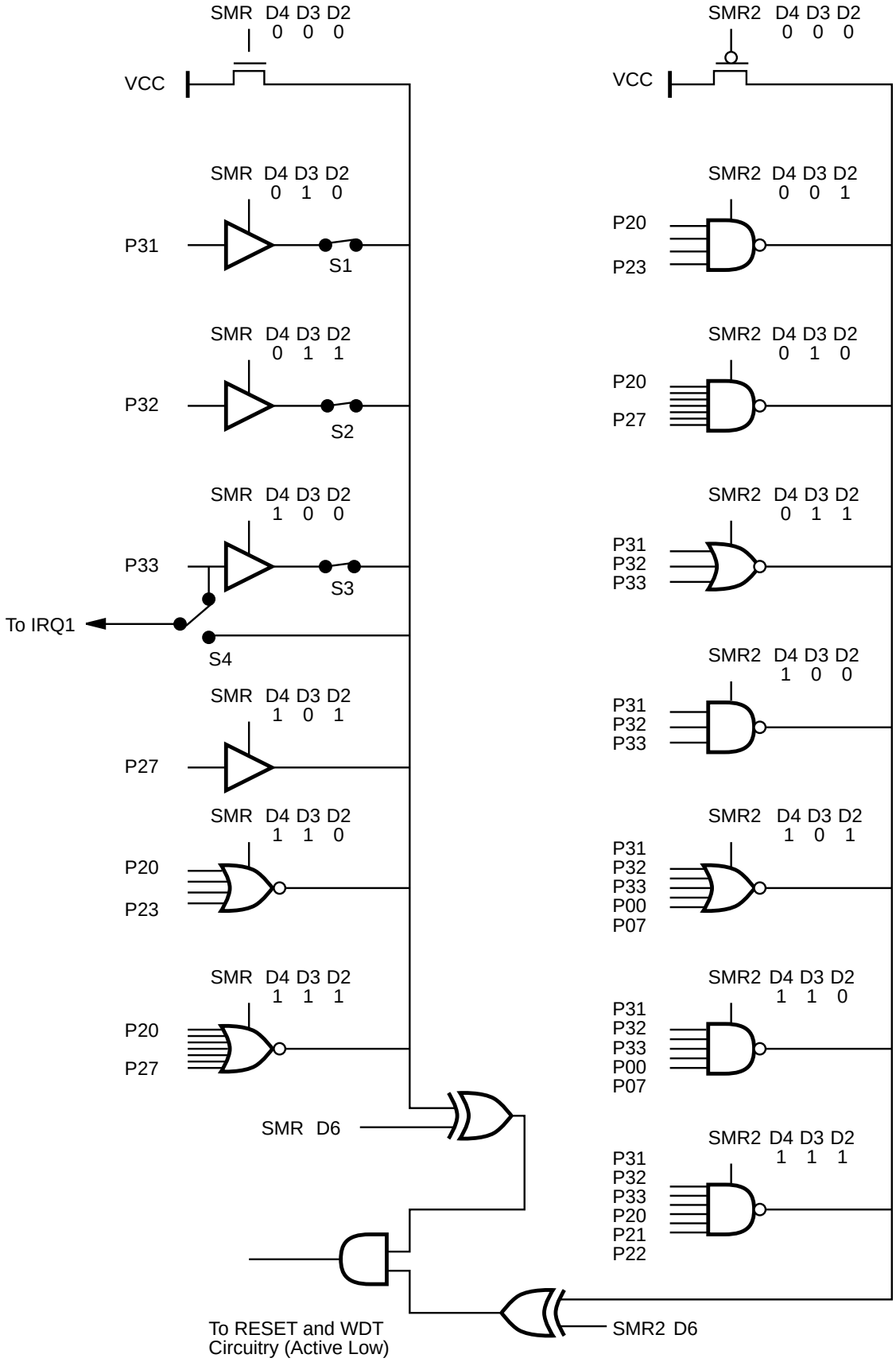


Figure 41. Stop-Mode Recovery Source

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

Stop-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the STOP recovery (Figure 41 and Table 7).

Table 7. Stop-Mode Recovery Source

SMR:432			Operation Description of Action
D4	**D3**	**D2**	Description of Action
0	0	0	POR and/or external reset recovery
0	0	1	Reserved
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of P20 through P23
1	1	1	Logical NOR of P20 through P27

Note: Any Port 2 bit defined as an output will drive the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to SMR2 register for other recover sources.

Stop-Mode Recovery Delay Select (D5). This bit, if low, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the "fast" wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

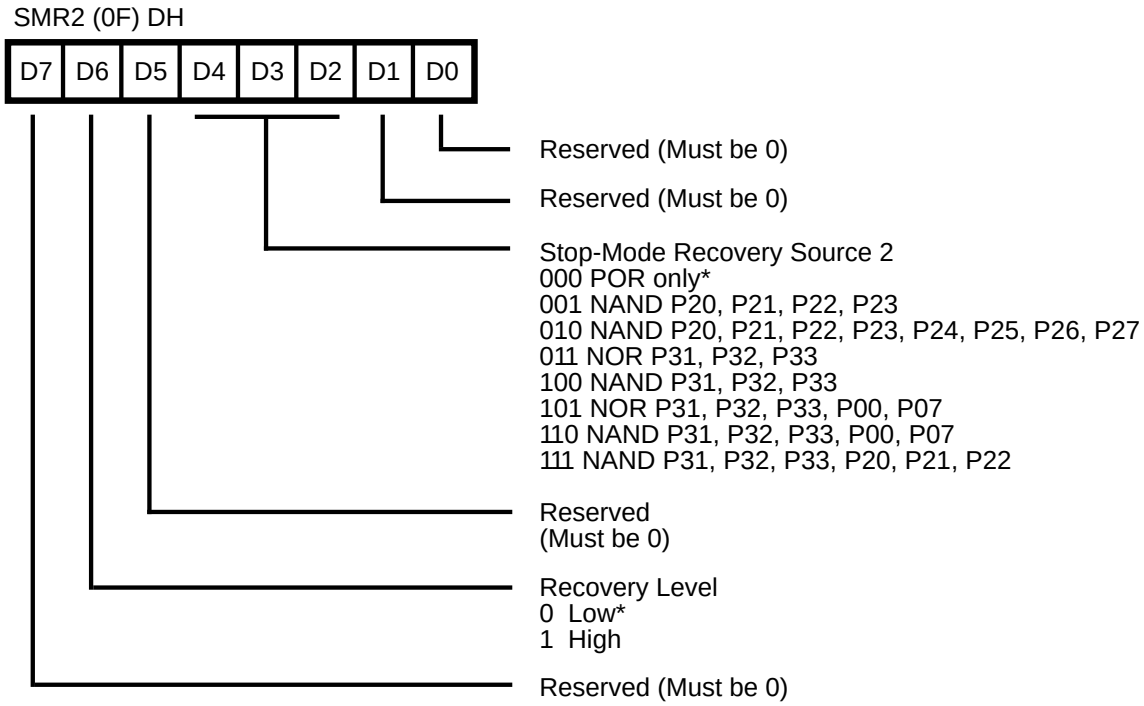
Stop-Mode Recovery Edge Select (D6). A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86LXX from STOP mode. A 0 indicates Low level recovery. The default is 0 on POR (Figure 36).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP mode. It is a Read Only Flag bit. A 1 in D7 (warm) indicates that the device will awaken from a SMR source or a WDT while in STOP mode. A 0 in this bit (cold) indicates that the device will be reset by a POR, WDT while not in STOP, or the device awakened from a low voltage standby mode.

Stop-Mode Recovery Register 2 (SMR2). This register determines the mode of Stop-Mode Recovery for SMR2 Figure 42).

If SMR2 is used in conjunction with SMR, either of the specified events will cause a Stop-Mode Recovery.

Note: Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND or P23-P20 is selected as the recovery source and P20 is configured as an output then the remaining SMR pins (P23-P21) form the NAND equation.



Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

*Default Setting After Reset

Figure 42. Stop-Mode Recovery Register 2 ((0F) DH: D2-D4, D6 Write Only)

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved (Figure 42). This register is accessible only during the first 61 processor cycles (122 XTAL clocks) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery (Figure 43). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as follows:

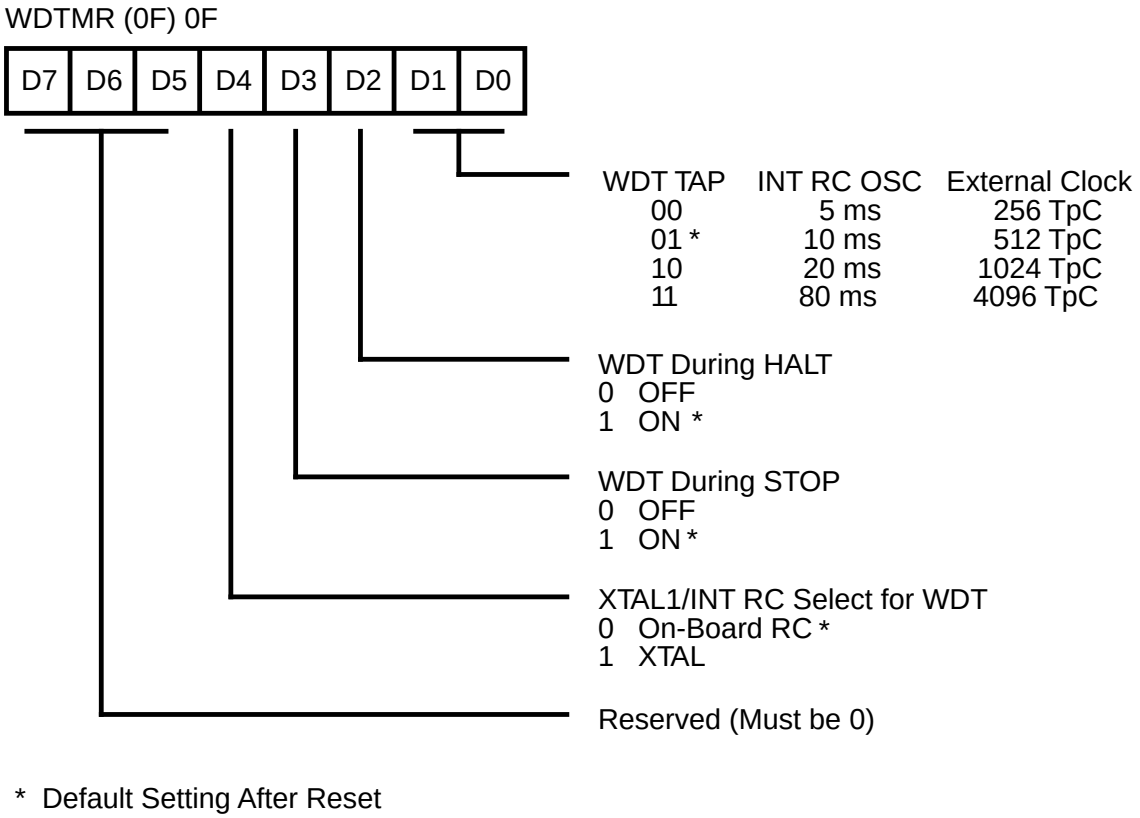


Figure 43. Watch-Dog Timer Mode Register (Write Only)

WDT Time Select (D0, D1). Selects the WDT time period. It is configured as shown in Table 8.

Table 8. WDT Time Select

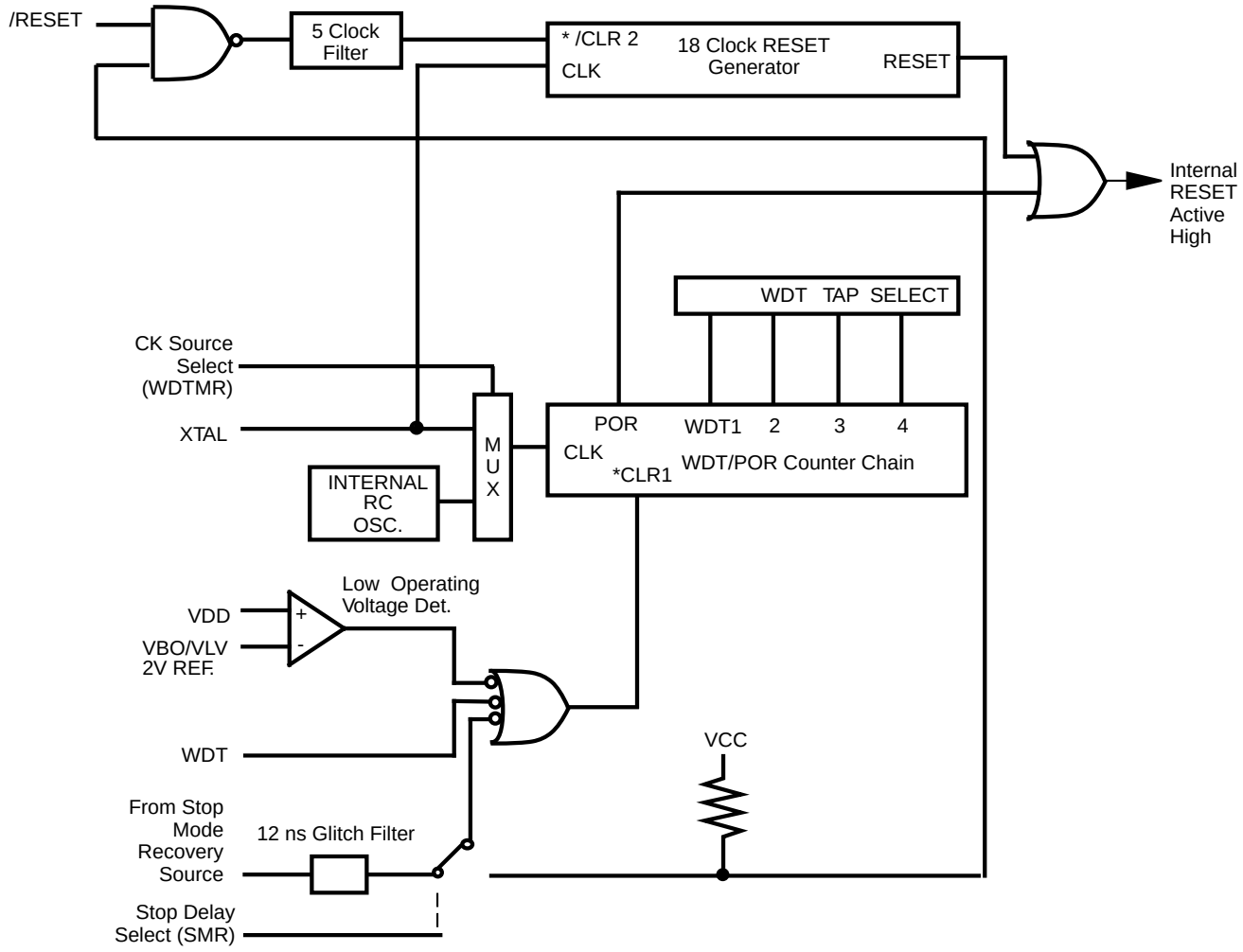
D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle.
The default on reset is 10 ms.

WDTMR During HALT (D2). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT. The default is 1.

WDTMR During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. Since the XTAL clock is stopped during STOP mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

Clock Source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.



* /CLR1 and /CLR2 enable the WDT/POR and
18 Clock Reset timers upon a Low to High input translation.

Figure 44. Resets and WDT

Mask Selectable Options. There are seven Mask Selectable Options to choose from based on ROM code requirements. These are:

RAM Protect	On/Off
RC/Other	RC/XTAL
32 kHz XTAL	On/Off
Port 04-07 Pull-Ups	On/Off
Port 00-03 Pull-Ups	On/Off
Port 20-27 Pull-Ups	On/Of
Port 30-33 Pull-Ups	On/Of
Port 3 Mouse Mode 0.4 V_{DD} Trip	On/Off

Low Voltage Detection/Standby. An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{LV} (Vrf1). A small further drop in V_{CC} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. Typical Low-Voltage power consumpion in this Low Voltage Standby mode (I_{LV}) is about 45 µA (varying with the number of Mask selectable options enabled). If the V_{CC} is allowed to stay above Vram, the RAM content is preserved. When the power level is returned to above V_{LV}, the device will perform a POR and function normally (Figure 45).

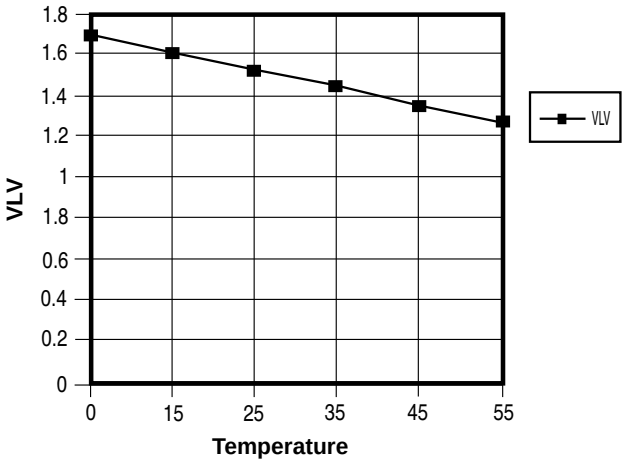


Figure 45. Typical Z86LXX Low Voltage vs Temperature at 8 MHZ

The minimum operating voltage varies with the temperature and operating frequency, while V_{LV} varies with temperature only.

The Low Voltage trip voltage (V_{LV}) is less than 2.1V under the following conditions:

Maximum (V_{LV}) Conditions:

T_A = 0°C, +55°C Internal clock frequency equal to or less than 4.0 MHz

Note: The internal clock frequency is one-half the external clock frequency.

EXPANDED REGISTER FILE CONTROL REGISTERS (0D)

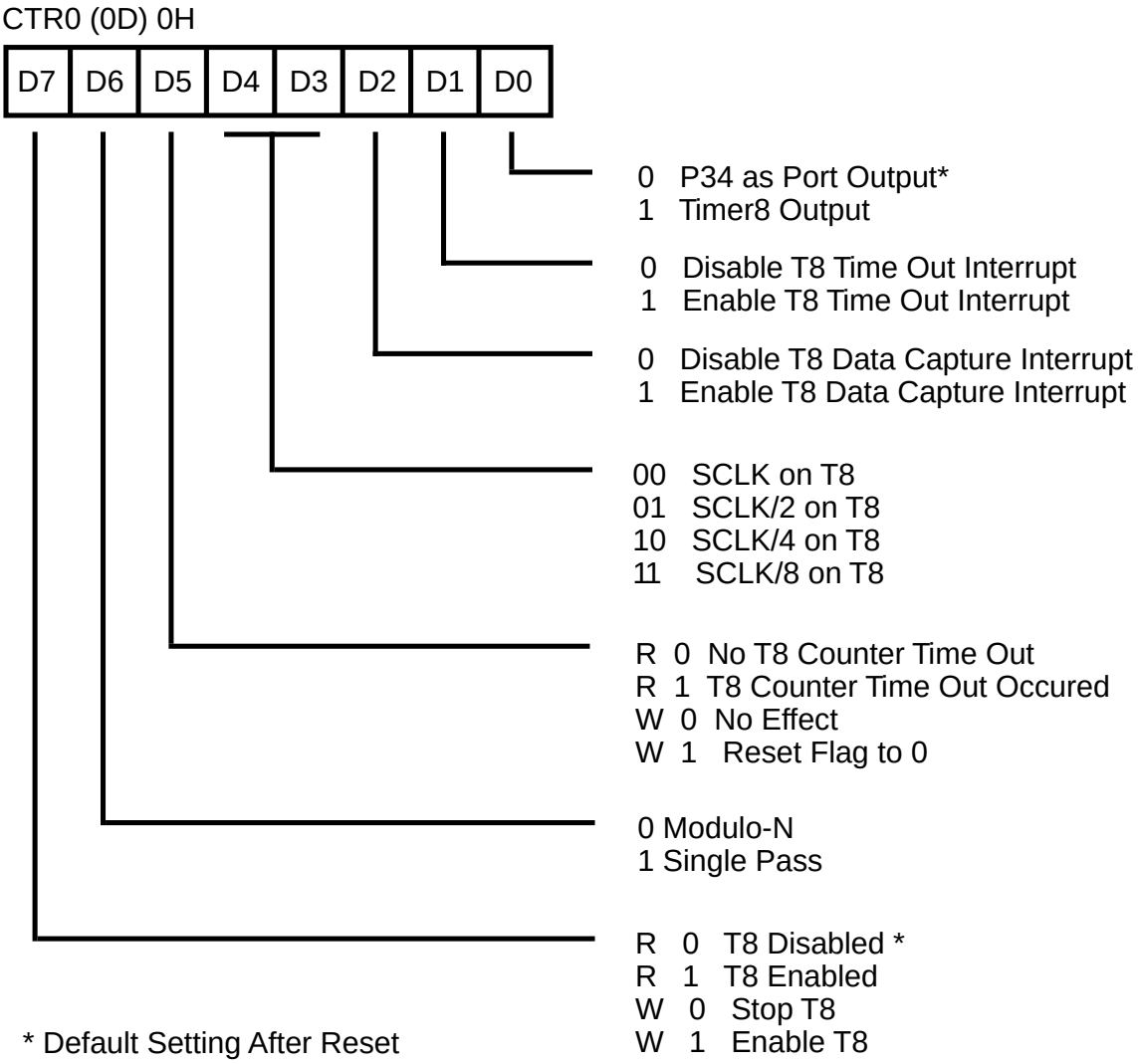
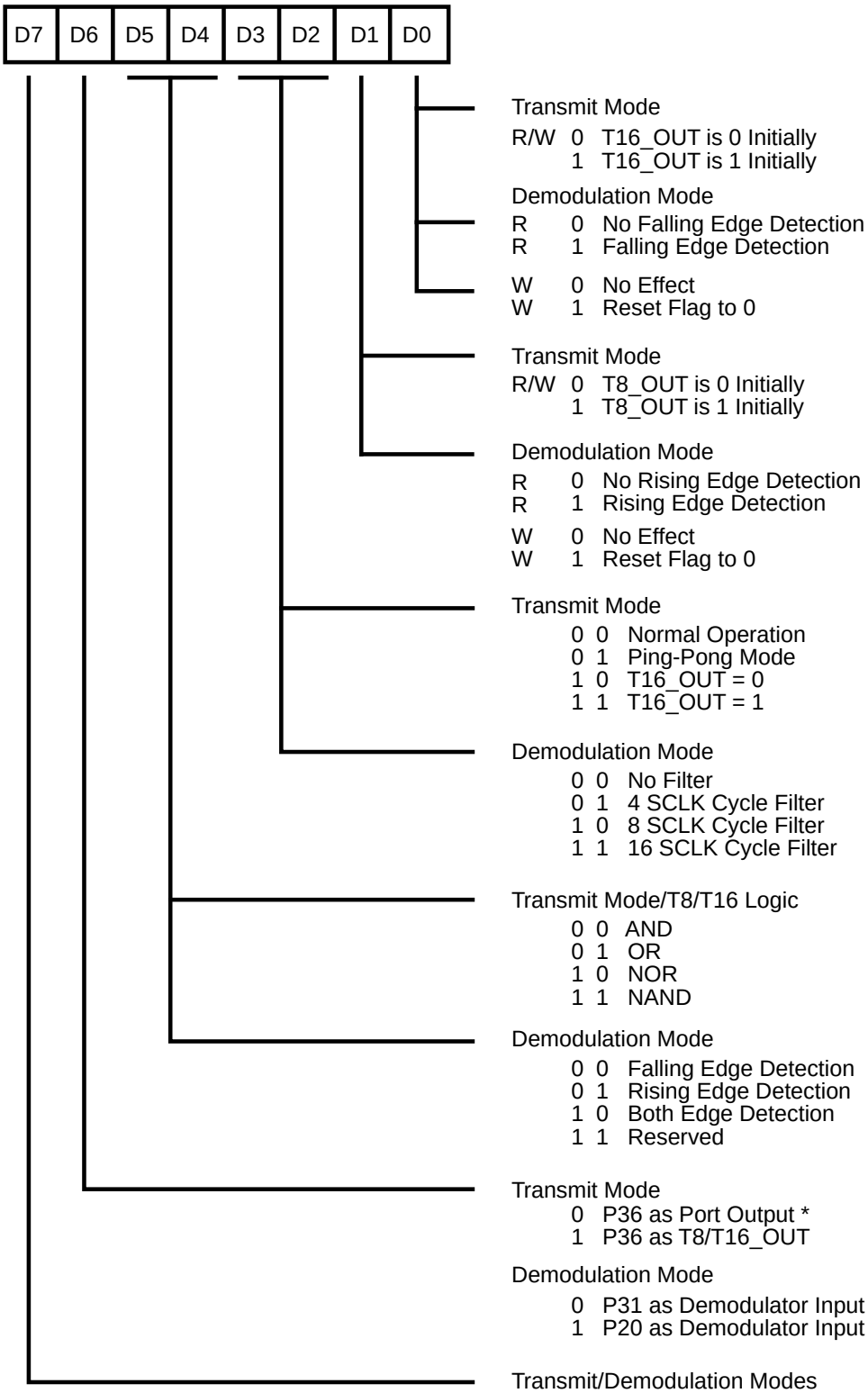


Figure 46. TC8 Control Register
((0D) OH: Read/Write Except Where Noted)

CTR1 (0D) 1H



*Default setting after Reset

Note: Care must be taken in differentiating Transmit Mode from Demodulation Mode. Depending on which of these two modes is operating, the CTR1 bit will have different functions.

Note: Changing from one mode to another cannot be done without disabling the counter/timers.

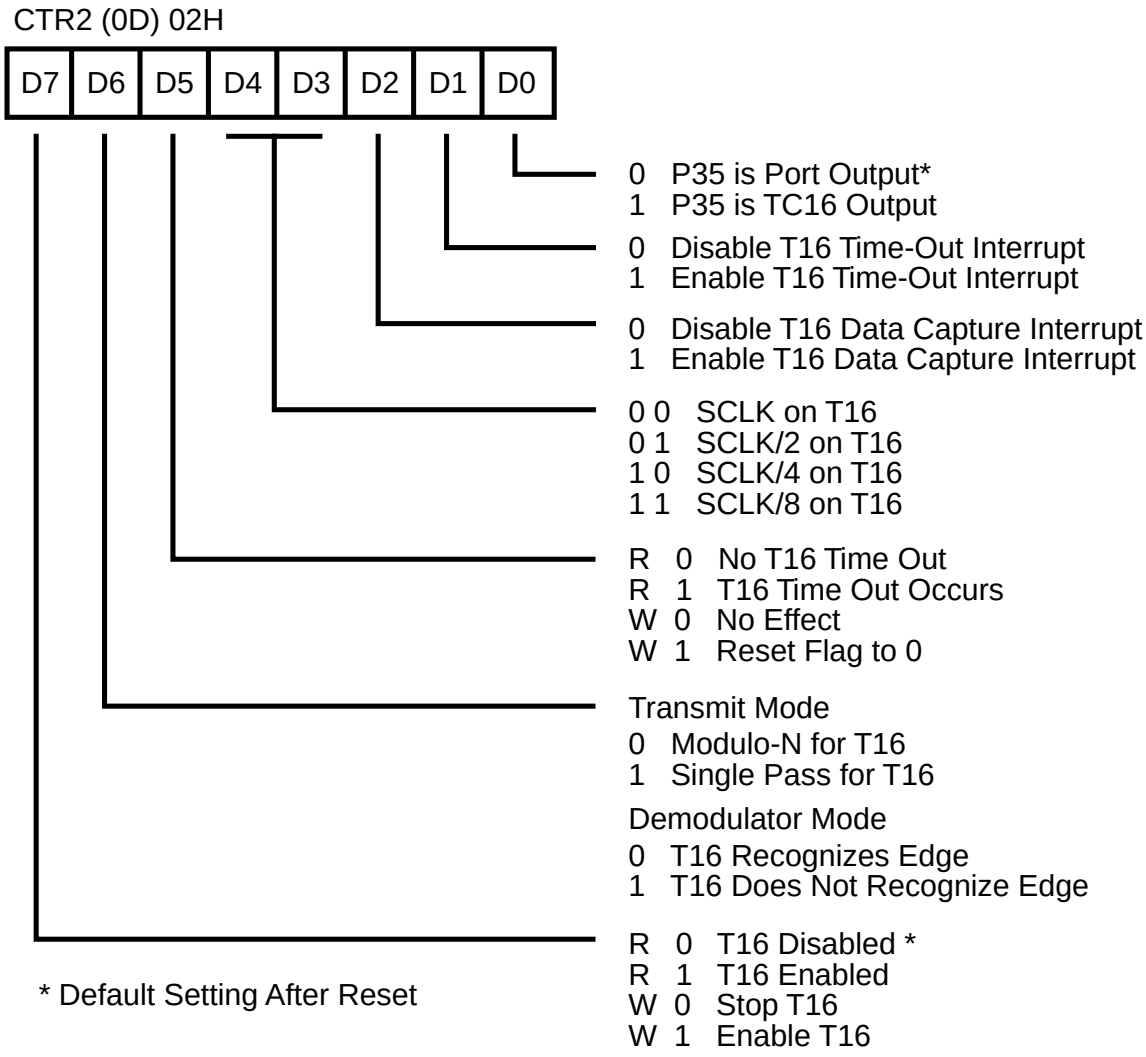
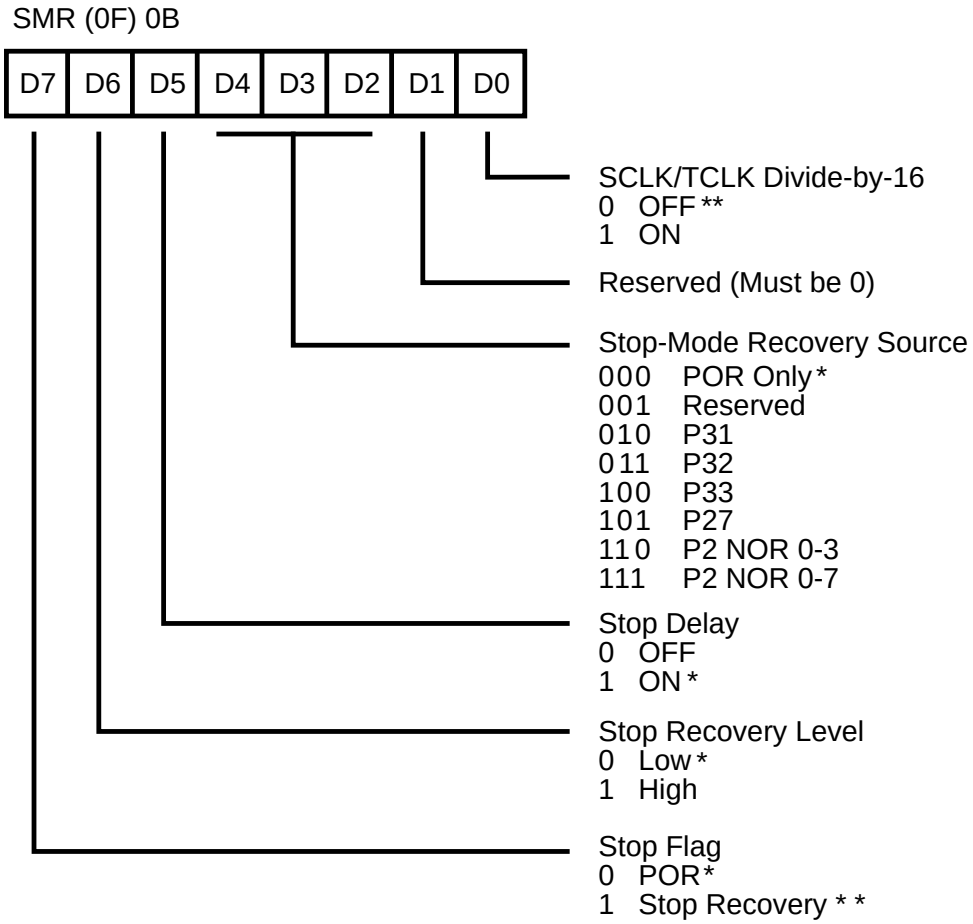


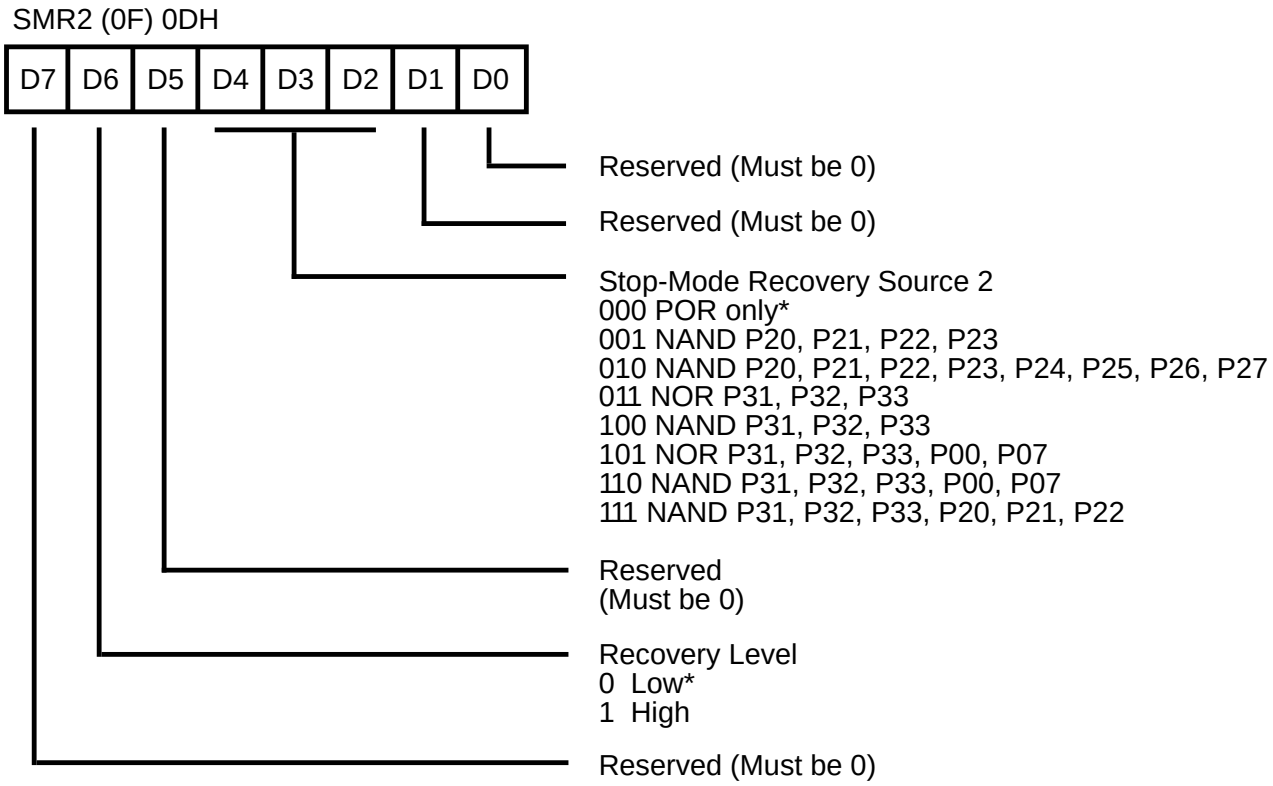
Figure 48. T16 Control Register
((0D) 2H: Read/Write Except Where Noted)

EXPANDED REGISTER FILE CONTROL REGISTERS (0F)



* Default Setting After Reset
** Default Setting After Reset and Stop-Mode Recovery

Figure 49. Stop-Mode Recovery Register ((0F) 0BH: D6-D0 = Write Only, D7 = Read Only)



Note: If used in conjunction with SMR, either of the two specified events will cause a Stop-Mode Recovery.

*Default Setting After Reset

Figure 50. Stop-Mode Recovery Register 2 ((0F) 0DH: D2-D4, D6 Write Only)

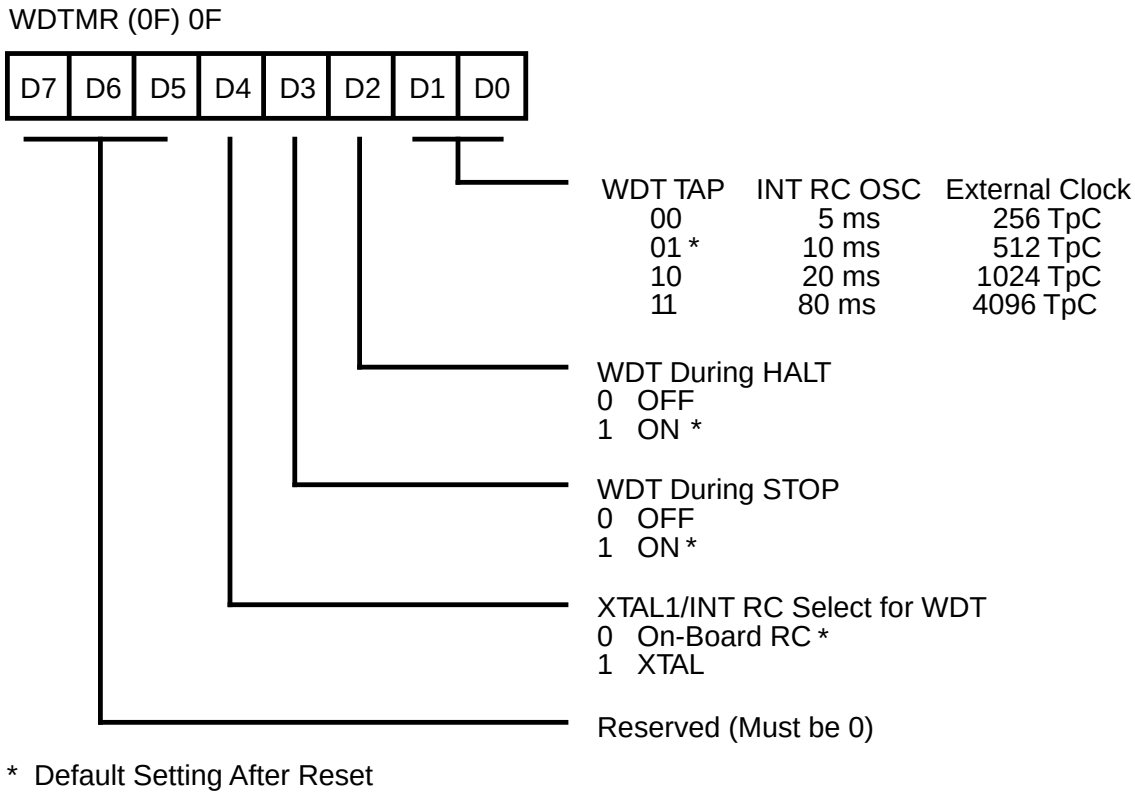


Figure 51. Watch-Dog Timer Register ((0F) 0FH: Write Only)

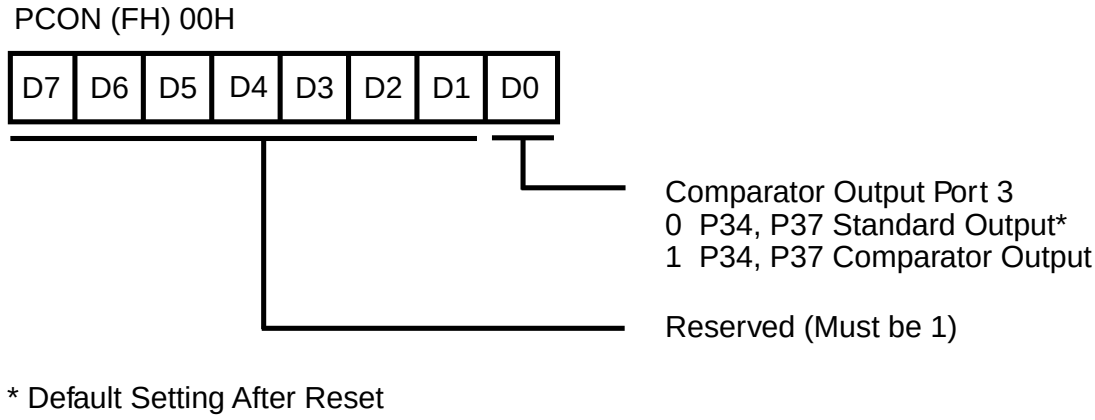


Figure 52. Port Configuration Register (PCON) ((0F) 0H: Write Only)

Z8 STANDARD CONTROL REGISTER DIAGRAMS

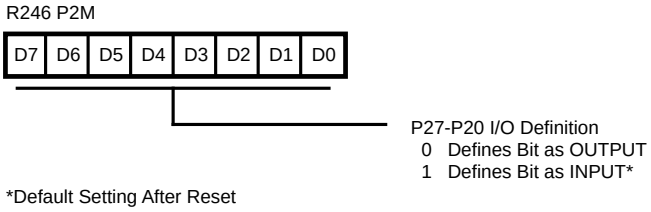


Figure 53. Port 2 Mode Register (F6H: Write Only)

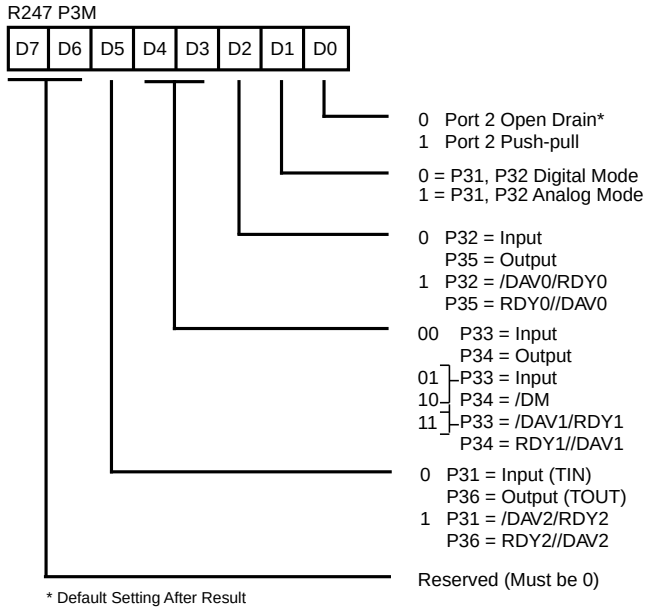


Figure 54. Port 3 Mode Register (F7H: Write Only)

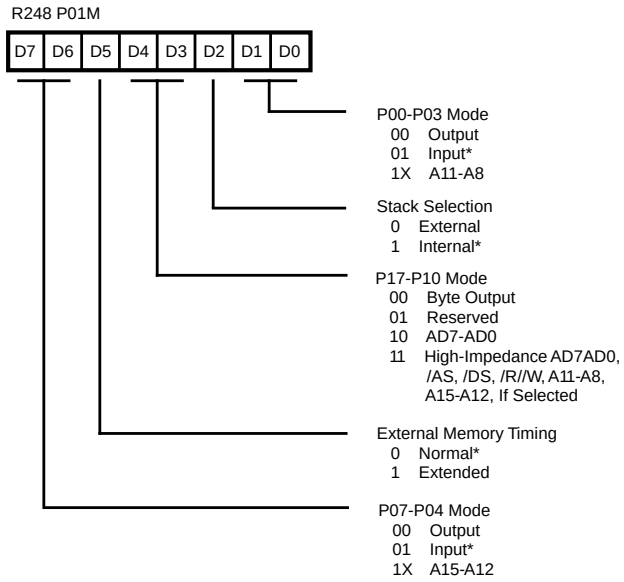


Figure 55. Port 0 and 1 Mode Register (F8H: Write Only)

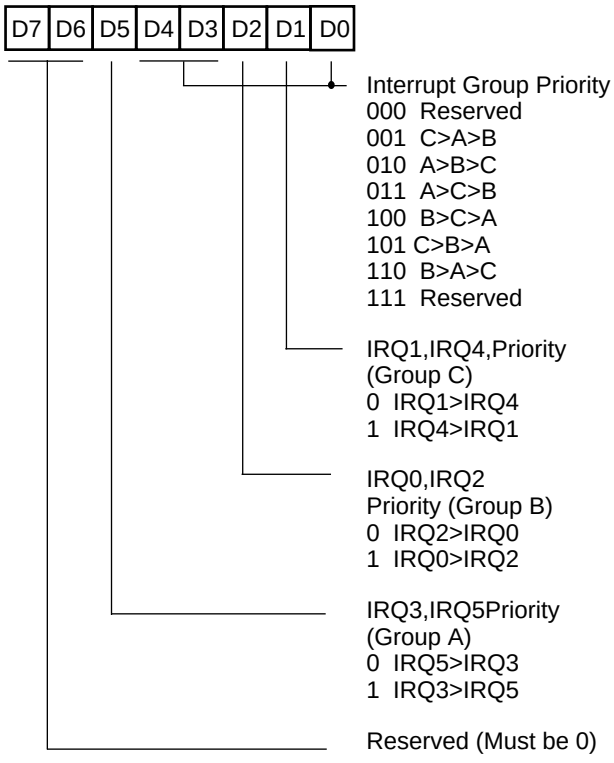


Figure 56. Interrupt Priority Registers ((0) F9H: Write Only)

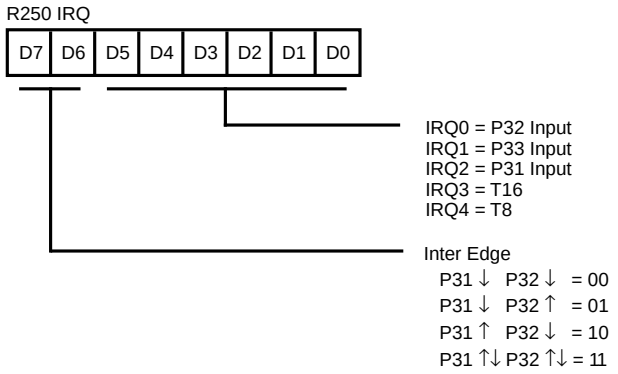


Figure 57. Interrupt Request Register ((0) FAH: Read/Write)

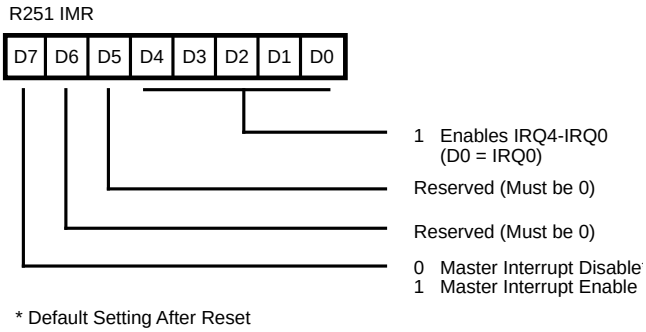


Figure 58. Interrupt Mask Register ((0) FBH: Read/Write)

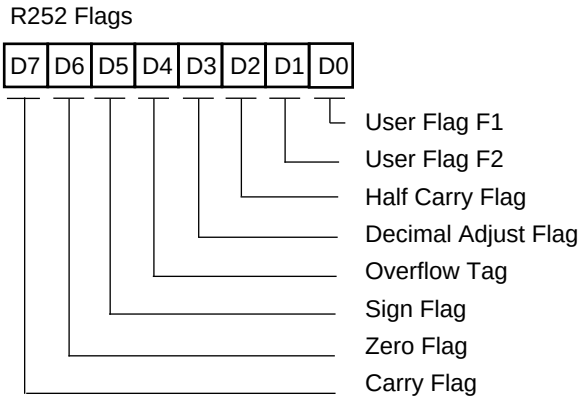


Figure 59. Flag Register ((0) FCH: Read/Write)

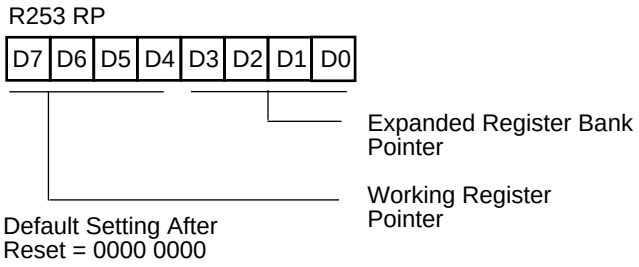


Figure 60. Register Pointer ((0) FDH: Read/Write)

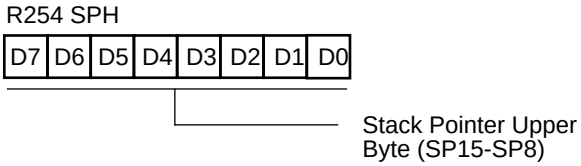


Figure 61. Stack Pointer High ((0) FEH: Read/Write)

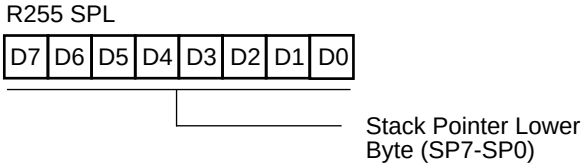
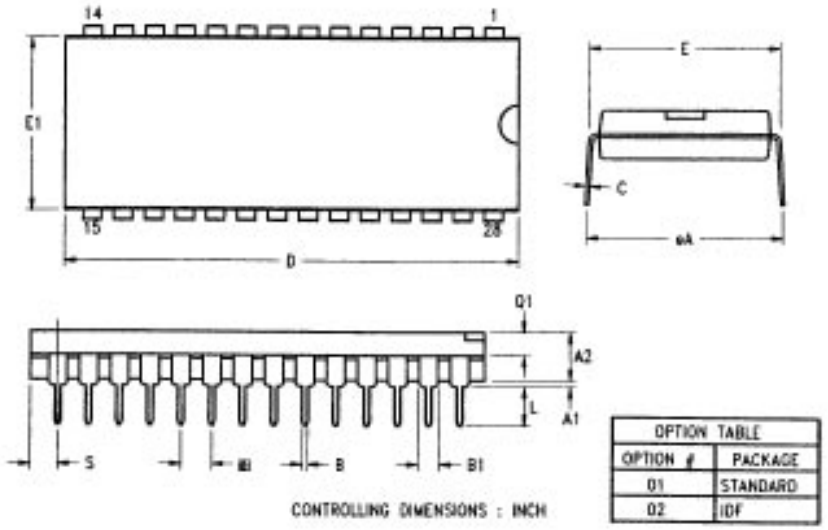


Figure 62. Stack Pointer Low ((0) FFH: Read/Write)

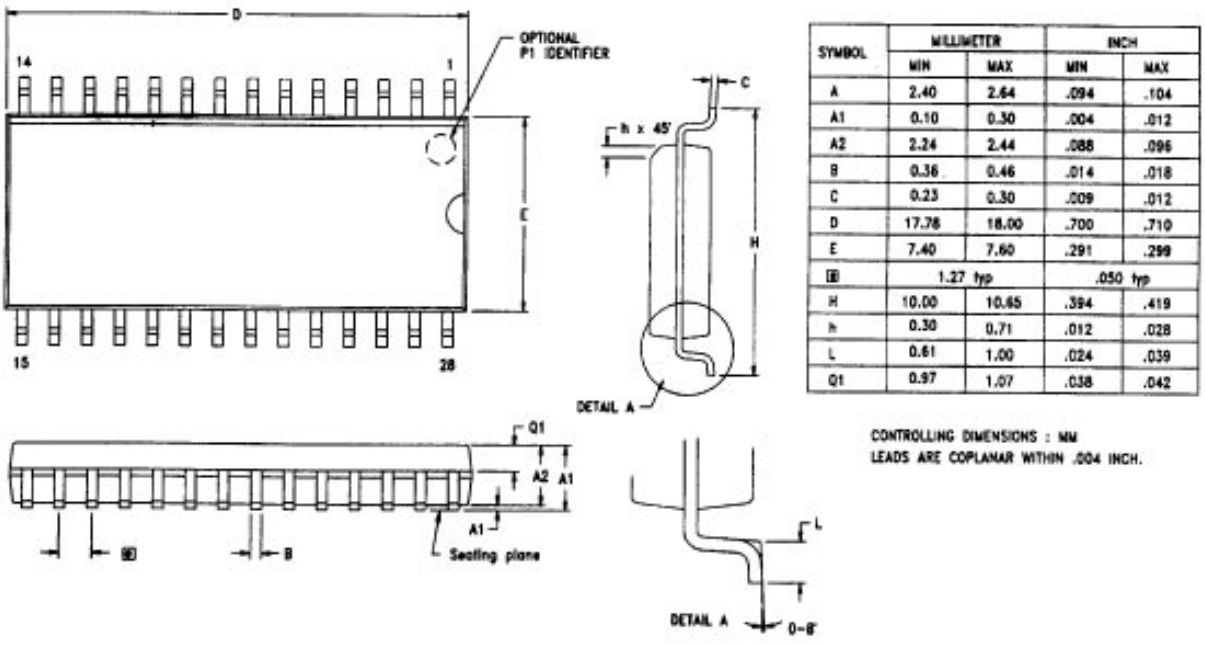
PACKAGE INFORMATION



SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

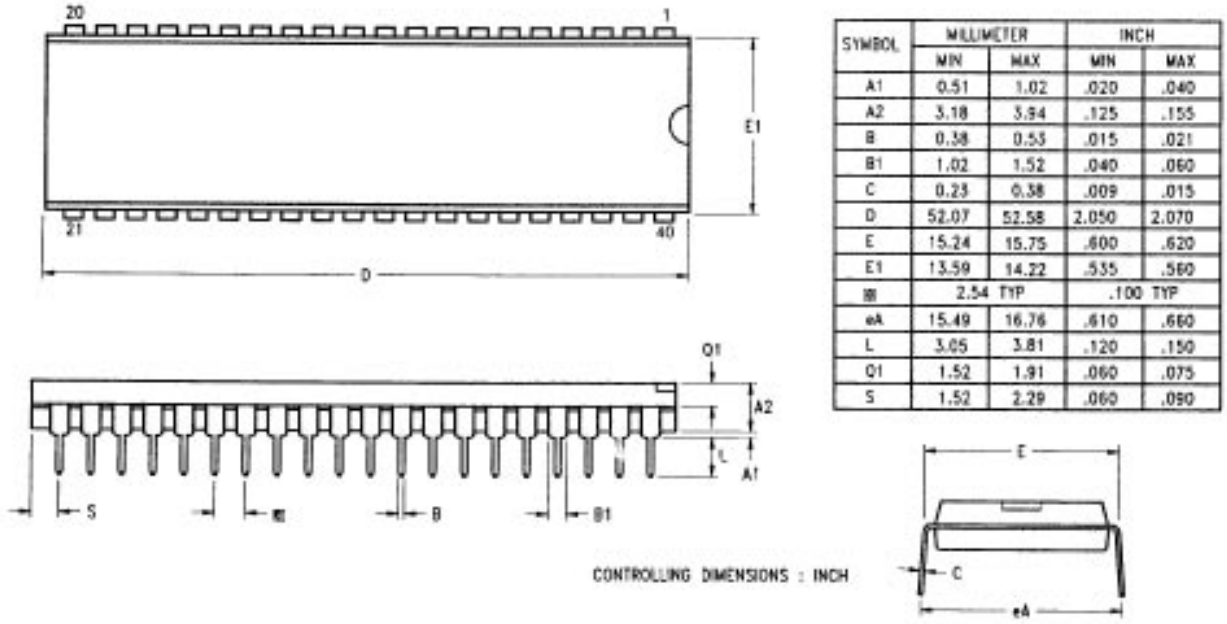
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

Figure 63. 28-Pin DIP Package Diagram



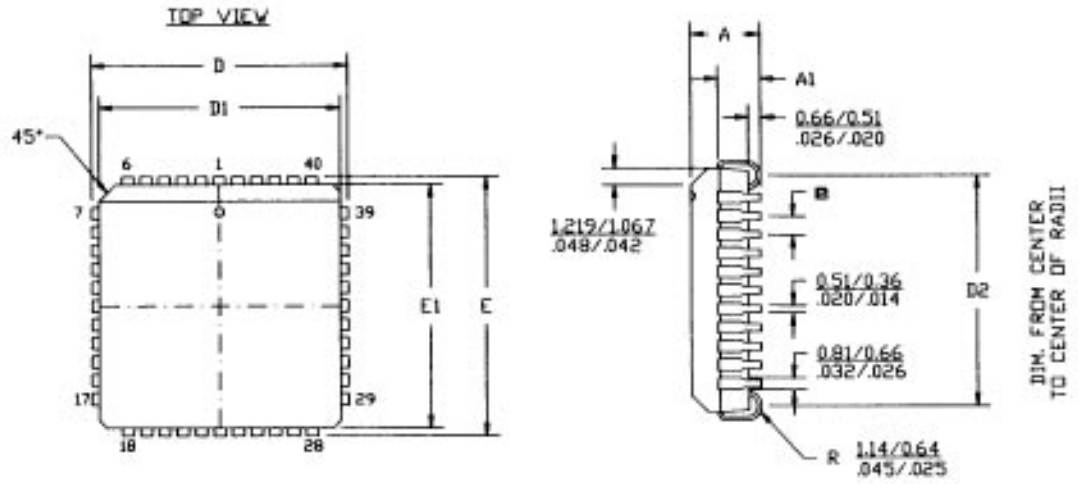
SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

Figure 64. 28-Pin SOIC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
eB	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

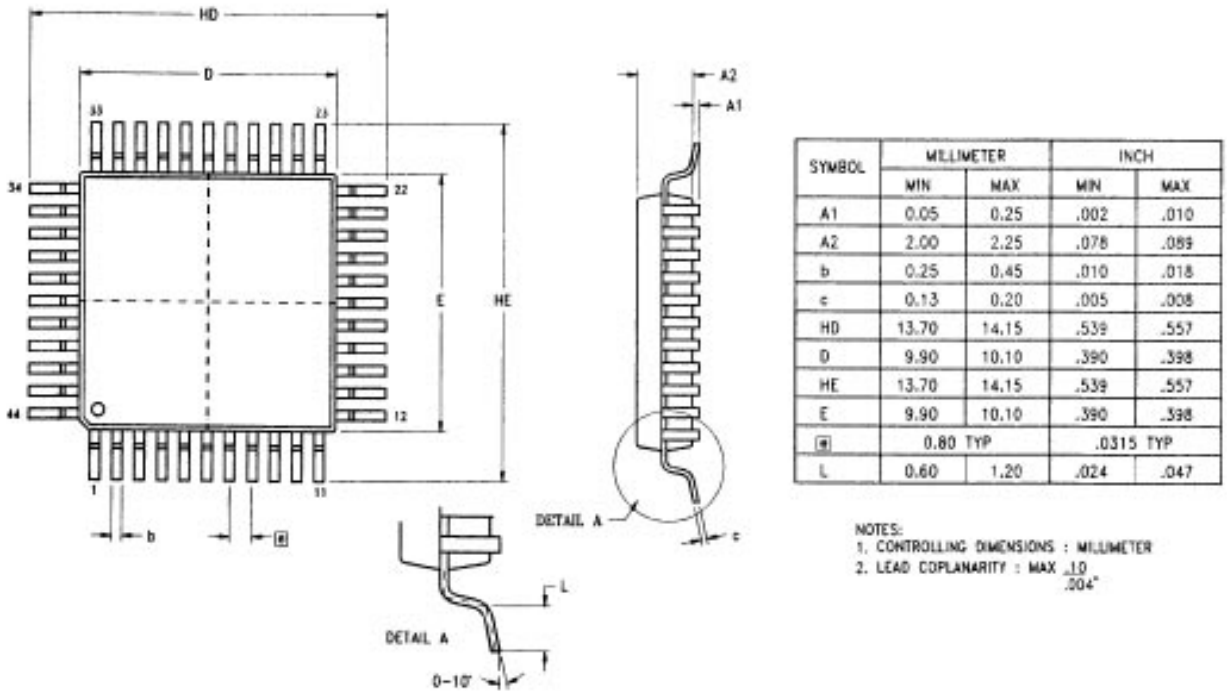
Figure 65. 40-Pin DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 66. 44-Pin PLCC Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX $\frac{.10}{.004"}$

Figure 67. 44-Pin QFP Package Diagram

ORDERING INFORMATION

Z86L88/81/86/87/89/73

8.0 MHz

28-Pin DIP	40-Pin DIP
Z86L8808PSC	Z86L8708PSC
Z86L8108PSC	Z86L8908PSC
Z86L8608PSC	Z86L7308PSC

28-Pin SIOC	44-Pin PLCC	44-Pin QFP
Z86L8808SSC	Z86L8708VSC	Z86L8708FSC
Z86L8108SSC	Z86L8908VSC	Z86L8908FSC
Z86L8608SSC	Z86L7308VSC	Z86L7308FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Codes

Package

P = Plastic DIP
F = Plastic Quad Flat Pack
V = Plastic Chip Carrier
S = SOIC (Small Outline Integrated Circuit)

Temperature

S = 0°C to +70°C

Speed

8 = 8.0 MHz

Environmental

C = Plastic Standard

Example:

Z 86LXX 08 P S C is a Z86LXX, 8 MHz, DIP, 0°C to +70°C, Plastic Standard Flow