

128XRGBX82 OUTPUT LCD DRIVER IC with built-in RAM

■ INSTRUCTION

HM17CM256 is a dot-Matrix LCD drive IC with 82 commons (80 + 2 icons) and 384 segments (128 X RGB) drive ports for 256 colors driving.

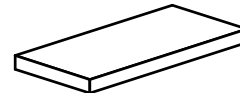
This IC stores the serial or parallel BIT data transferred by the microcomputer on the built-in RAM (81,920 bits for graphic + 2048 bits for icons) and generates the signals to drive LCD panel.

Color graphic display is achieved by selecting 8 gray (256 color) levels out of 32 gray palettes independently.

This IC is suitable for battery-operated system, hand-carrying information equipment by ensuring low power consumption, low power supply (1.7V ~) and a wide range of operating voltage.

And 164 x 128 display (maximum) is possible with master and slave application.

• EXTERNAL SHAPE



HM17CM256

■ FEATURES

- 256 color bitmap LCD driver
- LCD drive outputs 128xRGB segments, 80 commons for graphic and 2 commons for icons
- Display RAM capacity 81,920bits (for graphic usage)
2,048bits (for icon usage)
- Gradation display 8 gradations can be selected from 32 gradations by PWM control
- Black/White display 82 x (128 x 3) bits display is possible
- 8 bit BUS interface directly connectable with 68 / 80 series CPU
- RAM data length 8 BIT / 16 BIT selectable
- Serial interface available
- Programmable duty / bias ratio with command
- Various instruction set
 - display data read/write, display ON/OFF, positive/negative display, page address set
 - display start line address set, partial display, bias select,
 - column address set, all display ON/OFF, boosting selection, n line inversion mode
 - read modified write, power save ...
- Built-in voltage booster (programmable) : 7 x boosting
- Built-in voltage regulator
- Controllable contrast with built-in electric volume (128 steps)
- Low current consumption
- Logic supply 1.7V ~ 3.3V
- LCD drive supply 5.0V ~ 18.0V
- C-MOS silicon process
- Package bumped chip / bare chip

HM17CM256

■ PAD coordinates 1

chip size 19840 μ m x 2480 μ m (chip center : 0 μ m x 0 μ m)

PAD No.	Pin name	X(μ m)	Y(μ m)	PAD No.	Pin name	X (μ m)	Y (μ m)	PAD No.	Pin name	X (μ m)	Y (μ m)
1	DMY ₀ (L)	-9625	-1068	52	D ₁₀	-2550	-1068	103	C ₄₊ (L)	6120	-1068
2	DMY ₀ (R)	-9575	-1068	53	D ₁₁	-2380	-1068	104	C ₄₊ (R)	6290	-1068
3	COM ₆₇	-9525	-1068	54	D ₁₂	-2210	-1068	105	C ₄₋ (L)	6460	-1068
4	COM ₆₈	-9475	-1068	55	D ₁₃	-2040	-1068	106	C ₄₋ (R)	6630	-1068
5	COM ₆₉	-9425	-1068	56	D ₁₄	-1870	-1068	107	C ₅₊ (L)	6800	-1068
6	COM ₇₀	-9375	-1068	57	D ₁₅	-1700	-1068	108	C ₅₊ (R)	6970	-1068
7	COM ₇₁	-9325	-1068	58	V _{SS} (L)	-1472	-1068	109	C ₅₋ (L)	7140	-1068
8	COM ₇₂	-9275	-1068	59	V _{SS} (C)	-1340	-1068	110	C ₅₋ (R)	7310	-1068
9	COM ₇₃	-9225	-1068	60	V _{SS} (R)	-1190	-1068	111	C ₆₊ (L)	7480	-1068
10	COM ₇₄	-9175	-1068	61	CL	-1020	-1068	112	C ₆₊ (R)	7650	-1068
11	COM ₇₅	-9125	-1068	62	FLM	-850	-1068	113	C ₆₋ (L)	7820	-1068
12	COM ₇₆	-9075	-1068	63	FR	-680	-1068	114	C ₆₋ (R)	7990	-1068
13	COM ₇₇	-9025	-1068	64	CLK	-510	-1068	115	V _{LCD} (L)	8160	-1068
14	COM ₇₈	-8975	-1068	65	OSC ₁	-340	-1068	116	V _{LCD} (R)	8330	-1068
15	COM ₇₉	-8925	-1068	66	OSC ₂	-107	-1068	117	V _{OUT} (L)	8500	-1068
16	COM ₁	-8875	-1068	67	V _{SSH} (L)	74	-1068	118	V _{OUT} (R)	8670	-1068
17	V _{SSA} (L)	-8670	-1068	68	V _{SSH} (C)	196	-1068	119	COM ₃₉	8875	-1068
18	V _{SSA} (C)	-8500	-1068	69	V _{SSH} (R)	318	-1068	120	COM ₃₈	8925	-1068
19	V _{SSA} (R)	-8330	-1068	70	V _{LCD} (L)	510	-1068	121	COM ₃₇	8975	-1068
20	TEST	-8171	-1068	71	V _{LCD} (R)	680	-1068	122	COM ₃₆	9025	-1068
21	V _{DD} (L)	-7990	-1068	72	V ₁ (L)	850	-1068	123	COM ₃₅	9075	-1068
22	V _{DD} (C)	-7820	-1068	73	V ₁ (R)	1020	-1068	124	COM ₃₄	9125	-1068
23	V _{DD} (R)	-7650	-1068	74	V ₂ (L)	1190	-1068	125	COM ₃₃	9175	-1068
24	RES	-7480	-1068	75	V ₂ (R)	1360	-1068	126	COM ₃₂	9225	-1068
25	CS	-7310	-1068	76	V ₃ (L)	1530	-1068	127	COM ₃₁	9275	-1068
26	RS	-7140	-1068	77	V ₃ (R)	1700	-1068	128	COM ₃₀	9325	-1068
27	V _{SS} (L)	-6970	-1068	78	V ₄ (L)	1870	-1068	129	COM ₂₉	9375	-1068
28	V _{SS} (C)	-6800	-1068	79	V ₄ (R)	2040	-1068	130	COM ₂₈	9425	-1068
29	V _{SS} (R)	-6630	-1068	80	V _{REG} (L)	2210	-1068	131	COM ₂₇	9475	-1068
30	M/S	-6448	-1068	81	V _{REG} (R)	2380	-1068	132	COM ₂₆	9525	-1068
31	V _{DDA}	-6290	-1068	82	V _{BA} (L)	2550	-1068	133	DMY ₁ (L)	9575	-1068
32	P/S	-6120	-1068	83	V _{BA} (R)	2693	-1068	134	DMY ₁ (R)	9625	-1068
33	SEL68	-5950	-1068	84	V _{REF}	2879	-1068	135	DMY ₂ (L)	9726	-900
34	V _{SSA} (L)	-5780	-1068	85	V _{EE} (L)	3060	-1068	136	DMY ₂ (R)	9726	-850
35	V _{SSA} (C)	-5610	-1068	86	V _{EE} (C)	3230	-1068	137	COM ₂₅	9726	-800
36	V _{SSA} (R)	-5440	-1068	87	V _{EE} (R)	3400	-1068	138	COM ₂₄	9726	-750
37	WR	-5270	-1068	88	V _{SSH} (L)	3570	-1068	139	COM ₂₃	9726	-700
38	RD	-5111	-1068	89	V _{SSH} (C)	3740	-1068	140	COM ₂₂	9726	-650
39	V _{DD} (L)	-4930	-1068	90	V _{SSH} (R)	3910	-1068	141	COM ₂₁	9726	-600
40	V _{DD} (C)	-4760	-1068	91	C ₁₊ (L)	4102	-1068	142	COM ₂₀	9726	-550
41	V _{DD} (R)	-4590	-1068	92	C ₁₊ (R)	4250	-1068	143	COM ₁₉	9726	-500
42	D ₀ /SCL	-4420	-1068	93	C ₁₋ (L)	4420	-1068	144	COM ₁₈	9726	-450
43	D ₁ /SDA	-4250	-1068	94	C ₁₋ (R)	4590	-1068	145	COM ₁₇	9726	-400
44	D ₂ /EXCS	-3995	-1068	95	C ₂₊ (L)	4760	-1068	146	COM ₁₆	9726	-350
45	D ₃ /SMODE	-3740	-1068	96	C ₂₊ (R)	4930	-1068	147	COM ₁₅	9726	-300
46	D ₄ /SPOL	-3570	-1068	97	C ₂₋ (L)	5100	-1068	148	COM ₁₄	9726	-250
47	D ₅	-3400	-1068	98	C ₂₋ (R)	5270	-1068	149	COM ₁₃	9726	-200
48	D ₆	-3230	-1068	99	C ₃₊ (L)	5440	-1068	150	COM ₁₂	9726	-150
49	D ₇	-3060	-1068	100	C ₃₊ (R)	5610	-1068	151	COM ₁₁	9726	-100
50	D ₈	-2890	-1068	101	C ₃₋ (L)	5780	-1068	152	COM ₁₀	9726	-50
51	D ₉	-2720	-1068	102	C ₃₋ (R)	5950	-1068	153	COM ₉	9726	0

■ PAD coordiantes 2

chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
154	COM ₈	9726	50	205	SEGB ₁₀	8025	1068	256	SEGB ₂₇	5475	1068
155	COM ₇	9726	100	206	SEGC ₁₀	7975	1068	257	SEGC ₂₇	5425	1068
156	COM ₆	9726	150	207	SEGA ₁₁	7925	1068	258	SEGA ₂₈	5375	1068
157	COM ₅	9726	200	208	SEGB ₁₁	7875	1068	259	SEGB ₂₈	5325	1068
158	COM ₄	9726	250	209	SEGC ₁₁	7825	1068	260	SEGC ₂₈	5275	1068
159	COM ₃	9726	300	210	SEGA ₁₂	7775	1068	261	SEGA ₂₉	5225	1068
160	COM ₂	9726	350	211	SEGB ₁₂	7725	1068	262	SEGB ₂₉	5175	1068
161	COM ₁	9726	400	212	SEGC ₁₂	7675	1068	263	SEGC ₂₉	5125	1068
162	COM ₀	9726	450	213	SEGA ₁₃	7625	1068	264	SEGA ₃₀	5075	1068
163	COM ₀	9726	500	214	SEGB ₁₃	7575	1068	265	SEGB ₃₀	5025	1068
164	SEGS _{A0}	9726	550	215	SEGC ₁₃	7525	1068	266	SEGC ₃₀	4975	1068
165	SEGS _{B0}	9726	600	216	SEGA ₁₄	7475	1068	267	SEGA ₃₁	4925	1068
166	SEGS _{C0}	9726	650	217	SEGB ₁₄	7425	1068	268	SEGB ₃₁	4875	1068
167	SEGS _{A1}	9726	700	218	SEGC ₁₄	7375	1068	269	SEGC ₃₁	4825	1068
168	SEGS _{B1}	9726	750	219	SEGA ₁₅	7325	1068	270	SEGA ₃₂	4775	1068
169	SEGS _{C1}	9726	800	220	SEGB ₁₅	7275	1068	271	SEGB ₃₂	4725	1068
170	DMY _{3(L)}	9726	850	221	SEGC ₁₅	7225	1068	272	SEGC ₃₂	4675	1068
171	DMY _{3(R)}	9726	900	222	SEGA ₁₆	7175	1068	273	SEGA ₃₃	4625	1068
172	DMY _{4(L)}	9675	1068	223	SEGB ₁₆	7125	1068	274	SEGB ₃₃	4575	1068
173	DMY _{4(R)}	9625	1068	224	SEGC ₁₆	7075	1068	275	SEGC ₃₃	4525	1068
174	SEGA ₀	9575	1068	225	SEGA ₁₇	7025	1068	276	SEGA ₃₄	4475	1068
175	SEGB ₀	9525	1068	226	SEGB ₁₇	6975	1068	277	SEGB ₃₄	4425	1068
176	SEGC ₀	9475	1068	227	SEGC ₁₇	6925	1068	278	SEGC ₃₄	4375	1068
177	SEGA ₁	9425	1068	228	SEGA ₁₈	6875	1068	279	SEGA ₃₅	4325	1068
178	SEGB ₁	9375	1068	229	SEGB ₁₈	6825	1068	280	SEGB ₃₅	4275	1068
179	SEGC ₁	9325	1068	230	SEGC ₁₈	6775	1068	281	SEGC ₃₅	4225	1068
180	SEGA ₂	9275	1068	231	SEGA ₁₉	6725	1068	282	SEGA ₃₆	4175	1068
181	SEGB ₂	9225	1068	232	SEGB ₁₉	6675	1068	283	SEGB ₃₆	4125	1068
182	SEGC ₂	9175	1068	233	SEGC ₁₉	6625	1068	284	SEGC ₃₆	4075	1068
183	SEGA ₃	9125	1068	234	SEGA ₂₀	6575	1068	285	SEGA ₃₇	4025	1068
184	SEGB ₃	9075	1068	235	SEGB ₂₀	6525	1068	286	SEGB ₃₇	3975	1068
185	SEGC ₃	9025	1068	236	SEGC ₂₀	6475	1068	287	SEGC ₃₇	3925	1068
186	SEGA ₄	8975	1068	237	SEGA ₂₁	6425	1068	288	SEGA ₃₈	3875	1068
187	SEGB ₄	8925	1068	238	SEGB ₂₁	6375	1068	289	SEGB ₃₈	3825	1068
188	SEGC ₄	8875	1068	239	SEGC ₂₁	6325	1068	290	SEGC ₃₈	3775	1068
189	SEGA ₅	8825	1068	240	SEGA ₂₂	6275	1068	291	SEGA ₃₉	3725	1068
190	SEGB ₅	8775	1068	241	SEGB ₂₂	6225	1068	292	SEGB ₃₉	3675	1068
191	SEGC ₅	8725	1068	242	SEGC ₂₂	6175	1068	293	SEGC ₃₉	3625	1068
192	SEGA ₆	8675	1068	243	SEGA ₂₃	6125	1068	294	SEGA ₄₀	3575	1068
193	SEGB ₆	8625	1068	244	SEGB ₂₃	6075	1068	295	SEGB ₄₀	3525	1068
194	SEGC ₆	8575	1068	245	SEGC ₂₃	6025	1068	296	SEGC ₄₀	3475	1068
195	SEGA ₇	8525	1068	246	SEGA ₂₄	5975	1068	297	SEGA ₄₁	3425	1068
196	SEGB ₇	8475	1068	247	SEGB ₂₄	5925	1068	298	SEGB ₄₁	3375	1068
197	SEGC ₇	8425	1068	248	SEGC ₂₄	5875	1068	299	SEGC ₄₁	3325	1068
198	SEGA ₈	8375	1068	249	SEGA ₂₅	5825	1068	300	SEGA ₄₂	3275	1068
199	SEGB ₈	8325	1068	250	SEGB ₂₅	5775	1068	301	SEGB ₄₂	3225	1068
200	SEGC ₈	8275	1068	251	SEGC ₂₅	5725	1068	302	SEGC ₄₂	3175	1068
201	SEGA ₉	8225	1068	252	SEGA ₂₆	5675	1068	303	SEGA ₄₃	3125	1068
202	SEGB ₉	8175	1068	253	SEGB ₂₆	5625	1068	304	SEGB ₄₃	3075	1068
203	SEGC ₉	8125	1068	254	SEGC ₂₆	5575	1068	305	SEGC ₄₃	3025	1068
204	SEGA ₁₀	8075	1068	255	SEGA ₂₇	5525	1068	306	SEGA ₄₄	2975	1068

HM17CM256

PAD coordinates 3

chip size 19840 μ m x 2480 μ m (chip center : 0 μ m x 0 μ m)

PAD No.	Pin name	X(μ m)	Y(μ m)	PAD No.	Pin name	X (μ m)	Y (μ m)	PAD No.	Pin name	X (μ m)	Y (μ m)
307	SEGB ₄₄	2925	1068	358	SEGB ₆₁	375	1068	409	SEGB ₇₈	-2175	1068
308	SEGC ₄₄	2875	1068	359	SEGC ₆₁	325	1068	410	SEGC ₇₈	-2225	1068
309	SEGA ₄₅	2825	1068	360	SEGA ₆₂	275	1068	411	SEGA ₇₉	-2275	1068
310	SEGB ₄₅	2775	1068	361	SEGB ₆₂	225	1068	412	SEGB ₇₉	-2325	1068
311	SEGC ₄₅	2725	1068	362	SEGC ₆₂	175	1068	413	SEGC ₇₉	-2375	1068
312	SEGA ₄₆	2675	1068	363	SEGA ₆₃	125	1068	414	SEGA ₈₀	-2425	1068
313	SEGB ₄₆	2625	1068	364	SEGB ₆₃	75	1068	415	SEGB ₈₀	-2475	1068
314	SEGC ₄₆	2575	1068	365	SEGC ₆₃	25	1068	416	SEGC ₈₀	-2525	1068
315	SEGA ₄₇	2525	1068	366	SEGA ₆₄	-25	1068	417	SEGA ₈₁	-2575	1068
316	SEGB ₄₇	2475	1068	367	SEGB ₆₄	-75	1068	418	SEGB ₈₁	-2625	1068
317	SEGC ₄₇	2425	1068	368	SEGC ₆₄	-125	1068	419	SEGC ₈₁	-2675	1068
318	SEGA ₄₈	2375	1068	369	SEGA ₆₅	-175	1068	420	SEGA ₈₂	-2725	1068
319	SEGB ₄₈	2325	1068	370	SEGB ₆₅	-225	1068	421	SEGB ₈₂	-2775	1068
320	SEGC ₄₈	2275	1068	371	SEGC ₆₅	-275	1068	422	SEGC ₈₂	-2825	1068
321	SEGA ₄₉	2225	1068	372	SEGA ₆₆	-325	1068	423	SEGA ₈₃	-2875	1068
322	SEGB ₄₉	2175	1068	373	SEGB ₆₆	-375	1068	424	SEGB ₈₃	-2925	1068
323	SEGC ₄₉	2125	1068	374	SEGC ₆₆	-425	1068	425	SEGC ₈₃	-2975	1068
324	SEGA ₅₀	2075	1068	375	SEGA ₆₇	-475	1068	426	SEGA ₈₄	-3025	1068
325	SEGB ₅₀	2025	1068	376	SEGB ₆₇	-525	1068	427	SEGB ₈₄	-3075	1068
326	SEGC ₅₀	1975	1068	377	SEGC ₆₇	-575	1068	428	SEGC ₈₄	-3125	1068
327	SEGA ₅₁	1925	1068	378	SEGA ₆₈	-625	1068	429	SEGA ₈₅	-3175	1068
328	SEGB ₅₁	1875	1068	379	SEGB ₆₈	-675	1068	430	SEGB ₈₅	-3225	1068
329	SEGC ₅₁	1825	1068	380	SEGC ₆₈	-725	1068	431	SEGC ₈₅	-3275	1068
330	SEGA ₅₂	1775	1068	381	SEGA ₆₉	-775	1068	432	SEGA ₈₆	-3325	1068
331	SEGB ₅₂	1725	1068	382	SEGB ₆₉	-825	1068	433	SEGB ₈₆	-3375	1068
332	SEGC ₅₂	1675	1068	383	SEGC ₆₉	-875	1068	434	SEGC ₈₆	-3425	1068
333	SEGA ₅₃	1625	1068	384	SEGA ₇₀	-925	1068	435	SEGA ₈₇	-3475	1068
334	SEGB ₅₃	1575	1068	385	SEGB ₇₀	-975	1068	436	SEGB ₈₇	-3525	1068
335	SEGC ₅₃	1525	1068	386	SEGC ₇₀	-1025	1068	437	SEGC ₈₇	-3575	1068
336	SEGA ₅₄	1475	1068	387	SEGA ₇₁	-1075	1068	438	SEGA ₈₈	-3625	1068
337	SEGB ₅₄	1425	1068	388	SEGB ₇₁	-1125	1068	439	SEGB ₈₈	-3675	1068
338	SEGC ₅₄	1375	1068	389	SEGC ₇₁	-1175	1068	440	SEGC ₈₈	-3725	1068
339	SEGA ₅₅	1325	1068	390	SEGA ₇₂	-1225	1068	441	SEGA ₈₉	-3775	1068
340	SEGB ₅₅	1275	1068	391	SEGB ₇₂	-1275	1068	442	SEGB ₈₉	-3825	1068
341	SEGC ₅₅	1225	1068	392	SEGC ₇₂	-1325	1068	443	SEGC ₈₉	-3875	1068
342	SEGA ₅₆	1175	1068	393	SEGA ₇₃	-1375	1068	444	SEGA ₉₀	-3925	1068
343	SEGB ₅₆	1125	1068	394	SEGB ₇₃	-1425	1068	445	SEGB ₉₀	-3975	1068
344	SEGC ₅₆	1075	1068	395	SEGC ₇₃	-1475	1068	446	SEGC ₉₀	-4025	1068
345	SEGA ₅₇	1025	1068	396	SEGA ₇₄	-1525	1068	447	SEGA ₉₁	-4075	1068
346	SEGB ₅₇	975	1068	397	SEGB ₇₄	-1575	1068	448	SEGB ₉₁	-4125	1068
347	SEGC ₅₇	925	1068	398	SEGC ₇₄	-1625	1068	449	SEGC ₉₁	-4175	1068
348	SEGA ₅₈	875	1068	399	SEGA ₇₅	-1675	1068	450	SEGA ₉₂	-4225	1068
349	SEGB ₅₈	825	1068	400	SEGB ₇₅	-1725	1068	451	SEGB ₉₂	-4275	1068
350	SEGC ₅₈	775	1068	401	SEGC ₇₅	-1775	1068	452	SEGC ₉₂	-4325	1068
351	SEGA ₅₉	725	1068	402	SEGA ₇₆	-1825	1068	453	SEGA ₉₃	-4375	1068
352	SEGB ₅₉	675	1068	403	SEGB ₇₆	-1875	1068	454	SEGB ₉₃	-4425	1068
353	SEGC ₅₉	625	1068	404	SEGC ₇₆	-1925	1068	455	SEGC ₉₃	-4475	1068
354	SEGA ₆₀	575	1068	405	SEGA ₇₇	-1975	1068	456	SEGA ₉₄	-4525	1068
355	SEGB ₆₀	525	1068	406	SEGB ₇₇	-2025	1068	457	SEGB ₉₄	-4575	1068
356	SEGC ₆₀	475	1068	407	SEGC ₇₇	-2075	1068	458	SEGC ₉₄	-4625	1068
357	SEGA ₆₁	425	1068	408	SEGA ₇₈	-2125	1068	459	SEGA ₉₅	-4675	1068

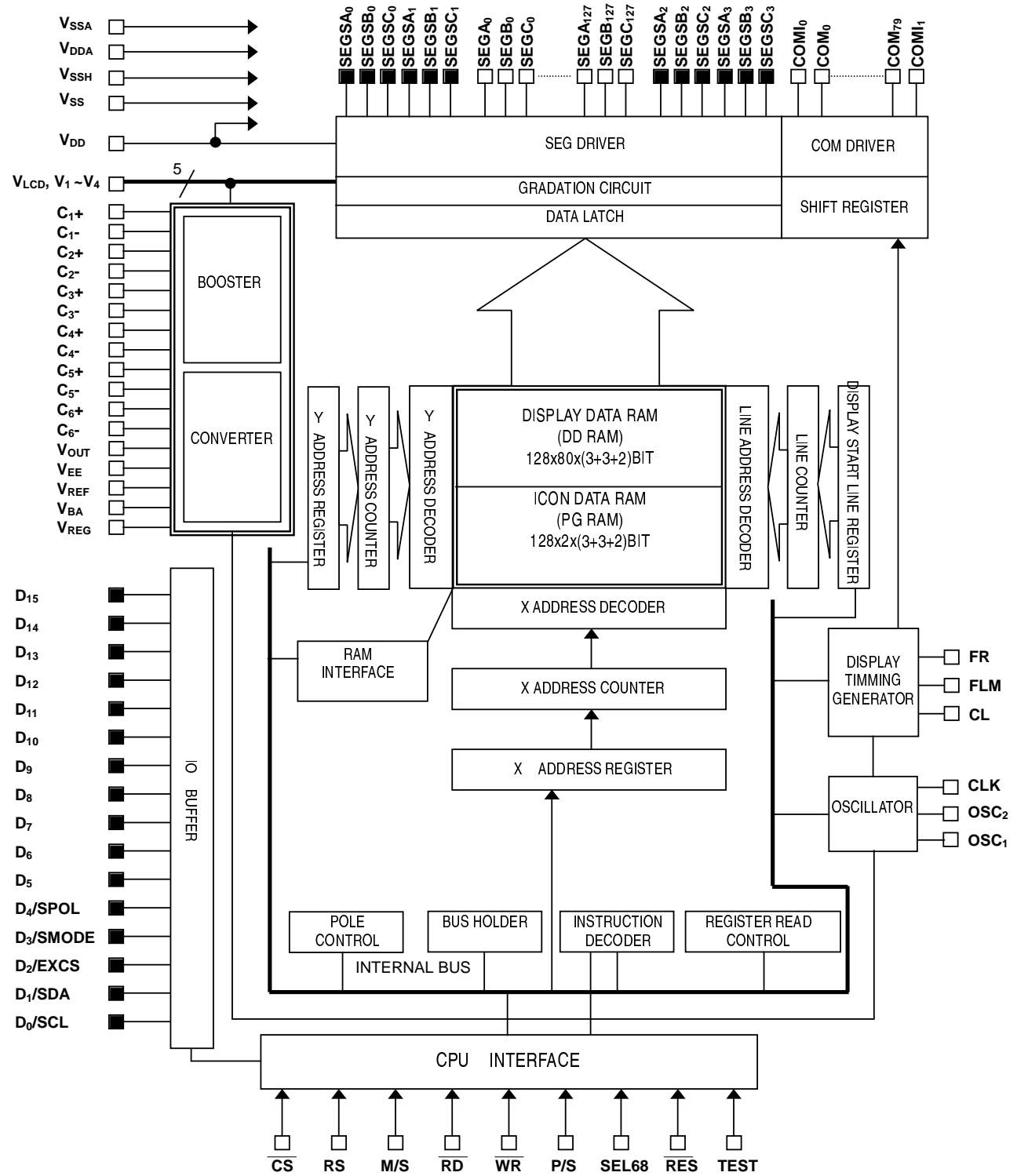
■ PAD coordinates 4

chip size 19840μm x 2480μm (chip center : 0μm x 0μm)

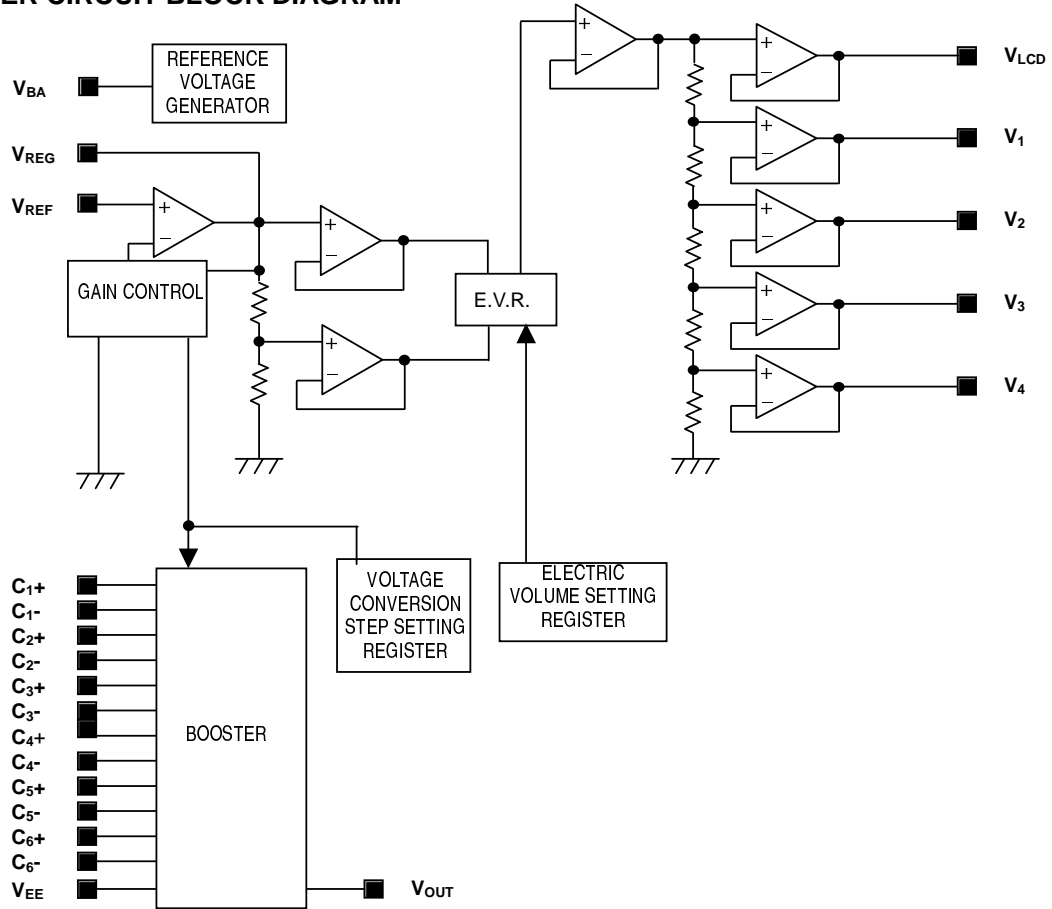
PAD No.	Pin name	X(μm)	Y(μm)	PAD No.	Pin name	X (μm)	Y (μm)	PAD No.	Pin name	X (μm)	Y (μm)
460	SEGB ₉₅	-4725	1068	511	SEGB ₁₁₂	-7275	1068	562	SEGSA ₂	-9726	800
461	SEGC ₉₅	-4775	1068	512	SEGC ₁₁₂	-7325	1068	563	SEGSB ₂	-9726	750
462	SEGA ₉₆	-4825	1068	513	SEGA ₁₁₃	-7375	1068	564	SEGSC ₂	-9726	700
463	SEGB ₉₆	-4875	1068	514	SEGB ₁₁₃	-7425	1068	565	SEGSA ₃	-9726	650
464	SEGC ₉₆	-4925	1068	515	SEGC ₁₁₃	-7475	1068	566	SEGSB ₃	-9726	600
465	SEGA ₉₇	-4975	1068	516	SEGA ₁₁₄	-7525	1068	567	SEGSC ₃	-9726	550
466	SEGB ₉₇	-5025	1068	517	SEGB ₁₁₄	-7575	1068	568	COM ₄₀	-9726	500
467	SEGC ₉₇	-5075	1068	518	SEGC ₁₁₄	-7625	1068	569	COM ₄₁	-9726	450
468	SEGA ₉₈	-5125	1068	519	SEGA ₁₁₅	-7675	1068	570	COM ₄₂	-9726	400
469	SEGB ₉₈	-5175	1068	520	SEGB ₁₁₅	-7725	1068	571	COM ₄₃	-9726	350
470	SEGC ₉₈	-5225	1068	521	SEGC ₁₁₅	-7775	1068	572	COM ₄₄	-9726	300
471	SEGA ₉₉	-5275	1068	522	SEGA ₁₁₆	-7825	1068	573	COM ₄₅	-9726	250
472	SEGB ₉₉	-5325	1068	523	SEGB ₁₁₆	-7875	1068	574	COM ₄₆	-9726	200
473	SEGC ₉₉	-5375	1068	524	SEGC ₁₁₆	-7925	1068	575	COM ₄₇	-9726	150
474	SEGA ₁₀₀	-5425	1068	525	SEGA ₁₁₇	-7975	1068	576	COM ₄₈	-9726	100
475	SEGB ₁₀₀	-5475	1068	526	SEGB ₁₁₇	-8025	1068	577	COM ₄₉	-9726	50
476	SEGC ₁₀₀	-5525	1068	527	SEGC ₁₁₇	-8075	1068	578	COM ₅₀	-9726	0
477	SEGA ₁₀₁	-5575	1068	528	SEGA ₁₁₈	-8125	1068	579	COM ₅₁	-9726	-50
478	SEGB ₁₀₁	-5625	1068	529	SEGB ₁₁₈	-8175	1068	580	COM ₅₂	-9726	-100
479	SEGC ₁₀₁	-5675	1068	530	SEGC ₁₁₈	-8225	1068	581	COM ₅₃	-9726	-150
480	SEGA ₁₀₂	-5725	1068	531	SEGA ₁₁₉	-8275	1068	582	COM ₅₄	-9726	-200
481	SEGB ₁₀₂	-5775	1068	532	SEGB ₁₁₉	-8325	1068	583	COM ₅₅	-9726	-250
482	SEGC ₁₀₂	-5825	1068	533	SEGC ₁₁₉	-8375	1068	584	COM ₅₆	-9726	-300
483	SEGA ₁₀₃	-5875	1068	534	SEGA ₁₂₀	-8425	1068	585	COM ₅₇	-9726	-350
484	SEGB ₁₀₃	-5925	1068	535	SEGB ₁₂₀	-8475	1068	586	COM ₅₈	-9726	-400
485	SEGC ₁₀₃	-5975	1068	536	SEGC ₁₂₀	-8525	1068	587	COM ₅₉	-9726	-450
486	SEGA ₁₀₄	-6025	1068	537	SEGA ₁₂₁	-8575	1068	588	COM ₆₀	-9726	-500
487	SEGB ₁₀₄	-6075	1068	538	SEGB ₁₂₁	-8625	1068	589	COM ₆₁	-9726	-550
488	SEGC ₁₀₄	-6125	1068	539	SEGC ₁₂₁	-8675	1068	590	COM ₆₂	-9726	-600
489	SEGA ₁₀₅	-6175	1068	540	SEGA ₁₂₂	-8725	1068	591	COM ₆₃	-9726	-650
490	SEGB ₁₀₅	-6225	1068	541	SEGB ₁₂₂	-8775	1068	592	COM ₆₄	-9726	-700
491	SEGC ₁₀₅	-6275	1068	542	SEGC ₁₂₂	-8825	1068	593	COM ₆₅	-9726	-750
492	SEGA ₁₀₆	-6325	1068	543	SEGA ₁₂₃	-8875	1068	594	COM ₆₆	-9726	-800
493	SEGB ₁₀₆	-6375	1068	544	SEGB ₁₂₃	-8925	1068	595	DMY ₇ (L)	-9726	-850
494	SEGC ₁₀₆	-6425	1068	545	SEGC ₁₂₃	-8975	1068	596	DMY ₇ (R)	-9726	-900
495	SEGA ₁₀₇	-6475	1068	546	SEGA ₁₂₄	-9025	1068				
496	SEGB ₁₀₇	-6525	1068	547	SEGB ₁₂₄	-9075	1068				
497	SEGC ₁₀₇	-6575	1068	548	SEGC ₁₂₄	-9125	1068				
498	SEGA ₁₀₈	-6625	1068	549	SEGA ₁₂₅	-9175	1068				
499	SEGB ₁₀₈	-6675	1068	550	SEGB ₁₂₅	-9225	1068				
500	SEGC ₁₀₈	-6725	1068	551	SEGC ₁₂₅	-9275	1068				
501	SEGA ₁₀₉	-6775	1068	552	SEGA ₁₂₆	-9325	1068				
502	SEGB ₁₀₉	-6825	1068	553	SEGB ₁₂₆	-9375	1068				
503	SEGC ₁₀₉	-6875	1068	554	SEGC ₁₂₆	-9425	1068				
504	SEGA ₁₁₀	-6925	1068	555	SEGA ₁₂₇	-9475	1068				
505	SEGB ₁₁₀	-6975	1068	556	SEGB ₁₂₇	-9525	1068				
506	SEGC ₁₁₀	-7025	1068	557	SEGC ₁₂₇	-9575	1068				
507	SEGA ₁₁₁	-7075	1068	558	DMY ₅ (L)	-9625	1068				
508	SEGB ₁₁₁	-7125	1068	559	DMY ₅ (R)	-9675	1068				
509	SEGC ₁₁₁	-7175	1068	560	DMY ₆ (L)	-9726	900				
510	SEGA ₁₁₂	-7225	1068	561	DMY ₆ (R)	-9726	850				

HM17CM256

BLOCK DIAGRAM



POWER CIRCUIT BLOCK DIAGRAM



HM17CM256

■ PIN DESCRIPTION 1

No.	NAME	I/O	FUNCTION
21,22,23, 39,40,41	V _{DD}	supply	Power pin for logic
27,28,29, 58,59,60	V _{SS}	supply	GND pin for logic
67,68,69, 88,89,90	V _{SSH}	supply	High voltage GND pin
31	V _{DDA}	supply	This pin is internally connected to V _{DD} pin. This pin is used when the voltage of each input pin is fixed to V _{DD} level. <i>caution) Do not use to main power pin.</i>
17,18,19, 34,35,36	V _{SSA}	supply	This pin is internally connected to V _{SS} pin. This pin is used when the voltage of each input pin is fixed to V _{SS} level. <i>caution) Do not use to main power pin.</i>
70,71,115,116 72,73 74,75 76,77 78,79	V _{LCD} V ₁ V ₂ V ₃ V ₄	supply/O	LCD driver supply voltage <ul style="list-style-type: none"> LCD driver power supply port when external power supply is used. When external power is used, voltages should have following relations. $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD}$ V_{LCD}, V₁~V₄ voltages are generated by voltage booster at master mode operation under power circuit ON. When internal power supply is used, capacitors must be connected between V_{LCD}, V₁~V₄ and V_{SS}.
91,92 93,94	C ₁₊ C ₁₋	O	Capacitor connection pin for voltage converter
95,96 97,98	C ₂₊ C ₂₋	O	Capacitor connection pin for voltage converter
99,100 101,102	C ₃₊ C ₃₋	O	Capacitor connection pin for voltage converter
103,104 105,106	C ₄₊ C ₄₋	O	Capacitor connection pin for voltage converter
107,108 109,110	C ₅₊ C ₅₋	O	Capacitor connection pin for voltage converter
111,112 113,114	C ₆₊ C ₆₋	O	Capacitor connection pin for voltage converter
82,83	V _{BA}	O	Reference voltage output pin for voltage regulating.
84	V _{REF}	I	Reference voltage input pin for voltage regulating.
85,86,87	V _{EE}	supply	Voltage supply pin for boosted voltage generation. V _{DD} level at normal status.
117,118	V _{OUT}	supply/O	Internal DC/DC converter output pin.
80,81	V _{REG}	O	Voltage regulator output pin.
24	$\overline{\text{RES}}$	I	Reset pin Reset when RES= "L"

■ PIN DESCRIPTION 2

No.	NAME	I/O	FUNCTION						
42	D ₀ /SCL	I/O	<ul style="list-style-type: none"> When parallel interface is selected (P/S="H"), data line is connected to MPU data bus with 8bit bi-directional bus When serial interface is selected (P/S="L"), D₀ and D₁(SCL, SDA) are used as serial interface pins and various sets are taken by serial interface use mode of D₂, D₃, D₄. SDA : serial data input pin SCL : data transfer clock EXCS : extension chip selection I/O pin SMODE : serial transfer mode setting input pin SPOL : RS polarity selection pin when 3 line serial interface is selected. SDA data is shifted at the rising edge of SCL Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8 th clock of SCL. Set to "L" after data transfer or during non-access time						
43	D ₁ /SDA	I/O							
44	D ₂ /EXCS	I/O							
45	D ₃ /SMODE	I/O							
46	D ₄ /SPOL	I/O							
47,48,49	D ₅ ,D ₆ ,D ₇	I/O							
50,51,52,53 54,55,56,57	D ₈ ,D ₉ ,D ₁₀ ,D ₁₁ , D ₁₂ ,D ₁₃ ,D ₁₄ ,D ₁₅	I/O	Connect to data bus to MPU with 8bit bi-directional bus. Used as MSB 8bit data bus in the 16bit data RAM transfer mode Set to "L" or "H" when not used.						
25	$\overline{\text{CS}}$	I	Chip selection pin. Data in-out is possible when CS = "L".						
26	RS	I	Input data selection pin. Distinguish bus data from CPU whether instruction or display data. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>RS</td> <td>H</td> <td>L</td> </tr> <tr> <td>class</td> <td>instruction</td> <td>display data</td> </tr> </table>	RS	H	L	class	instruction	display data
RS	H	L							
class	instruction	display data							
38	$\overline{\text{RD}}$ (E)	I	<80 series CPU interface (P/S="H",SEL68="L")> RD signal connection port of 80 series CPU. Data bus goes to output state at $\overline{\text{RD}}$ = "L". <68 series CPU interface (P/S="H",SEL68="H")> Enable signal connection port of 68 series CPU. Active status when this signal is at "H".						
37	$\overline{\text{WR}}$ (R/W)	I	<80 series CPU interface (P/S="H",SEL68="L")> WR signal connection port of 80 series CPU. Active at "L" and data bus signal is taken at the rising edge of WR. <68 series CPU interface (P/S="H",SEL68="H")> Read write control signal , R/W connection port of 68-series MPU. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>R/W</td> <td>H</td> <td>L</td> </tr> <tr> <td>status</td> <td>read</td> <td>write</td> </tr> </table>	R/W	H	L	status	read	write
R/W	H	L							
status	read	write							

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■ PIN DESCRIPTION 3

No.	NAME	I/O	FUNCTION																		
33	SEL68	I	CPU interface selection port <table border="1"> <tr> <td>SEL68</td> <td>H</td> <td>L</td> </tr> <tr> <td>status</td> <td>68 series</td> <td>80 series</td> </tr> </table>	SEL68	H	L	status	68 series	80 series												
SEL68	H	L																			
status	68 series	80 series																			
32	P/S	I	Serial / parallel interface selection port <table border="1"> <tr> <td>P/S</td> <td>chip select</td> <td>data/ command</td> <td>data</td> <td>read/ write</td> <td>serial clock</td> </tr> <tr> <td>H</td> <td>\overline{CS}</td> <td>RS</td> <td>D₀~D₇</td> <td>\overline{RD}, \overline{WR}</td> <td>-</td> </tr> <tr> <td>L</td> <td>\overline{CS}</td> <td>RS</td> <td>SDA(D₁)</td> <td>write only</td> <td>SCL (D₀)</td> </tr> </table> <p>※ P/S = "L" :serial interface selection ,D15~D5 goes to Hi-Z state. Fix \overline{RD}, \overline{WR} to "H" or "L".</p>	P/S	chip select	data/ command	data	read/ write	serial clock	H	\overline{CS}	RS	D ₀ ~D ₇	\overline{RD} , \overline{WR}	-	L	\overline{CS}	RS	SDA(D ₁)	write only	SCL (D ₀)
P/S	chip select	data/ command	data	read/ write	serial clock																
H	\overline{CS}	RS	D ₀ ~D ₇	\overline{RD} , \overline{WR}	-																
L	\overline{CS}	RS	SDA(D ₁)	write only	SCL (D ₀)																
20	TEST	I	Test port. Fix to "L".																		
61	CL	I/O	Latching signal pin of display data. Display line counter is counted up at the rising edge and LCD driving signal is generated at the falling edge <table border="1"> <tr> <td>M/S</td> <td>status</td> <td>CL</td> </tr> <tr> <td>H</td> <td>master</td> <td>output</td> </tr> <tr> <td>L</td> <td>slave</td> <td>input</td> </tr> </table>	M/S	status	CL	H	master	output	L	slave	input									
M/S	status	CL																			
H	master	output																			
L	slave	input																			
62	FLM	I/O	LCD synchronous signal (first line marker) I/O pin. Display start address is loaded in the display line counter at FLM = "H". <table border="1"> <tr> <td>M/S</td> <td>status</td> <td>FLM</td> </tr> <tr> <td>H</td> <td>master</td> <td>output</td> </tr> <tr> <td>L</td> <td>slave</td> <td>input</td> </tr> </table>	M/S	status	FLM	H	master	output	L	slave	input									
M/S	status	FLM																			
H	master	output																			
L	slave	input																			
63	FR	I/O	Alternated display signal of LCD driver output I/O pin. <table border="1"> <tr> <td>M/S</td> <td>status</td> <td>FR</td> </tr> <tr> <td>H</td> <td>master</td> <td>output</td> </tr> <tr> <td>L</td> <td>slave</td> <td>input</td> </tr> </table>	M/S	status	FR	H	master	output	L	slave	input									
M/S	status	FR																			
H	master	output																			
L	slave	input																			
30	M/S	I	Master / slave mode selection pin <table border="1"> <tr> <td>M/S</td> <td>mode</td> <td>oscillator</td> <td>Power supply</td> </tr> <tr> <td>H</td> <td>master</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>L</td> <td>slave</td> <td>disable</td> <td>disable</td> </tr> </table> <p>Fix to "H" or "L" according to operating mode.</p>	M/S	mode	oscillator	Power supply	H	master	enable	enable	L	slave	disable	disable						
M/S	mode	oscillator	Power supply																		
H	master	enable	enable																		
L	slave	disable	disable																		

PIN DESCRIPTION 4

No.	NAME	I/O	FUNCTION															
174~557	SEGA₀~SEGA₁₂₇, SEGB₀~SEGB₁₂₇, SEGC₀~SEGC₁₂₇	O	Segment drive port Segment output from display RAM data <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 30%;">mode</th> <th style="width: 35%;">Non-lighted</th> <th style="width: 35%;">lighted</th> </tr> </thead> <tbody> <tr> <td>Normal</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> </tr> <tr> <td>Reverse</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> </tr> </tbody> </table> The output level is selected among V_{LCD} , V_2 , V_3 , V_{SS} by the combination of FR signal and RAM data (B/W mode) <div style="margin-top: 10px;"> </div>	mode	Non-lighted	lighted	Normal	0	1	Reverse	1	0						
mode	Non-lighted	lighted																
Normal	0	1																
Reverse	1	0																
164~169, 562~567	SEGSA₀~SEGSA₃, SEGSB₀~SEGSB₃, SEGSC₀~SEGSC₃	O	Dummy segment driver output Located at both side of segment drivers, used for edge display.															
162~137, 132~119, 568~594, 3~15	COM₀~COM₇₉	O	Common driver output The output level is selected among V_{LCD} , V_1 , V_4 and V_{SS} by the combination of FR and scan data. <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">data</th> <th style="width: 20%;">FR</th> <th style="width: 60%;">Output level</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td style="text-align: center;">V_{SS}</td> </tr> <tr> <td>L</td> <td>H</td> <td style="text-align: center;">V_1</td> </tr> <tr> <td>H</td> <td>L</td> <td style="text-align: center;">V_{LCD}</td> </tr> <tr> <td>L</td> <td>L</td> <td style="text-align: center;">V_4</td> </tr> </tbody> </table>	data	FR	Output level	H	H	V_{SS}	L	H	V_1	H	L	V_{LCD}	L	L	V_4
data	FR	Output level																
H	H	V_{SS}																
L	H	V_1																
H	L	V_{LCD}																
L	L	V_4																
163	COMI₀	O	Common drive output for icon display															
16	COMI₁	O	Common drive output for icon display															
65, 66	OSC₁, OSC₂	I O	External reference clock input pin Open when using internal oscillator clock or used as slave device. In this case, OSC ₁ goes to V_{SS} level. Connect external oscillating source to OSC ₁ port or connect resistor between OSC ₁ and OSC ₂ when using external oscillator.															
64	CLK	I/O	Input / output pin for display timing clock Output clock from master device is applied to slave chip through CLK pin when used as master / slave mode. <table border="1" style="margin: 10px auto; border-collapse: collapse;"> <thead> <tr> <th style="width: 15%;">M/S</th> <th style="width: 35%;">mode</th> <th style="width: 50%;">CLK</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>master</td> <td style="text-align: center;">output</td> </tr> <tr> <td>L</td> <td>slave</td> <td style="text-align: center;">input*</td> </tr> </tbody> </table> <p style="text-align: right; margin-top: 5px;">*input from master chip's CLK output</p>	M/S	mode	CLK	H	master	output	L	slave	input*						
M/S	mode	CLK																
H	master	output																
L	slave	input*																

(port No. 1,2,133,134,135,136,170,171,172,173,558,559,560,561,595,596 is dummy port.)

HM17CM256

■ FUNCTION DESCRIPTION

(1) CPU interface

(1-1) Selection of interface type

HM17CM256 receives data through 8 bit parallel I/O(D₀~D₇), 16 bit parallel I/O(D₀~D₁₅) or divided into serial data input (SDA, SCL). Parallel or serial selection is decided by P/S pin setting. Parallel or serial selection is possible as following table.

Reading out from internal register or RAM is not possible at serial interface mode.

TABLE

P/S	Type	\overline{CS}	RS	\overline{RD}	\overline{WR}	SEL68	SDA	SCL	data
H	Parallel input	\overline{CS}	RS	\overline{RD}	\overline{WR}	SEL68			D ₀ ~D ₇ (D ₀ ~D ₁₅)
L	Serial input	\overline{CS}	RS	-	-	-	SDA	SCL	-

caution 1) "-" mark item : Fix to "H" or "L"

(1-2) Parallel input

In the parallel interface mode selected by P/S port, parallel data is transferred from the 8bit/16bit MPU through data bus. SEL68 port setting makes 80-series or 68-series interface selection

TABLE

SEL68	CPU type	\overline{CS}	RS	\overline{RD}	\overline{WR}	data
H	68 series CPU	\overline{CS}	RS	E	R/W	D ₀ ~D ₇ (D ₀ ~D ₁₅)
L	80 series CPU	\overline{CS}	RS	\overline{RD}	\overline{WR}	D ₀ ~D ₇ (D ₀ ~D ₁₅)

(1-3) Data identification

Combinations of RS, \overline{RD} , and \overline{WR} signals identify contents of 8bit data bus.

TABLE

RS	68 series	80 series		FUNCTION
	R/W	\overline{RD}	\overline{WR}	
1	1	0	1	Read out from internal register
1	0	1	0	Write in to internal register
0	1	0	1	Read display data
0	0	1	0	Write display data

(1-4) Serial interface

2 types of serial interface (3 line type mode, 4 line type mode) are available by selecting SMODE pin.

TABEL

SMODE	Serial interface mode
H	3 line type
L	4 line type

(1-5) 4 line type serial interface

4 line serial interface by SDA and SCL is possible at chip selection state (\overline{CS} ="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Serial input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of D_7, \dots, D_1, D_0 and converted into 8-bit parallel data at the rising edge of 8th serial clock.

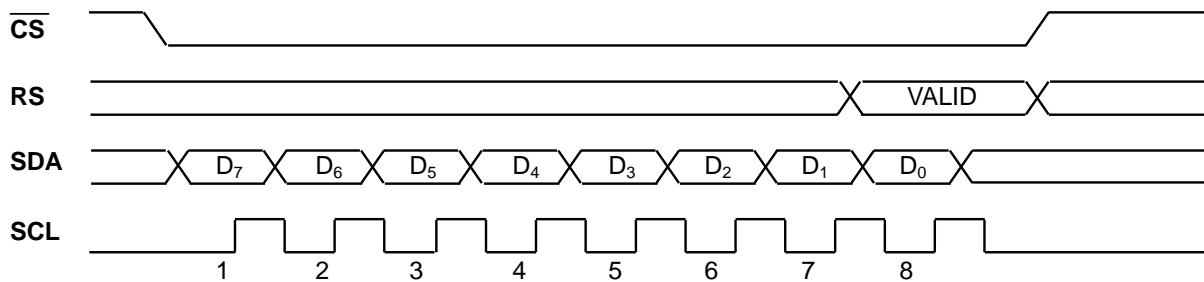
Serial data (SDA) are identified to display data or command by RS input.

TABLE

RS	Data contents
H	command
L	Display data

Make serial clock (SCL) "L" at the non-access period and after 8bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent mal-function, chip selector state should be released (\overline{CS} = "H") after 8bit data transfer as shown in the following figure.



4 line serial interface

(1-6) 3 line type serial interface

3-line serial interface by SDA and SCL is possible at chip selection state (\overline{CS} ="L")

When chip is not selected, internal shift register and counter are reset to initial value.

Input data from SDA are latched at the rising edge of serial clock (SCL) in the sequence of RS, D_7, \dots, D_1, D_0 , and converted to 8bit parallel data and handled at the rising edge of 9th serial clock.

Serial data (SDA) are identified to display data or command by RS bit data at the rising of first serial clock (SCL) and state of command data bit polarity shift pin (SPOL).

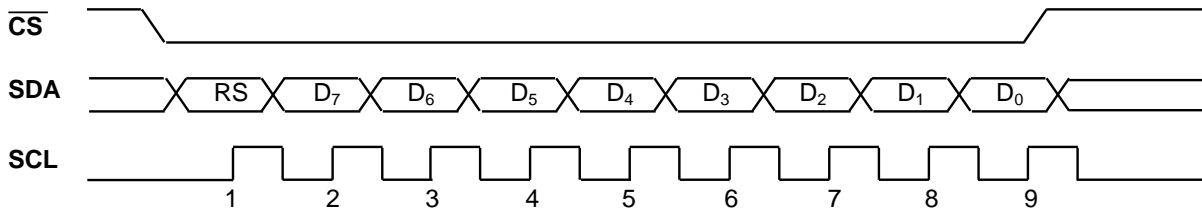
TABLE

SPOL=L		SPOL=H	
RS	Data identify	RS	Data identify
L	Display data	L	command
H	command	H	Display data

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Serial clock (SCL) should go to "L" at the non-access period and after 9bit data transfer.

SDA and SCL signals are sensitive to external noise. To prevent miss operation chip selector state should be released ($\overline{CS} = "H"$) after 9bit data transfer as shown in the following figure.



3line serial interface

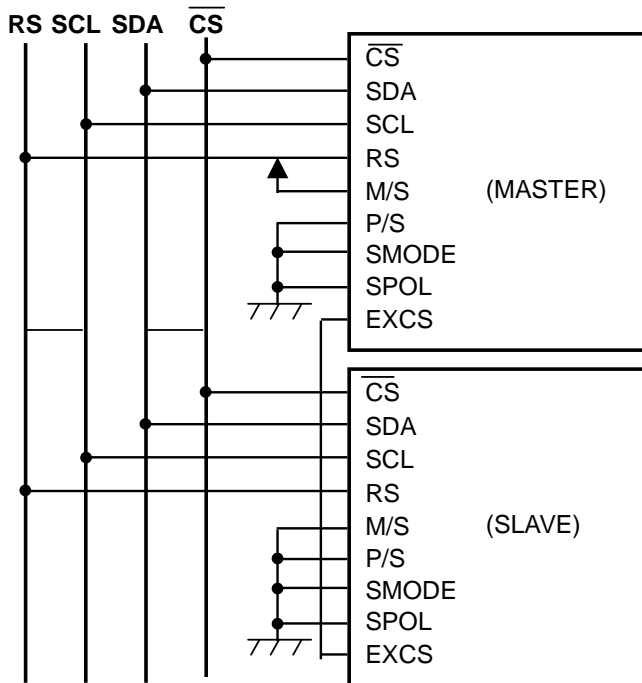
(1-7) One systematization of \overline{CS} when serial interface is selected

In the multi-chip operation (master/slave) mode with serial I/F connection, one \overline{CS} signal controls two chips to reduce control signal.

Connect extended chip selection port (EXCS) of master chip to EXCS port (input at slave device and output at master device mode) of slave chip.

When EXCS is "L", master chip cannot accept command except for EXCS control; at this point, only slave chip can be controlled.

Slave device control is possible when $\overline{CS} = "L"$ period within EXCS = "L" state.



EXCS: expand \overline{CS} signal (input port)

Master device : output port

Slave device : input port

P/S: parallel . serial selection port

(input port)

P/S=0: serial I/F

P/S=1: parallel I/F

M/S: master . slave selection port

(input port)

M/S=0: slave operation

M/S=1: master operation

SMODE: serial I/Fmode selection port

(input port)

SMODE=0: 4 line serial I/F

SMODE=1: 3 line serial I/F

SPOL: command data bit polarity selection port

(input port)

At 3 line serial I/F mode

Access display RAM at SPOL=0:RS=0

Access display RAM at SPOL=1:RS=1

(2) DDRAM and internal register access

DDRAM and internal register are accessed by data bus $D_0 \sim D_7$ ($D_0 \sim D_{15}$), chip select pin (\overline{CS}), DDRAM / register select pin (RS), read / write control pin (RD) or \overline{WR} pin.

When $\overline{CS} = "H"$, it is in non-selective state and DDRAM and internal register access is impossible. During access, Set $\overline{CS} = "L"$.

Access selection to DDRAM or internal register is controlled by RS input.

TABLE

RS	Data contents
L	Display RAM data
H	Internal command register

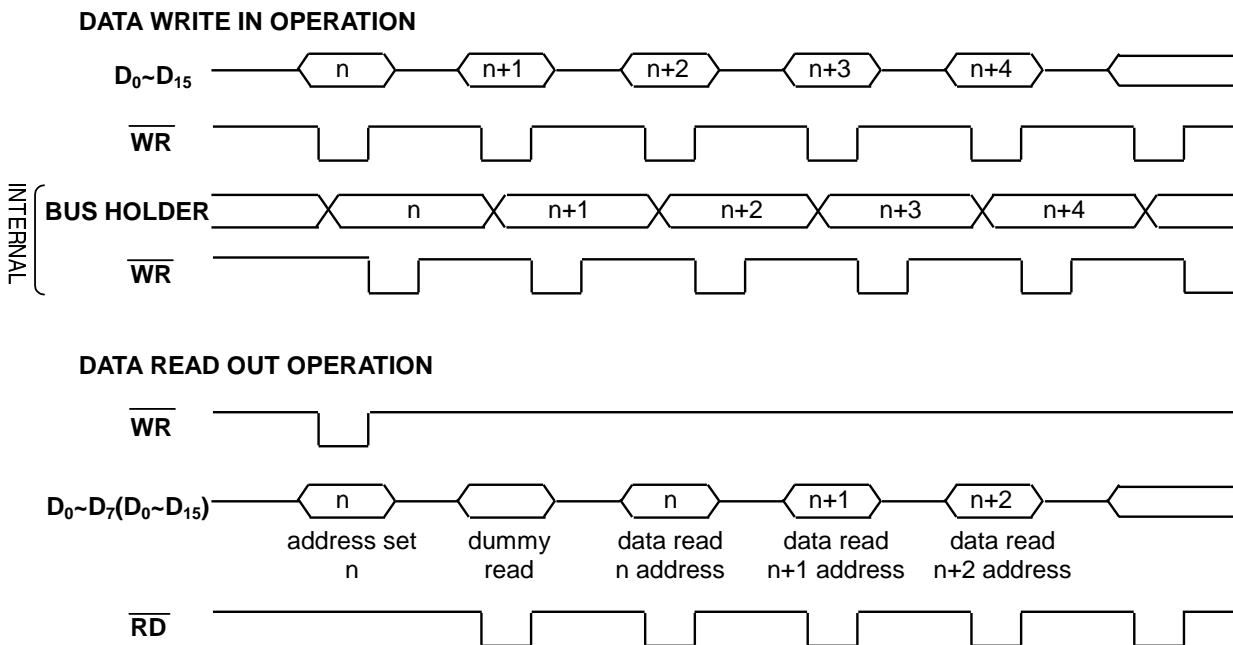
Write process starts after address setting and then the data on the 8bit data bus $D_0 \sim D_7$ or 16bit data bus $D_0 \sim D_{15}$ will be written in by CPU. The data is written at the rising edge of \overline{WR} (80 series) or falling edge of E (68 series).

Internally, bus holder data is processed to data bus and data are written to bus holder from CPU until next cycle.

After address setting, data of assigned address are read at the 1st and 3rd clock, which means it needs dummy read at the 2nd clock.

There are rules at reading data out of display RAM, after address setting, the data of assigned address is shown directly after the end of the read command, so pay attention that assigned data is available at 2nd timing step.

In other words, 1 cycle dummy read is needed after address setting and write cycle.



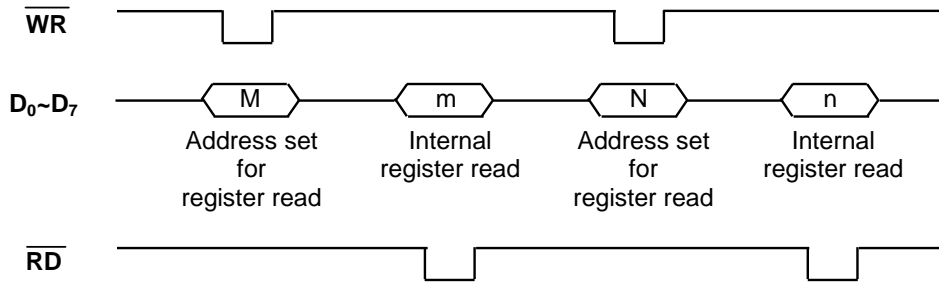
caution) When 16 bit mode, do write in and read out by 16 bit not only RAM access but also command setting.

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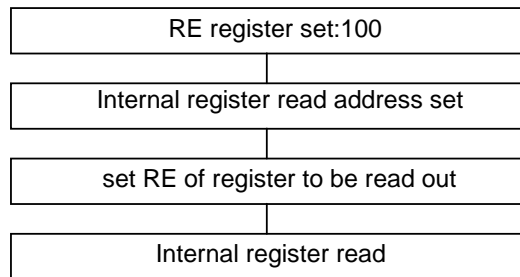
(3) Read out of internal register

Read out is possible not only from DDRAM, but also from the internal register. Addresses for read (0~F_H) are allocated in each register.

Read out is executed after writing read-out register address to internal register.



Internal register read out sequence



When register is read out, upper 4 bit data are "1111".

Non-used bits of active registers are "0".

When non-used registers are read out, upper 4 bits are "1111" and lower 4 bits are "0000".

(4) 16 bit data access to DDRAM

It is possible to write in DDRAM by 16-bits access with the data of 16 bits data bus D₀~D₁₅. 16 bits data access mode is possible by setting the value of WLS register to "1".

TABEL

WLS	Access mode
L	8 bit
H	16 bit

Each command should be set to 8-bits(D₀~D₇) as well as to 16-bit access mode.

16-bit access is available at display RAM access.

(5) Display start line register

When displaying the DDRAM data, it is the contents of Y address register that is corresponding to display start line.

The data of Y address is displayed on the display start line depending on the value of the shift command register and the display start line register.

The data of this register are preset to the display line counter per FLM signal transition.

Line counter is counted up in synchronization with CL input and generates line address that read out 384bit data from DDRAM to LCD driver circuit.

(6) DDRAM addressing

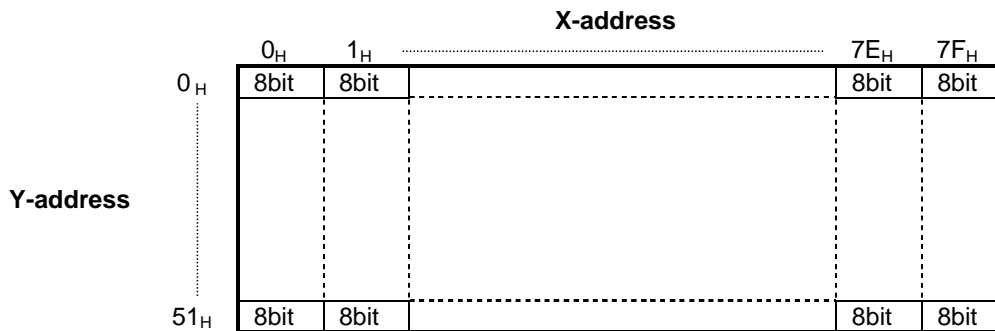
This IC includes display memory Bit mapped that is composed of 1024 bit of X direction (8bit×128) and 82bit of Y direction.

In gray mode, neighboring 3-bit data or 2-bit data are displayed by segment driver with 8 grays or 4 grays, respectively.

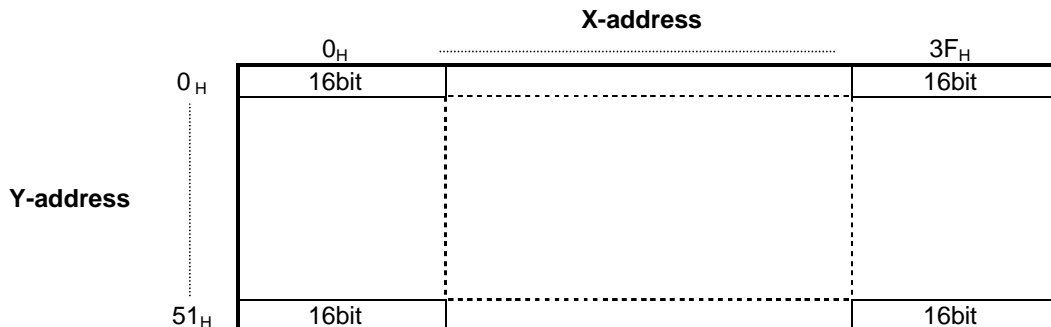
3 outputs of segment driver compose 1 pixel of RGB and 128×82 pixels are displayed with 256 color (8gray×8gray×4gray).

Address area of X direction is varied according to accessed data length. The area of X direction is 0_H~7F_H at 8bit access mode and 0_H~3F_H at 16bit access mode.

. 8BIT access



. 16 BIT access



In the Black & white mode, the MSBs of 3 bit and 2 bit corresponding with RGB are used to display data. And so, 128x82 dot gray display or 384 x 82 B/W mode display is possible.

Display RAM is accessed with X address and Y address from CPU by 8 bit or 16 bit unit.

X address and Y address can be increased automatically by setting status of control register.

The address is increased per every read and write of display RAM by CPU. (Please see detail description at command function.)

X direction is selected by X address and Y direction is selected by Y address. Please do not set the address on non-effective area and it is forbidden to set address on outside area in each case.

384bit display data of Y direction are read out to display latch at rising edge of CL signal per 1 line cycle and this data comes out from display latch at falling edge of CL signal.

Display start line address register is preset to line counter at "H" state of FLM signal which changes per one frame cycle and the address is counted up with synchronized CL input.

Display line address counter is synchronized by timing signals of LCD driver, and it operates independently with X, Y address counters.

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(7) Window address assign of display RAM

This IC can be accessed to display RAM by window area designation in addition to access to display RAM designated by X and Y address.

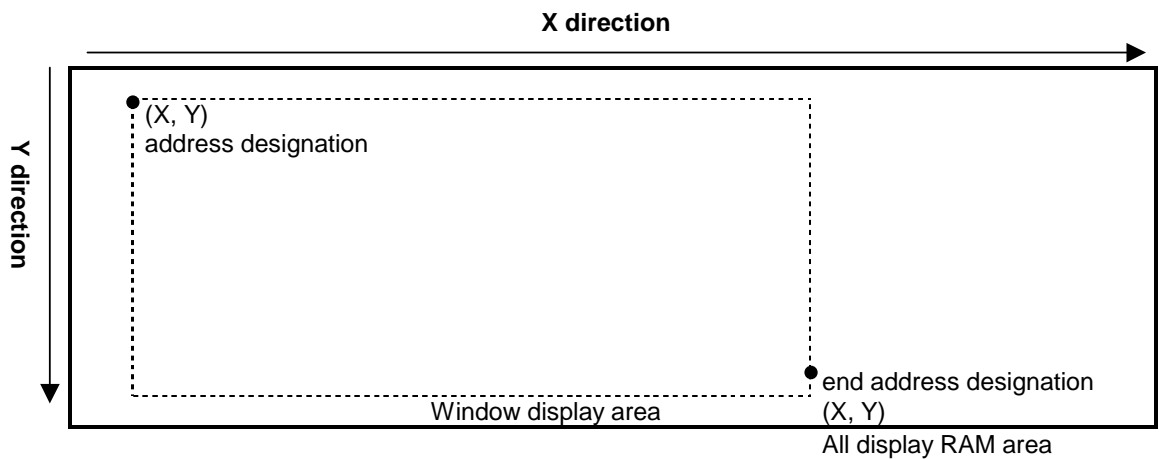
Through address space of all display address, specific area of RAM can be accessed by designated two points.

The start point of two point addresses is assigned by normal X address and Y address register and the end point of them is done by X end address and Y end address register value. Designated inner addresses depend on WLS bit.

Read modified write action can be taken by AIM="1".

In case of using window area accessing mode, you must set start point X address, Y address in sequence and end point X address, Y address in sequence after executing Win command (WIN="1", auto increase mode AXI="1", AYI="1") and then access to Display RAM.

And set start point and end point not to be designated to access the outside of available address area. Address set value should be taken to set $AX \leq EX$ (end point of X address) and $AY \leq EY$ (end point of Y address).



(8) display RAM data and LCD

Display RAM data related with one dot of LCD is dependent on REV register. Normal display and reverse display by REV register are set up as follows.

TABLE

REV	Display	RAM data
L	normal	0
		1
H	reverse	0
		1

(9) Segment display output order/reverse set up

The order of display outputs, $SEGA_0$, $SEGB_0$, $SEGC_0$ to $SEGA_{127}$, $SEGB_{127}$, and can be reversed by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

(10) Relation between Display RAM and address

. RAM address and bitmap

COLOR / 16 BIT MODE

REF	SWAP	X address / bit / segment assign																	
0	0	X=00 _H							X=3F _H									
1	1	X=3F _H							X=00 _H									
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅		
		palette A			palette B			palette C			palette A			palette B			palette C		
		SEGA ₀			SEGB ₀			SEGC ₀			SEGA ₁			SEGB ₁			SEGC ₁		
			
		palette A			palette B			palette C			palette A			palette B			palette C		
		SEGA ₁₂₆			SEGB ₁₂₆			SEGC ₁₂₆			SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇		

REF	SWAP	X address / bit / segment assign																	
0	1	X=00 _H							X=3F _H									
1	0	X=3F _H							X=00 _H									
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
		palette C			palette B			palette A			palette C			palette B			palette A		
		SEGA ₀			SEGB ₀			SEGC ₀			SEGA ₁			SEGB ₁			SEGC ₁		
			
		palette C			palette B			palette A			palette C			palette B			palette A		
		SEGA ₁₂₆			SEGB ₁₂₆			SEGC ₁₂₆			SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇		

COLOR / 8 BIT MODE

REF	SWAP	X address / bit / segment assign																	
0	0	X=00 _H				X=01 _H				X=7E _H				X=7F _H				
1	1	X=7F _H				X=7E _H				X=01 _H				X=00 _H				
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇		
		palette A		palette B		palette C		palette A		palette B		palette C		palette A		palette B		palette C	
		SEGA ₀		SEGB ₀		SEGC ₀		SEGA ₁		SEGB ₁		SEGC ₁		SEGA ₁₂₆		SEGB ₁₂₆		SEGC ₁₂₆	
		
		palette A		palette B		palette C		palette A		palette B		palette C		palette A		palette B		palette C	
		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇	

REF	SWAP	X address / bit / segment assign																	
0	1	X=00 _H				X=01 _H				X=7E _H				X=7F _H				
1	0	X=7F _H				X=7E _H				X=01 _H				X=00 _H				
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
		palette C		palette B		palette A		palette C		palette B		palette A		palette C		palette B		palette A	
		SEGA ₀		SEGB ₀		SEGC ₀		SEGA ₁		SEGB ₁		SEGC ₁		SEGA ₁₂₆		SEGB ₁₂₆		SEGC ₁₂₆	
		
		palette C		palette B		palette A		palette C		palette B		palette A		palette C		palette B		palette A	
		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇		SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇	

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BLACK & WHITE / 16 BIT MODE

REF	SWAP	X address / bit / segment assign																																																
0	0	X=00 _H								X=3F _H																																							
1	1	X=3F _H								X=00 _H																																							
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅																
		SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

REF	SWAP	X address / bit / segment assign																																																
0	1	X=00 _H								X=3F _H																																							
1	0	X=3F _H								X=00 _H																																							
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																
		SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

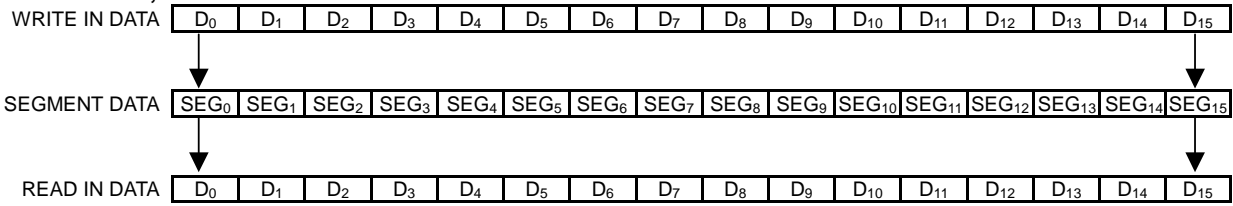
BLACK & WHITE / 8 BIT MODE

REF	SWAP	X address / bit / segment assign																																																
0	0	X=00 _H				X=01 _H				X=7E _H				X=7F _H																																			
1	1	X=7F _H				X=7E _H				X=01 _H				X=00 _H																																			
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇																
		SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

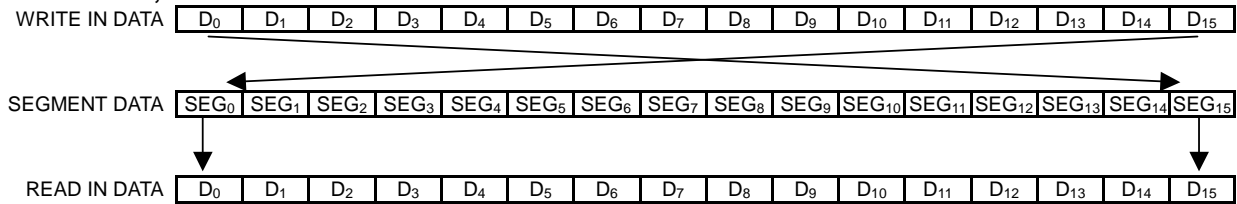
REF	SWAP	X address / bit / segment assign																																																
0	1	X=00 _H				X=01 _H				X=7E _H				X=7F _H																																			
1	0	X=7F _H				X=7E _H				X=01 _H				X=00 _H																																			
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀																
		SEGA ₀				SEGB ₀				SEGC ₀				SEGA ₁				SEGB ₁				SEGC ₁				SEGA ₁₂₆				SEGB ₁₂₆				SEGC ₁₂₆				SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

. WRITE IN / READ IN BITMAP (16 BIT MODE)

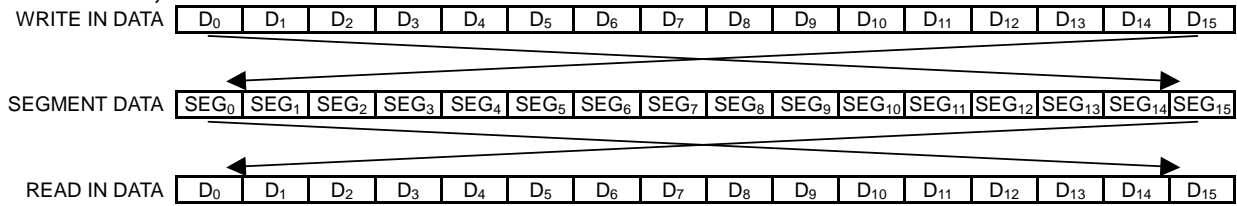
REF=0, SWAP=0



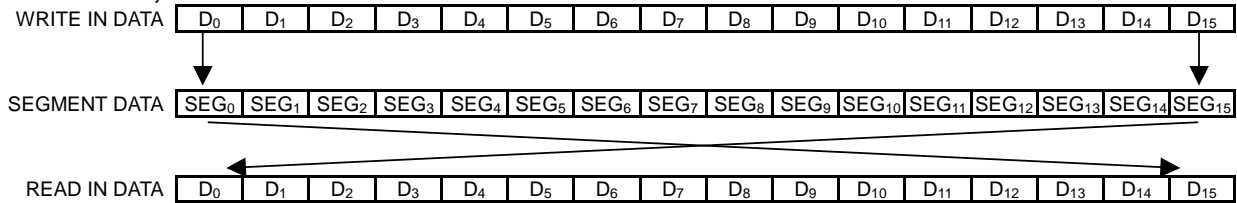
REF=0, SWAP=1



REF=1, SWAP=0



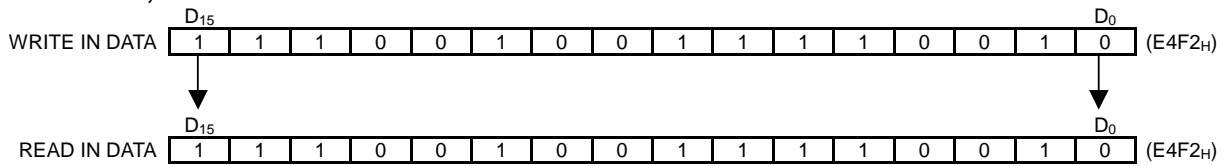
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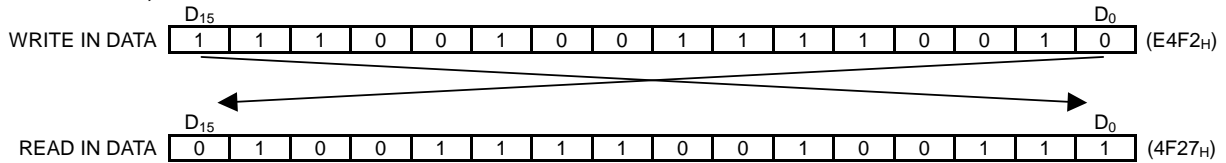
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. READ OUT AFTER WROTE IN DATA (16 BIT MODE)

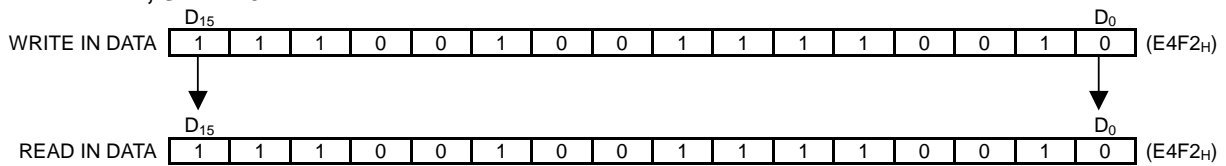
REF=0, SWAP=0



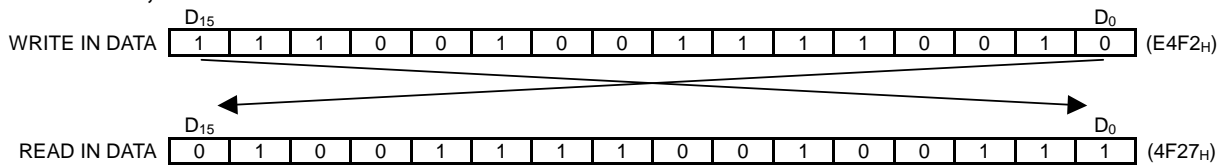
REF=0, SWAP=1



REF=1, SWAP=0

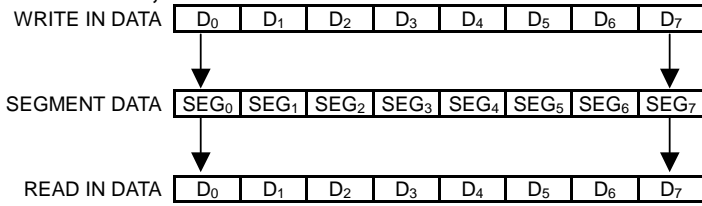


REF=1, SWAP=1

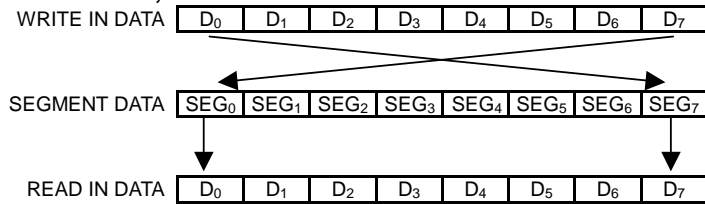


. WRITE IN / READ IN BITMAP (8 BIT MODE)

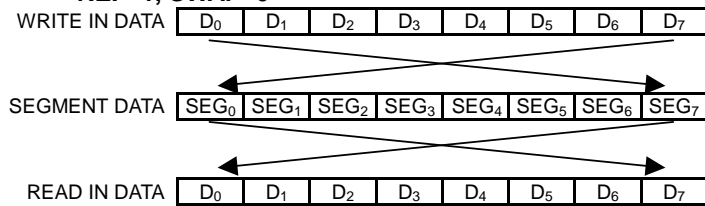
REF=0, SWAP=0



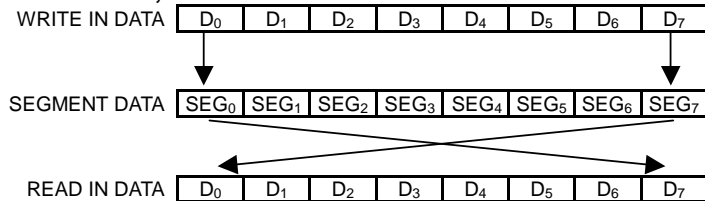
REF=0, SWAP=1



REF=1, SWAP=0



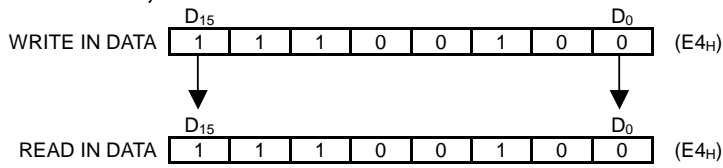
REF=1, SWAP=1



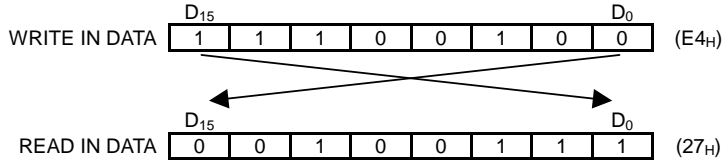
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. READ OUT AFTER WROTE IN DATA (8 BIT MODE)

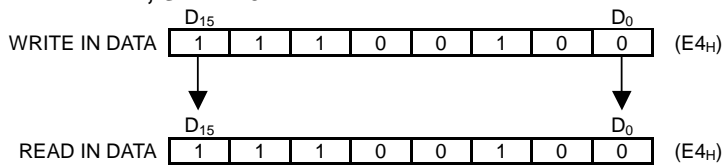
REF=0, SWAP=0



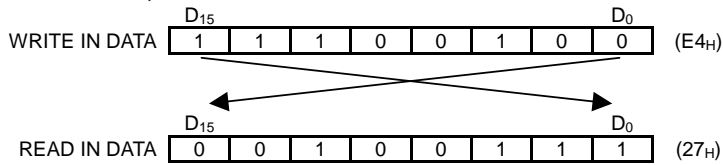
REF=0, SWAP=1



REF=1, SWAP=0



REF=1, SWAP=1



. DUMMY SEGMENT REGISTER ADDRESS AND BITMAP COLOR / 16 BIT MODE

REF	SWAP	X address / bit segment assign																							
0	0	X=00 _H							X=01 _H																
1	1	X=01 _H							X=00 _H																
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅								
		Palette A			Palette B			Palette C			Palette A			Palette B			Palette C								
		SEGSA ₀			SEGSA ₁			SEGSA ₂			SEGSA ₃			SEGSB ₀			SEGSB ₁			SEGSB ₂			SEGSB ₃		

REF	SWAP	X address / bit segment assign																							
0	1	X=00 _H							X=01 _H																
1	0	X=01 _H							X=00 _H																
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀								
		Palette C			Palette B			Palette A			Palette C			Palette B			Palette A								
		SEGSA ₀			SEGSA ₁			SEGSA ₂			SEGSA ₃			SEGSB ₀			SEGSB ₁			SEGSB ₂			SEGSB ₃		

COLOR / 8 BIT MODE

REF	SWAP	X address / bit segment assign															
0	0	X=00 _H		X=01 _H			X=02 _H		X=03 _H								
1	1	X=03 _H		X=02 _H			X=01 _H		X=00 _H								
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇								
		Palette A		Palette B		Palette C		Palette A		Palette B		Palette C					
		SEGSA ₀		SEGSA ₁		SEGSA ₂		SEGSA ₃		SEGSB ₀		SEGSB ₁		SEGSB ₂		SEGSB ₃	

REF	SWAP	X address / bit segment assign															
0	1	X=00 _H		X=01 _H			X=02 _H		X=03 _H								
1	0	X=03 _H		X=02 _H			X=01 _H		X=00 _H								
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀								
		Palette C		Palette B		Palette A		Palette C		Palette B		Palette A					
		SEGSA ₀		SEGSA ₁		SEGSA ₂		SEGSA ₃		SEGSB ₀		SEGSB ₁		SEGSB ₂		SEGSB ₃	

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. BLACK 7 WHITE / 16 BIT MODE

REF	SWAP	X address / bit segment assign															
0	0	X=00 _H								X=01 _H							
1	1	X=01 _H								X=00 _H							
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			SEGS _{C1}

REF	SWAP	X address / bit segment assign															
0	1	X=00 _H								X=01 _H							
1	0	X=01 _H								X=00 _H							
		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		SEGS _{A0}						SEGS _{C0}		SEGS _{A1}				SEGS _{B1}		SEGS _{C1}	

. BLACK & WHITE / 8 BIT MODE

REF	SWAP	X address / bit segment assign															
0	0	X=00 _H				X=01 _H				X=02 _H				X=03 _H			
1	1	X=03 _H				X=02 _H				X=01 _H				X=00 _H			
		D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			SEGS _{C1}

REF	SWAP	X address / bit segment assign															
0	1	X=00 _H				X=01 _H				X=02 _H				X=03 _H			
1	0	X=03 _H				X=02 _H				X=01 _H				X=00 _H			
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			SEGS _{C1}

(11) display data structure and gradation control

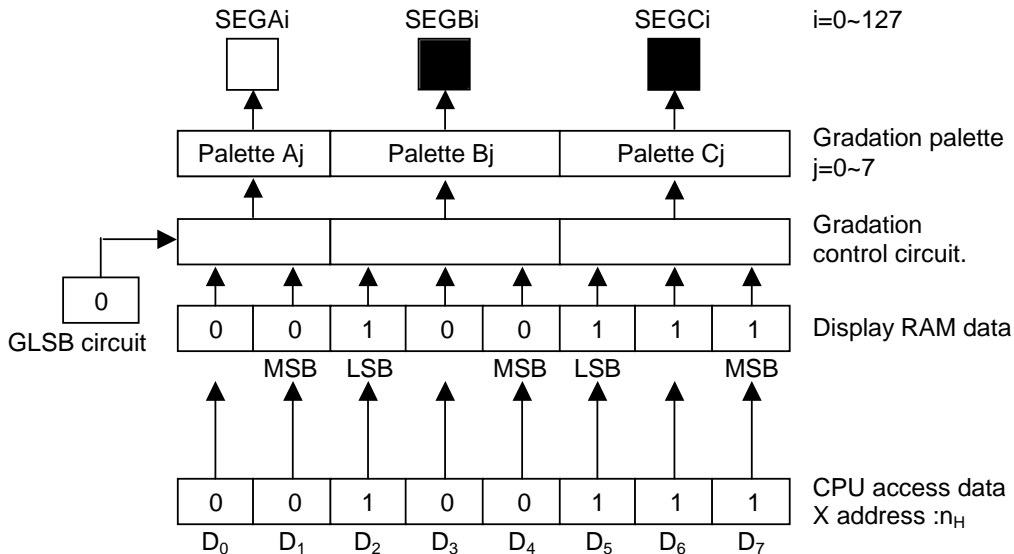
For the purpose of gradation control, information per pixel requires multiple bits. This IC has 3 bit or 2 bit data per output to achieve the gradation display.

This IC is connected to an STN color LCD panel by three segment port units and one pixel consists of three outputs of segment driver, and so 256 color (3 bits x 3 bits x 2 bits) display on 128 x 82 pixels is realized.

Since one pixel data can be processed by one time access to memory, the data can be rewritten fast and naturally.

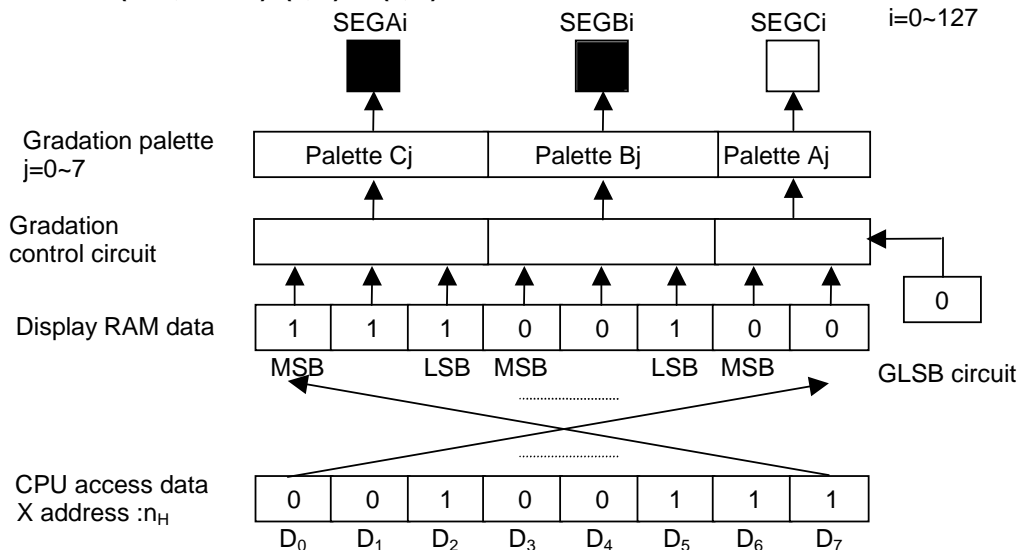
The weight of each data bit is dependent on the status of SWAP register bit and REF register when data is written to the display RAM.

. ACCESS when (REF, SWAP)=(0, 0) or (1, 1)



notice) internal access X address : $n_H \sim 7F_H$ (access when REF="0")
 : $7F_H \sim n_H$ (access when REF="1")

. ACCESS when (REF, SWAP)=(0, 1) or (1, 0)

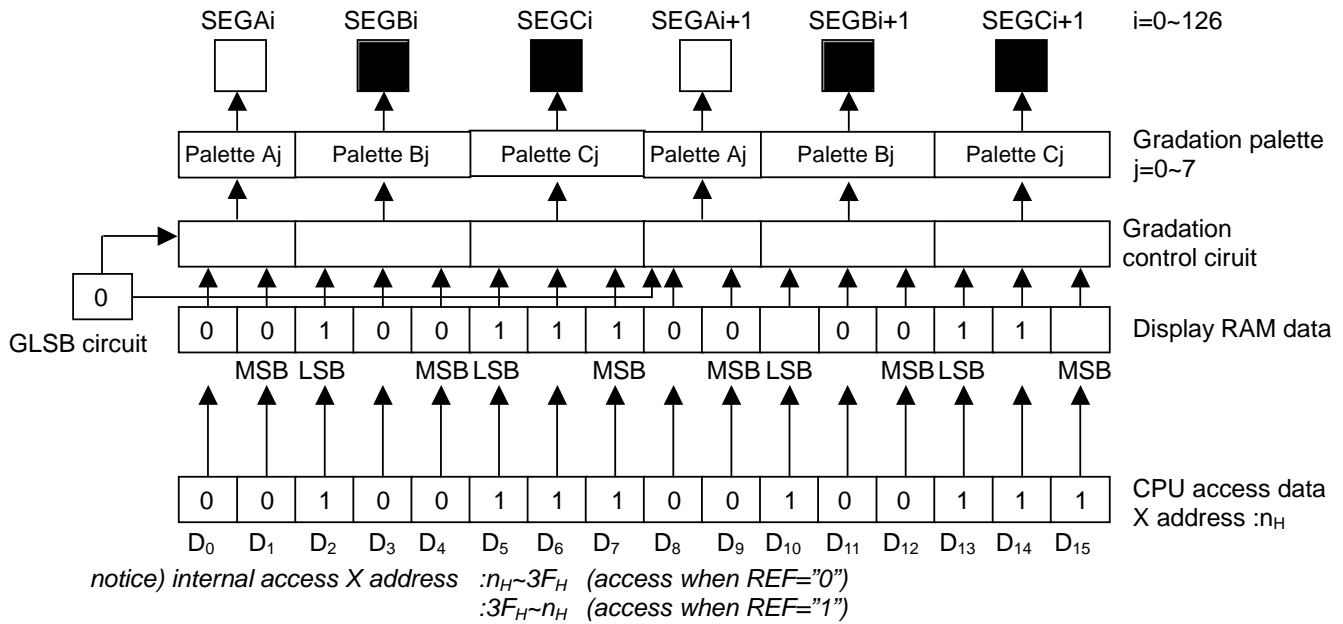


notice) internal access X address : $n_H \sim 7F_H$ (access when REF="0")
 : $7F_H \sim n_H$ (access when REF="1")

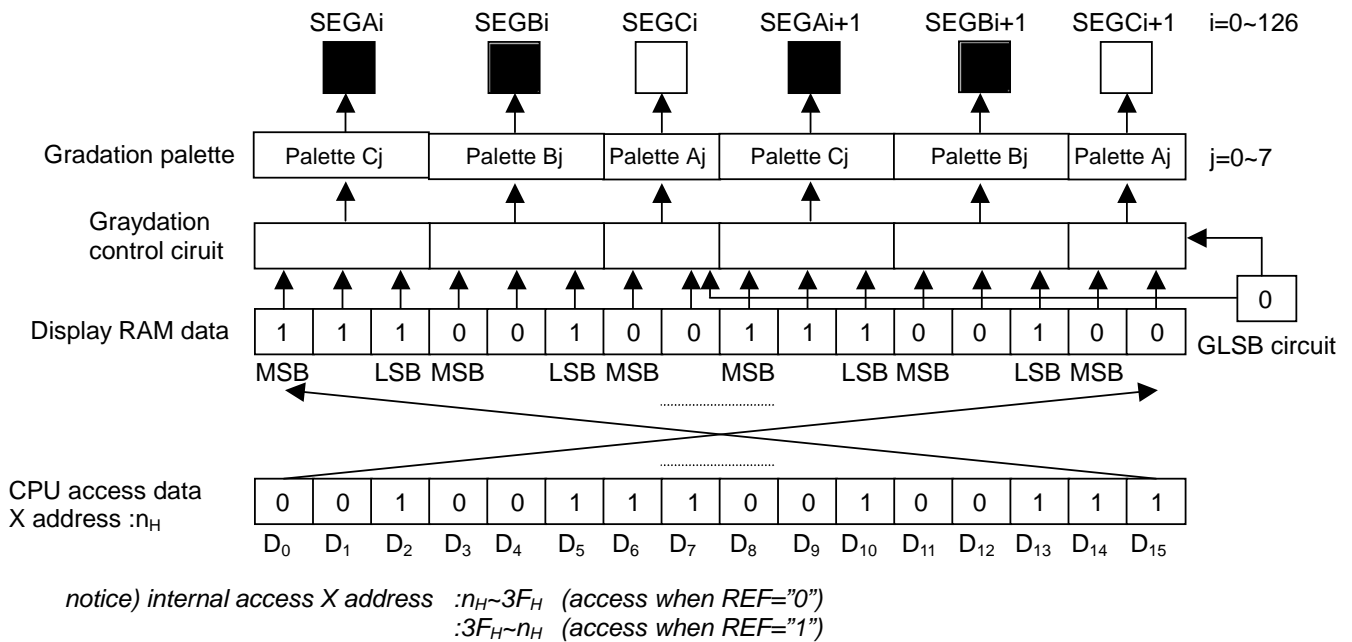
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When display RAM is accessed by 16 bit data width, the weight of each data bit is dependent on the status of SWAP register and REF register, the same method as 8 bit access

. ACCESS when (REF, SWAP)=(0, 0) or (1, 1)



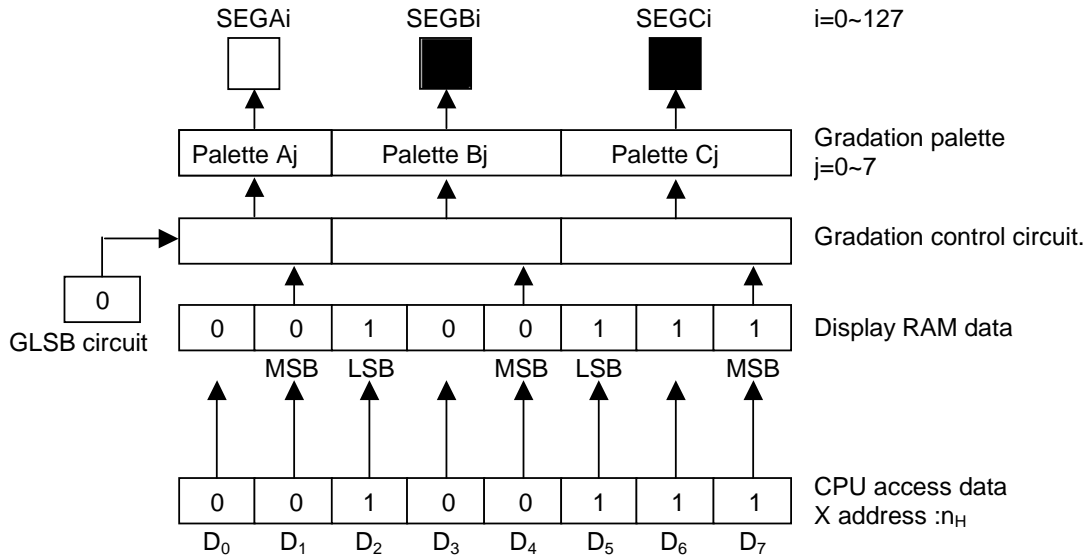
. ACCESS when (REF, SWAP)=(0, 1) or (1, 0)



- DISPLAY RAM BITMAP AT BLACK & WHITE MODE (MON="1")
The MSBs of display RAM data (3 bit, 2 bit) is used as display data at black and white mode.

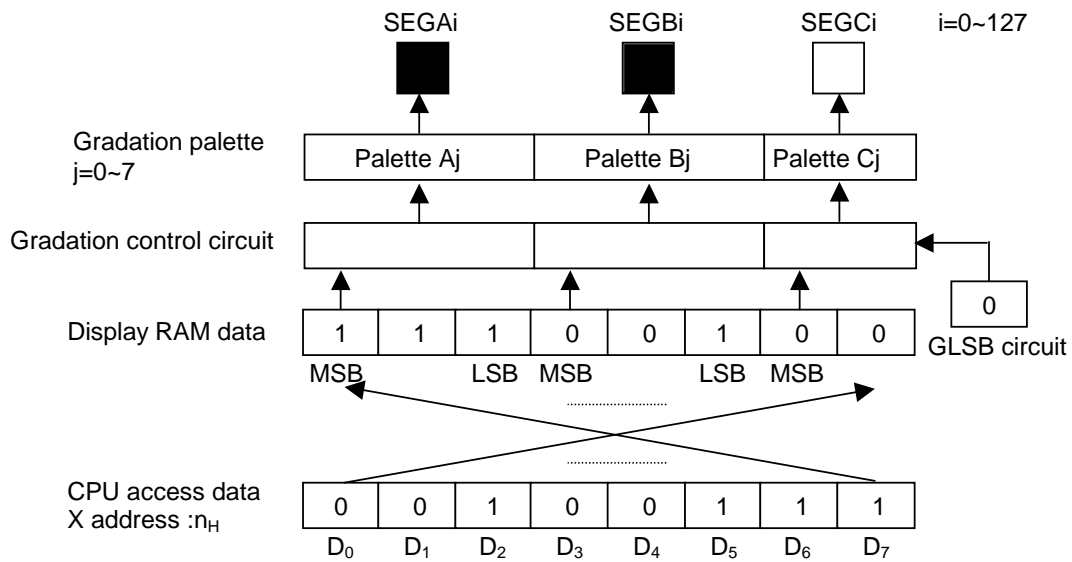
example) 8 bit width access (the same method as 16 bit width access)

- ACCESS when (REF, SWAP)=(0, 0) or (1, 1)



notice) internal access X address $:n_H$ (access when REF="0")
 $:7Fn_H \sim n_H$ (access when REF="1")

- ACCESS when (REF, SWAP)=(0, 1) or (1, 0)



notice) internal access X address $:n_H$ (access when REF="0")
 $:7Fn_H \sim n_H$ (access when REF="1")

gradation level table (MON="1", Black & white mode)

(MSB)RAM data (LSB)			Gradation level
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

RAM data	GLSB	Gradation level
0	0	*
0	1	*
1	0	*
1	1	*

*: Don't Care

(12) GRADATION LSB CONTROL

At 256 colors input mode, this IC provides segment driver output for 8-gradation display using successive 3 bits of data and that for 4-gradation display using successive 2 bits of data.

The segment driver output for the 4-gradation display uses 2 bits written to the corresponding RAM area and 1 bit supplemented by the gradation LSB circuit, and then selects 4 gradations from 8-gradations.

At fixed gradation mode, the segment driver output for the 4-gradation display result in a gradation level of 0 regardless of gradation LSB register, when 2 bits of data on the display RAM are "00". When 2 bits of data on the display RAM is "11", a gradation level of 7/7 is selected regardless of gradation LSB register. The other gradation levels are selected depending on 2 bits of data on the display RAM and the gradation LSB register.

One bit of data is supplemented by setting the gradation LSB register (GLSB).

For this register, the bit information specified for only one time setting is used as the LSB of the RAM for all the 4-gradation segment drivers.

Gradation LSB = "0": Set 0 as the LSB of the RAM for 4-gradation segment drivers.

Gradation LSB = "1": Set 1 as the LSB of the RAM for 4-gradation segment drivers.

(13) GRADATION PALETTE

This IC has two gradation display modes, the fixed gradation display mode and the variable gradation display mode.

Select mode by setting the gradation display mode register (PWM command) to the purpose.

PWM="0" : variable gradation mode among 32-level gradations.

PWM="1" : fixed 8 gradation mode

To select the best gradation level suited to LCD panel at variable gradation display mode, use the gradation palette register among 32-level gradation palettes. Segment driver outputs are set by selected 8-level gradation palette.

The gradation palette register provides three registers (palette Aj, Bj, and Cj : j=0~7) for the segment driver outputs, SEG Ai(0~127), SEG Bi(0~127), and SEG Ci(0~127) . Each register consists of a 5-bit register, selecting 8 gradations from the 32 gradation pattern.

Segment driver selects 4 gradations among 8 gradation by 2 bits wrote-in RAM and 1bit calibrated by GLSB.

GRADATION PALETTE INITIAL VALUE

(palette Aj, palette Bj, palette Cj (j=0~7))

(MSB)RAM data (LSB)	Register name	Initial value
0 0 0	Gradation palette 0	0 0 0 0
0 0 1	Gradation palette 1	0 0 1 0 1
0 1 0	Gradation palette 2	0 1 0 1 0
0 1 1	Gradation palette 3	0 1 1 1 0
1 0 0	Gradation palette 4	1 0 0 0 1
1 0 1	Gradation palette 5	1 0 1 0 1
1 1 0	Gradation palette 6	1 1 0 1 0
1 1 1	Gradation palette 7	1 1 1 1 1

GRADATION PALETTE TABLE (PWM="0", variable mode)

(palette Aj, palette Bj, palette Cj (j=0~7))

Palette	Gradation	remark	Palette	gradation	remark
0 0 0 0 0	0	Palette 0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 4 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 1 initial value	1 0 1 0 1	21/31	Palette 5 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Palette 2 initial value	1 1 0 1 0	26/31	Palette 6 initial value
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Palette 3 initial value	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Palette 7 initial value

GRADATION PALETTE TABLE (PWM="1", fixed mode)

(MSB)RAM data(LSB)	gradation	RAM data	GLSB	gradation
0 0 0	0	0	0	0
0 0 1	1/7	0	1	
0 1 0	2/7	0	1	2/7
0 1 1	3/7	0	0	
1 0 0	4/7	0	1	3/7
1 0 1	5/7	1	0	
1 1 0	6/7	1	0	5/7
1 1 1	7/7	1	1	
				7/7

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(14) DISPLAY TIMMING GENERATOR

The display-timing generator makes a timing clock and timing pulses (CL, FLM, FR and CLK) for internal operation by inputting the original oscillating clock CK or by the oscillating circuit.

By setting up Master / Slave mode (M/S), the state of timing pulse pins and the timing generator changes.

Display timing pulse pins and generator status

M/S port	mode	CL port	FR port	FLM port	CLK port	Timing generator status
L	Slave	Input	Input	Input	Input	CL, FLM, FR signal generator stop
H	Master	Output	Output	Output	Output	Operating status

(15) SIGNAL GENERATION OF DISPLAY LINE COUNTER, DISPLAY DATA LATCH CIRCUIT.

The latch signal from line counter clock to display data latch circuit is generated from display clock (CL). Synchronized with the display clock, the line addresses of Display RAM are generated and 384-bit display data are latched to display-data latching circuit and then output to the LCD drive circuit (SEG output port).

Read-out of the display data to the LCD drive circuit is completely independent of MPU side and so MPU can access it with no relationship with the read-out operation of the display data.

(16) GENERATION OF THE ALTERNATED SIGNAL(FR), SYNCHRONOUS SIGNAL(FLM).

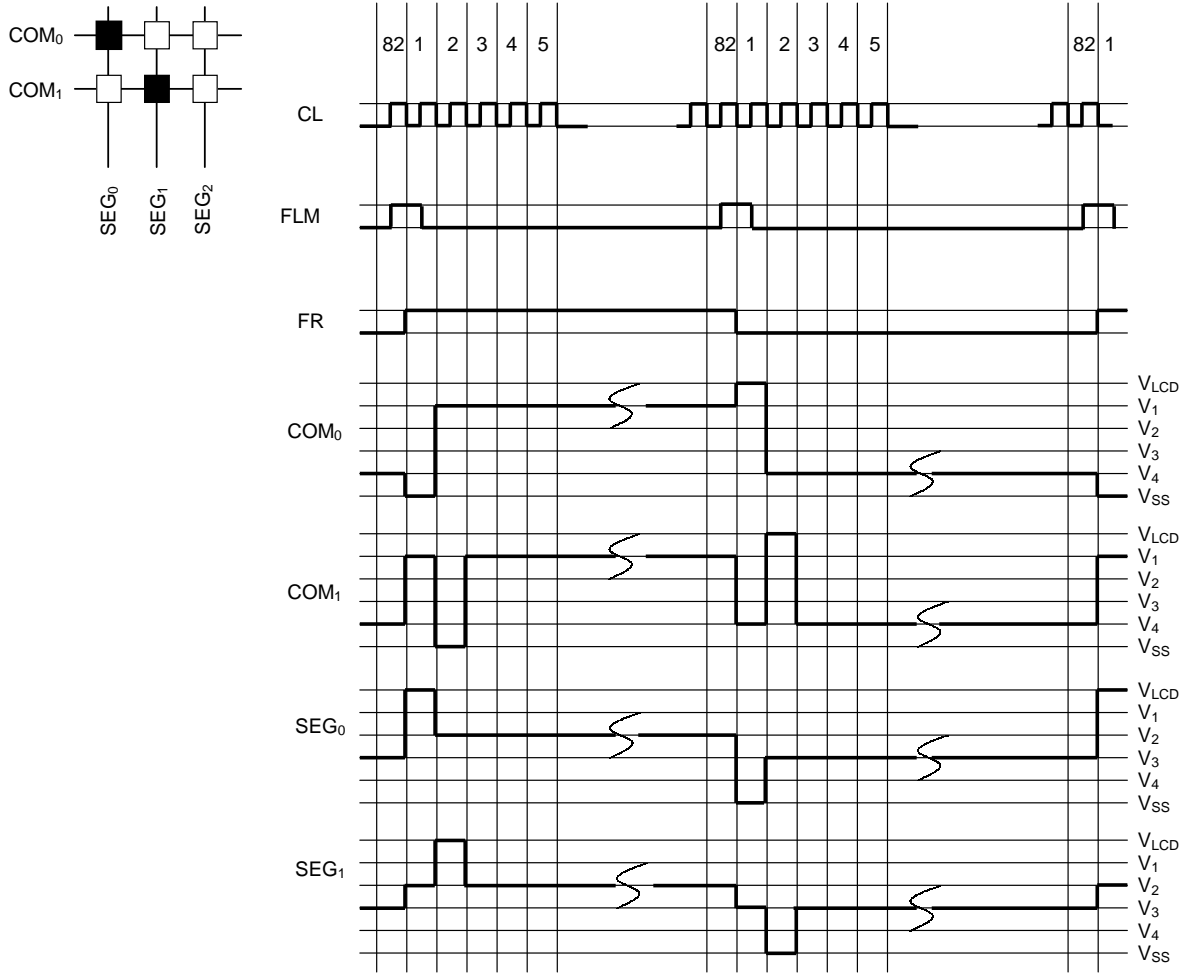
The alternated signal (FR) and synchronous signal (FLM) are generated from the display clock (CL). The FLM generates alternated drive waveform to the LCD drive circuit per frame at normal state (inverse FR signal level per 1 frame). But by setting up data (n-1) on n-line inversion register and "1" on n-line alternated command (NLIN), n-line inverse waveform can be generated.

When this **HM17CM256** is used in multi-chip application, the signals of CL, FLM, FR and CLK must be sent from master side to slave side.

(17) DISPLAY DATA LATCH CIRCUIT

This circuit latches the display data from display RAM to LCD driver circuit temporarily per every common period. Normal / reverse display, display ON/OFF, and display all on command are done by controlling data in this latch. And no data within display RAM changes.

(18) EXAMPLE OF LCD DRIVING (NORMAL MODE, 1/82 DUTY, BLACK & WHITE DISPLAY MODE)



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(19) LCD DRIVER CIRCUIT

This drive circuit generates four levels of LCD drive voltage. The circuit has 384 segment outputs and 82 common outputs and outputs combined display data and FR signal.

Two of common outputs(COMI₀,COMI₁) are for pictograph marker display only. The common drive circuit that has shift register and outputs common scan signals sequentially.

(20) DUMMY SEGMENT DRIVER CIRCUIT

Segment driver circuit has 6 dummy output (SEGSA₀ ~ SEGSA₃, SEGSB₀ ~ SEGSB₃, SEGSC₀ ~ SEGSC₃) at each edge side. Normally, the segment driver output is generated by memorized RAM data but there are no RAMs but registers for dummy segment driver. There are 8 bit registers correspond to SEGSA₀, SEGSB₀, SEGSC₀ and drive LCD with same level to Y direction. (SEGSA₁ ~ SEGSA₃, SEGSB₁ ~ SEGSB₃, SEGSC₁ ~ SEGSC₃ are the same function.)

SEGSA₀ ~ SEGSA₃ port is used same gradation palette with SEGA₀ ~ SEGA₁₂₇, SEGSB₀ ~ SEGSB₃ with SEGB₀ ~ SEGB₁₂₇ , and SEGSC₀ ~ SEGSC₃ with SEGC₀ ~ SEGC₁₂₇

This circuit is effective at display of boundary or background display. The dummy segment drivers do not depend on LREV polarity but ALLON and REV command for display

There are 4-byte registers for dummy segment driver, SEGSA₀ ~ SEGSA₃, SEGSB₀ ~ SEGSB₃, SEGSC₀ ~ SEGSC₃, if you want to access this register, please use DMY = "1" command.

RS	DMY	68 series	80 series		Function
		R/W	RD	WR	
0	0	1	0	1	Read out display data
0	0	0	1	0	Write in display data
0	1	1	0	1	Read out dummy segment register
0	1	0	1	0	Write in dummy segment register

There are the same rules at read out of dummy segment register as display RAM data read out sequence. After address setting, the data of assigned address is shown directly after the end of the read command, so pay attention that assigned data is available at 2nd timing step. In other words, there needs 1 cycle dummy read after address set and write cycle.

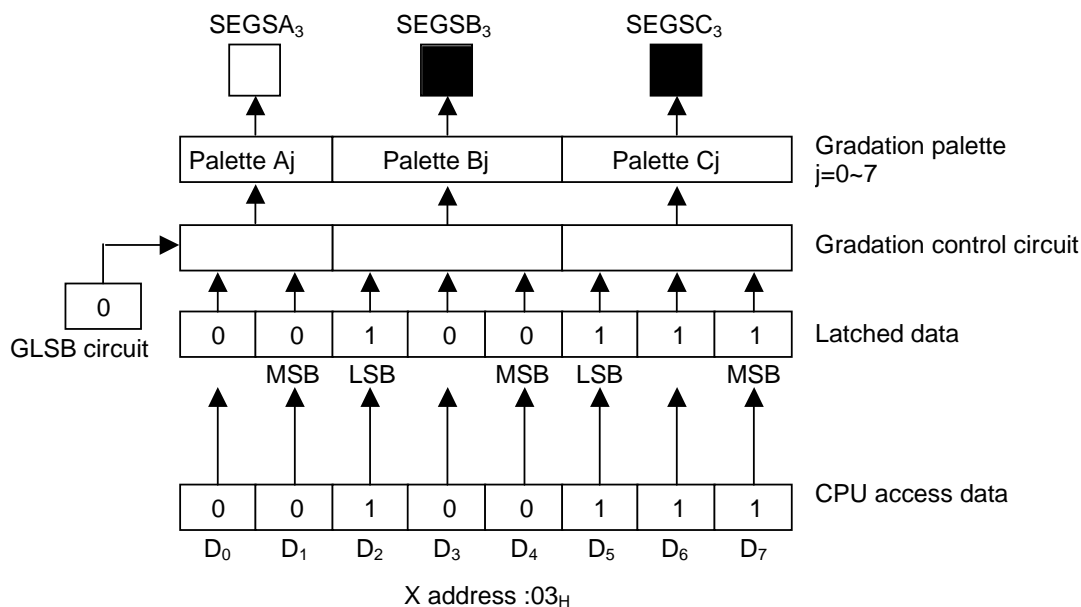
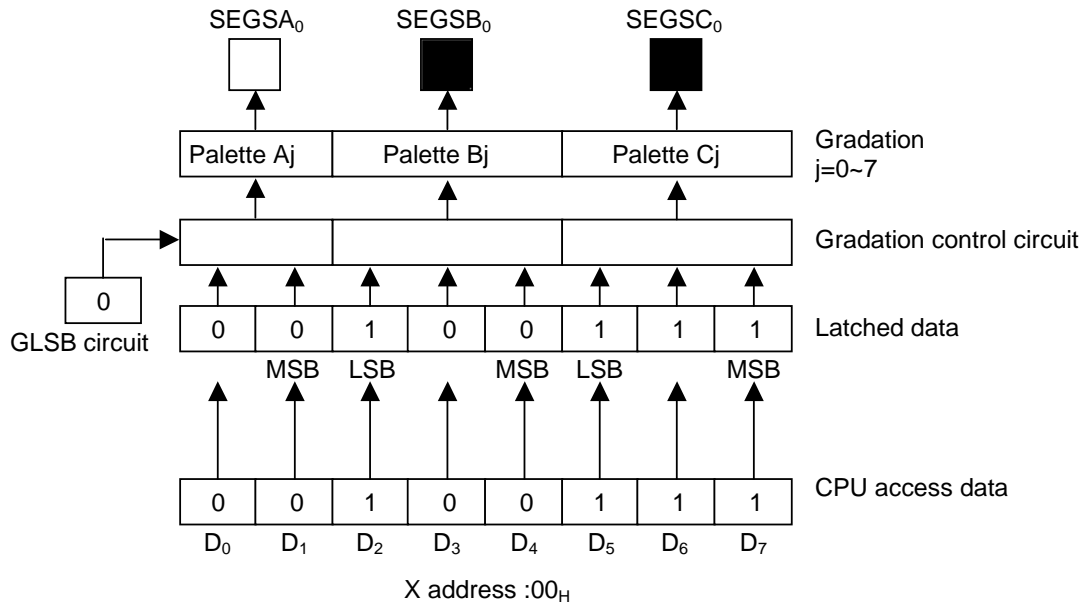
1 cycle dummy read is necessary for after address setting and write cycle.

When access with DMY="1", X address is an effective value at address setting. There are 4-byte and so 00_H, 01_H, 02_H, 03_H are effective at 8-bit mode and 00_H, 01_H are effective at 16-bit mode. The access bears no relation to Y address setting.

When access with DMY="1", it is possible that the data is written into register by increment operation.

notice) more detail information at 「DUMMY SEGMENT REGISTER ADDRESS AND BITMAP」 in 「(10) Relation between Display RAM and address」

ACCESS WITH 8 BIT BUS EXAMPLE : GRAY MODE , ACCESS UNDER (REF, SWAP)=(0, 0)



(21) OSCILLATOR CIRCUIT

HM17CM256 has the CR oscillator. The output of oscillator is used as the timing signal source of display and boosting clock to the booster. This is valid only in the master operation mode.

When in the master operation mode and if external clock is used, feed the clock to OSC₁ pin or connect resistor between OSC₁ and OSC₂.

And feedback resistance with command can set the inner oscillator circuit of HM17CM256.

The frame frequency can be altered by changed oscillator frequency according to feedback resistance length set value. To get optimum frame frequency, please check LCD and then set the frequency of oscillator.

(22) POWER SUPPLY CIRCUIT

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This block generates the voltages necessary for driving LCD panel. The power supply circuit consists of voltage boosting circuit and voltage converting circuit and generates the voltages (V_{LCD} , V_1 , V_2 , V_3 , V_4 .) for LCD driving.

For large panel driving, it's preferable to use external voltage source rather than to use built-in power supply circuit for good image quality.

When using external voltage source, disable the built-in power supply circuit(AMPON, DCON='00'), supply the V_{LCD} , V_1 , V_2 , V_3 , V_4 and V_{OUT} externally and open the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} , V_{REF} , V_{REG} , V_{EE} terminals.

According to power supply circuit control command input, the power supply circuit can be enabled partially. External power supply and partial inner power circuit can be used together. Refer to the next table.

DCON	AMPON	Boosting circuit	Converting circuit	External voltage input	remark
0	0	Disable	disable	V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 , V_4 common	※ 1,3
0	1	Disable	enable	V_{OUT} common	※ 2,3
1	1	Enable	enable	-	-

※1. All the built-in boosting circuit, converting circuit is not used. Open the , C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} , V_{REF} , V_{REG} , V_{EE} terminals, LCD driving voltage should be applied externally.

※2.Only the Boosting circuit is not used. Open the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} , V_{OUT} terminals, The power for converting circuit must be supplied through V_{OUT} terminal and the reference voltage must be supplied by V_{REF} terminal.

※3.The conditions between V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 , and V_4 are $V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.

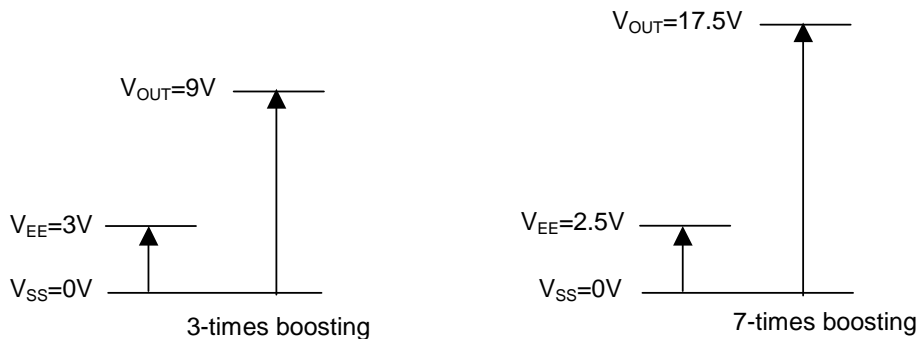
(23) VOLTAGE BOOSTING CIRCUIT

By connecting capacitor CA_1 between C_{1+} and C_{1-} , C_{2+} and C_{2-} , C_{3+} and C_{3-} , C_{4+} and C_{4-} , C_{5+} and C_{5-} , C_{6+} and C_{6-} , V_{OUT} and V_{SS} , n-time boosted voltage of $V_{EE} - V_{SS}$ can be generated through V_{OUT} port. The boosting coefficient can be set by command and 2-times/ 3-times / 4-times/ 5-times/ 6-times/ 7-times boosted voltage is output through V_{OUT} port.

At application, specific boosting coefficient is used, refer to the following description.

- ① At 2-times boosting is designed, connect boosting capacitor CA_1 between C_{1+} and C_{1-} , and open C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} terminals.
- ② At 3-times boosting is designed, connect boosting capacitor CA_1 between C_{1+} and C_{1-} , C_{2+} and C_{2-} , and open C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} terminals.
- ③ At 4-times boosting is designed, connect boosting capacitor CA_1 between C_{1+} and C_{1-} , C_{2+} and C_{2-} , C_{3+} and C_{3-} , and open C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} terminals
- ④ At 5-times/ 6-times/ 7-times boosting are same structures with upper case.

Special care should be taken so that the voltage of V_{OUT} would not exceed 18V MAX. V_{OUT} voltage exceeding 18V can cause malfunction and reliability problem.



(24) ELECTRIC VOLUME

The electric volume is within voltage converting circuit and the brightness of LCD can be controlled by adjusting V_{LCD} level with command.

The LCD driving voltage V_{LCD} is generated by selecting 1 level within 128 step electric volume controlled levels by setting 7 bit electric volume register.

(25) VOLTAGE REGULATOR CIRCUIT

The voltage regulator circuit is within voltage converting circuit and generates regulated voltage using V_{REF} input with magnification by adjusting internal resistor. The generated voltage by voltage regulator is output at V_{REG} terminal. Even though boosted voltage variation, generated regulator voltage is stable because boosting voltage level is higher than the amplified regulator voltage V_{REG} . And so, stable voltage level can be generated even if there is load variation.

V_{REG} is used as input voltage of electric volume circuit to generate LCD driving voltage.

(26) REFERENCE VOLTAGE GENERATION CIRCUIT

The reference voltage generation circuit is within voltage converting circuit.

This circuit generates reference voltage V_{BA} terminal for using at regulator circuit through. The output voltage level from V_{BA} terminal is as following description.

$$V_{BA} = V_{EE} \times 0.9$$

The LCD driving voltages can be made by applying reference voltage to reference voltage input terminal V_{REF} .

(27) LCD DRIVING VOLTAGE GENERATION CIRCUIT

The generation circuit of LCD driving voltage is within voltage converting circuit and generates voltages V_{LCD} , V_1 , V_2 , V_3 , V_4 by resistively dividing V_{LCD} into 4 levels.

The bias ratio of LCD driving voltages can be one of 1/5, 1/6, 1/7, 1/8, 1/9, 1/10.

When using built-in power supply circuit, you should connect voltage stabilization capacitor CA_2 at each of LCD power terminals. There is need for selecting the coefficient of capacitor CA_2 after display the LCD.

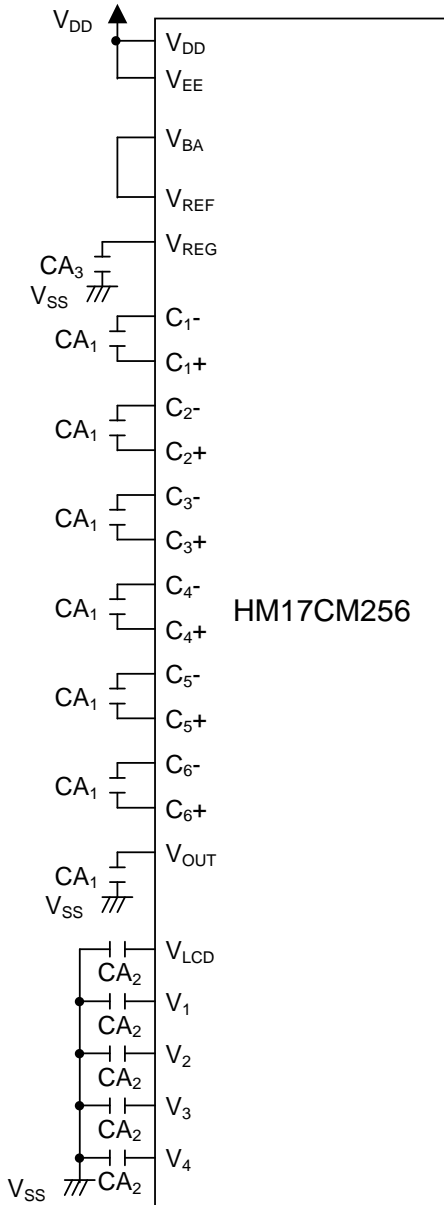
When using external voltage supply, disable the built-in power supply circuit (AMPON, DCON='00'), supply the V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 , V_4 voltages externally and open the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} , V_{EE} , V_{REF} , V_{REG} terminals.

When using external voltage source and parts of built-in voltage converting circuit, the terminals of C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , C_{6+} , C_{6-} should be open because boosting circuit is not activated, you should supply reference voltage through V_{REF} terminal and the voltage for voltage converting circuit at V_{OUT} .

Connecting stabilization capacitor CA_3 at V_{REG} terminal is recommended.

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internal power circuit / internal reference voltage generating circuit are activated case.(7 times boosting)



internal power circuit is not used case



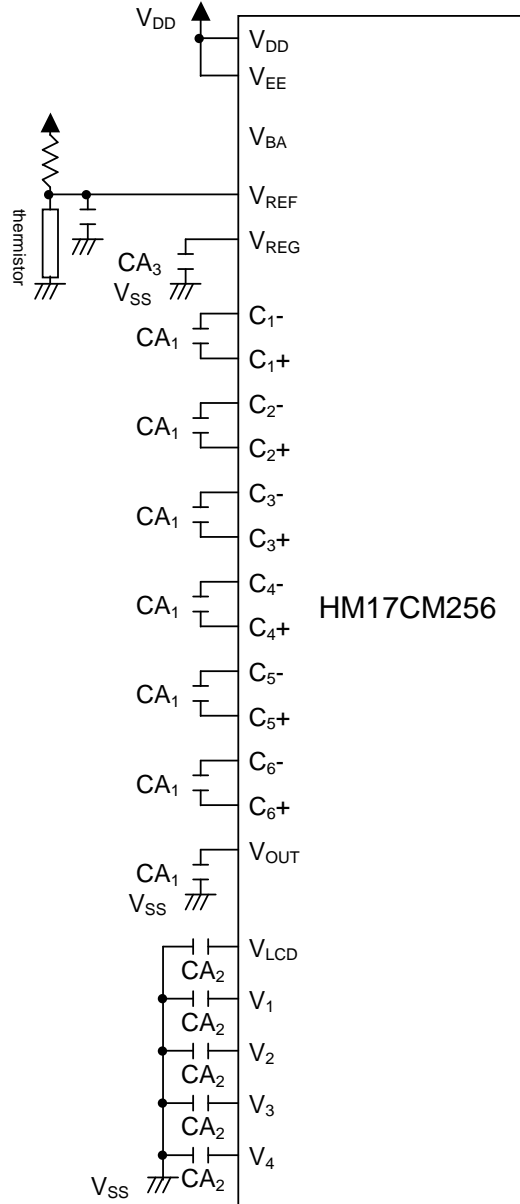
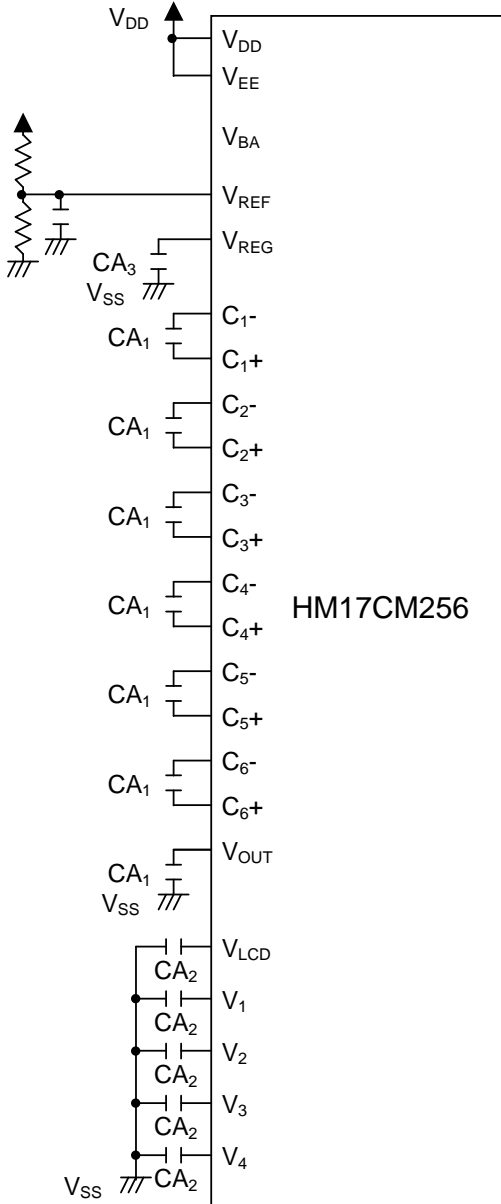
value

CA ₁	1.0 ~ 4.7μF
CA ₂	1.0 ~ 2.2μF
CA ₃	0.1μF

caution) Please use B grade capacitor.

Internal power circuit is used case. Reference voltage input from outside . (7 times boosting)

Internal power circuit is used case. Temperature compensation by external thermistor . (7 times boosting)



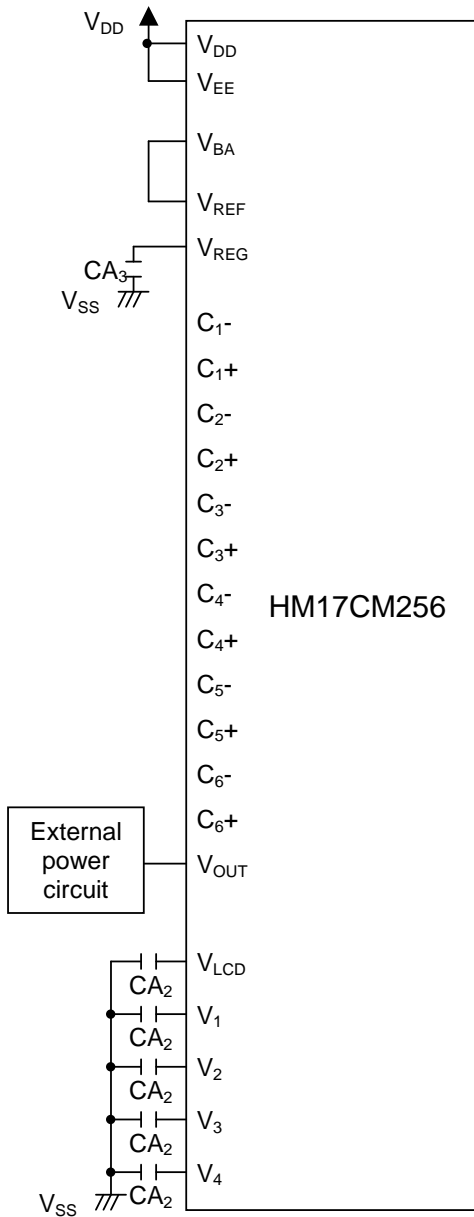
value

CA ₁	1.0 ~ 4.7μF
CA ₂	1.0 ~ 2.2μF
CA ₃	0.1μF

caution) Please use B grade capacitor.

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Internal power circuit is used case. (boosting circuit is not used, V_{OUT} is supplied from outside)



value

CA_1	1.0 ~ 4.7 μ F
CA_2	1.0 ~ 2.2 μ F
CA_3	0.1 μ F

caution) Please use B grade capacitor.

(28) PARTIAL DISPLAY FUNCTION

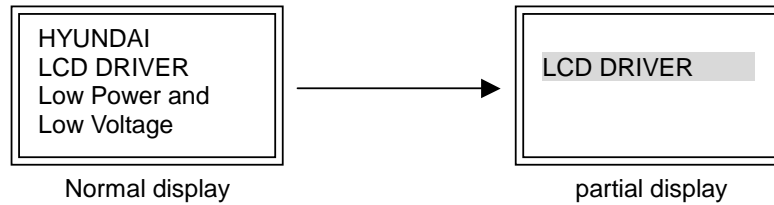
HM17CM256 can realize the partial display at graphic display area on LCD panel.

Partial display is used with lower duty than normal state at driving.

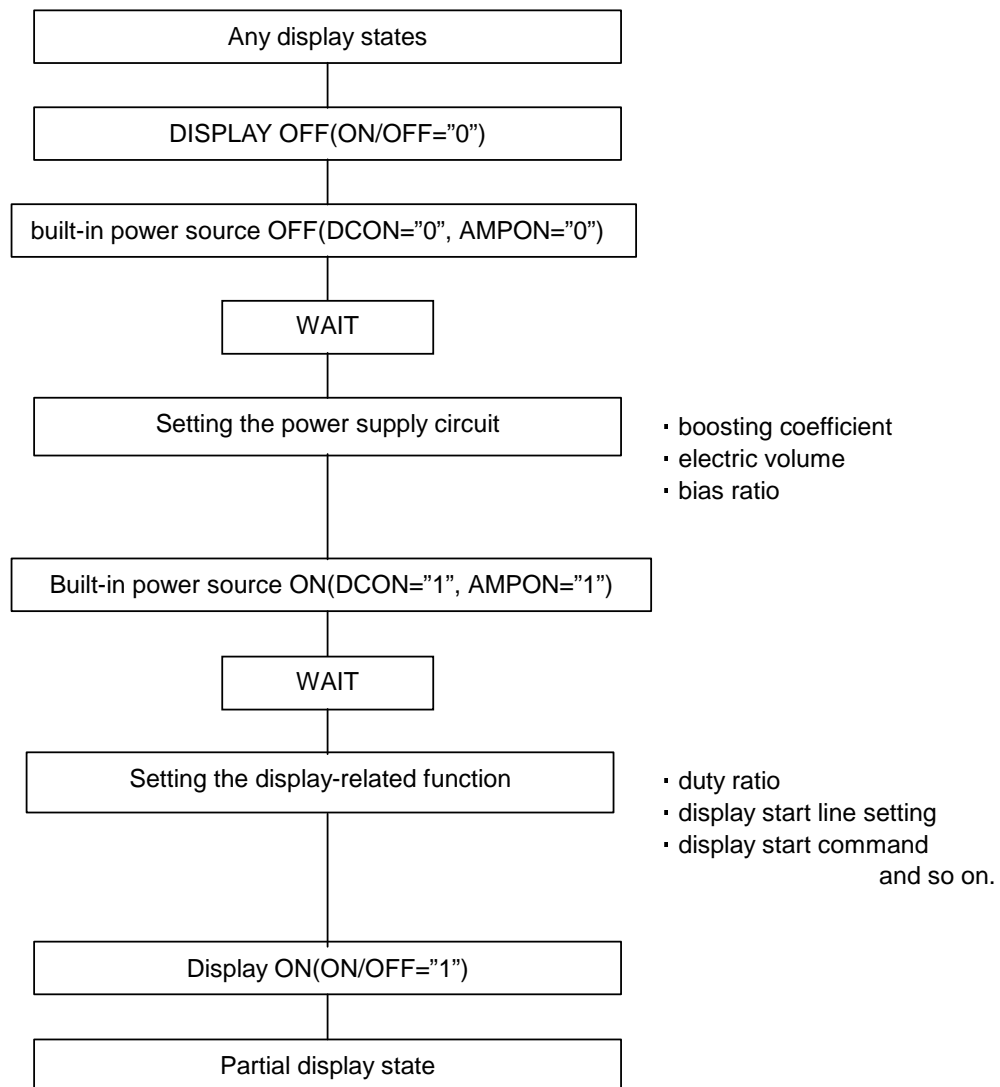
And so, HM17CM256 can drive the LCD panel with lower bias ratio, lower boosting times and lower LCD driving voltages, and that can drive the LCD panel with lower power consumption.

This function is suitable for calendar or clock display at mobile information apparatus.

PARTIAL DISPLAY IMAGE



The next sequence should be followed carefully to realize partial display function.



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When using partial display function, the display duty can be selected among 1/17, 1/26, 1/32, 1/38, 1/47, 1/66, 1/77 by setting the LCD duty set command.

The display states such as LCD driving bias ratio, LCD Driving voltage, electric volume setting value, boosting coefficient should be optimized to the selected LCD and display duty.

(29) DISCHARGE CIRCUIT

The discharge circuit of voltage (V_{LCD} , $V_1 \sim V_4$) stabilization capacitor is built in the HM17CM256.

To discharge the capacitors, set the DIS register to "1" or set the \overline{RES} terminal to "0". When built-in power supply circuit is used, built-in power supply circuit should be disabled before discharging of the capacitor is executed. When external power supply (V_{LCD} , $V_1 \sim V_4$, V_{OUT}) is used, external power supply should be turned off before discharging of the capacitor is executed. Do not turn on the internal power supply and external power supply (V_{LCD} , $V_1 \sim V_4$, V_{OUT}) during discharging is executed.

(30) RESET CIRCUIT

HM17CM256 is initialized as following description when \overline{RES} terminal is set to "L".

INITIAL SETTING CONDITION (default setting)

1. display RAM	:unknown
2. X address	:00 _H set
3. Y address	:00 _H set
4. display start line	:1 line value 0 _H
5. display ON/OFF	:display OFF
6. positive/negative	:positive
7. display duty ratio	:1/82
8. n line inversion	:n inversion disable
9. COM shift direction	:COM ₀ → COM ₇₉ , COM _{I0} , COM _{I1}
10. increment mode	:increment OFF
11. REF mode	:positive
12. data SWAP mode	:OFF
13. electric volume	:(0, 0, 0, 0, 0, 0, 0)
14. power circuit	:OFF
15. display mode:gradation display mode	
16. bias ratio	:1/10 bias
17. gradation palette 0	:(0, 0, 0, 0, 0)
18. gradation palette 1	:(0, 0, 1, 0, 1)
19. gradation palette 2	:(0, 1, 0, 1, 0)
20. gradation palette 3	:(0, 1, 1, 1, 0)
21. gradation palette 4	:(1, 0, 0, 0, 1)
22. gradation palette 5	:(1, 0, 1, 0, 1)
23. gradation palette 6	:(1, 1, 0, 1, 0)
24. gradation palette 7	:(1, 1, 1, 1, 1)
25. gradation mode	:variable mode
26. GLSB	:"0"
27. RAM data length	:8 bit mode
28. discharge register	:"0"

Usually \overline{RES} terminal is connected reset terminal of CPU, so that the chip can be initialized simultaneously with CPU. HM17CM256 should be initialized when the power is on.

(31) SUPPLYING POWER AND ON/OFF SEQUENCE

Special care should be taken to the next notice. Supplying the power at LCD driving voltage terminal when the logic VDD is floating can cause over-current and damage the IC

(31-1) WHEN USING EXTERNAL POWER SUPPLY

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal, and then turn on the LCD driving voltage at the terminals (V_{LCD} , V_1 , V_2 , V_3 , V_4).

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

- power OFF sequence

Execute HALT command or reset the IC to turn off the outputs of LCD driving output port, and then turn off the LCD driving voltage after logic power OFF.

Inserting series resistor of 50 ~100 Ω or fuse at V_{LCD} or V_{OUT} terminal (when only internal voltage converting circuit is used) is recommended to prevent over-current.

This series resistor should be selected carefully because image quality can be dependent on.

(31-2) WHEN USING BUILT-IN POWER SUPPLY CIRCUIT

- power ON sequence

Reset the IC after supplying the logic power at V_{DD} terminal or after supplying power through voltage common port (V_{EE}) of boosting voltage generation and then operate internal power circuit by command.

And when internal voltage converter is used, reset the IC after supplying the logic power at V_{DD} terminal, and then supply power to V_{LCD} terminal.

You should turn on the display after the output level of internal power module is set.

If you do not keep this sequence, LCD can display wrong data.

- power OFF sequence

To make off state of LCD driving output, cut the source to voltage common port (V_{EE}) of boosting voltage generation, the logic power at V_{DD} terminal after reset the IC by HALT command.

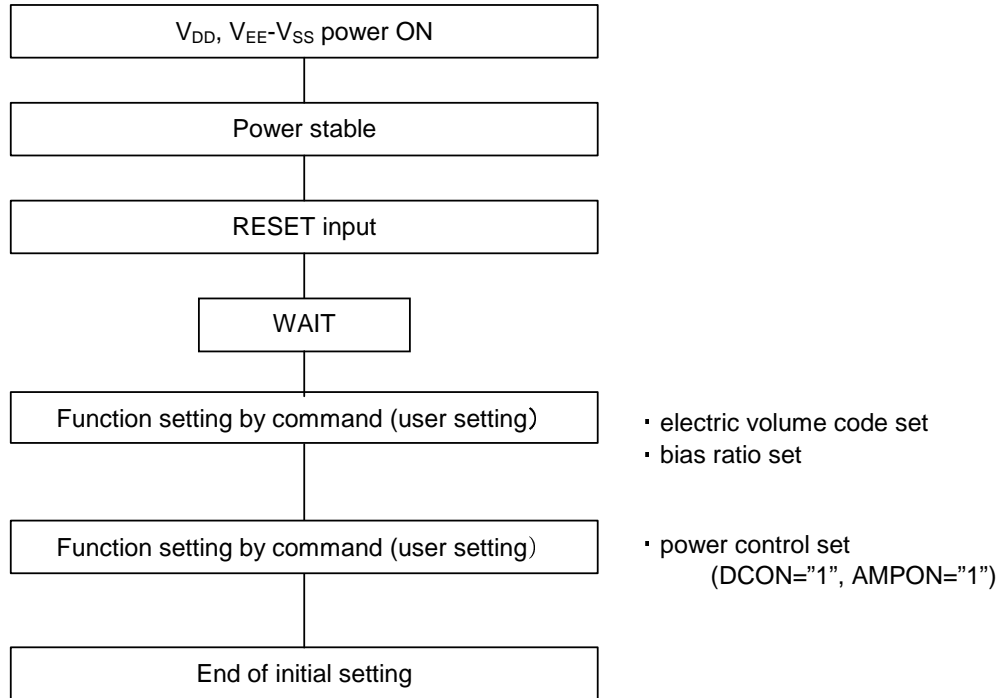
If V_{EE} , and V_{DD} are supplied from different power source, V_{EE} terminal should be turned on/off during V_{DD} terminal voltage maintain voltage level specified in specification sheet.

Specially, when turn off the power, after cut the source to voltage common port (V_{EE}), and then turn off the logic power at V_{DD} terminal after the voltage levels of V_{EE} , V_{OUT} , V_{LCD} , V_1 ~ V_4 become under LCD on voltage(LCD threshold voltage)level.

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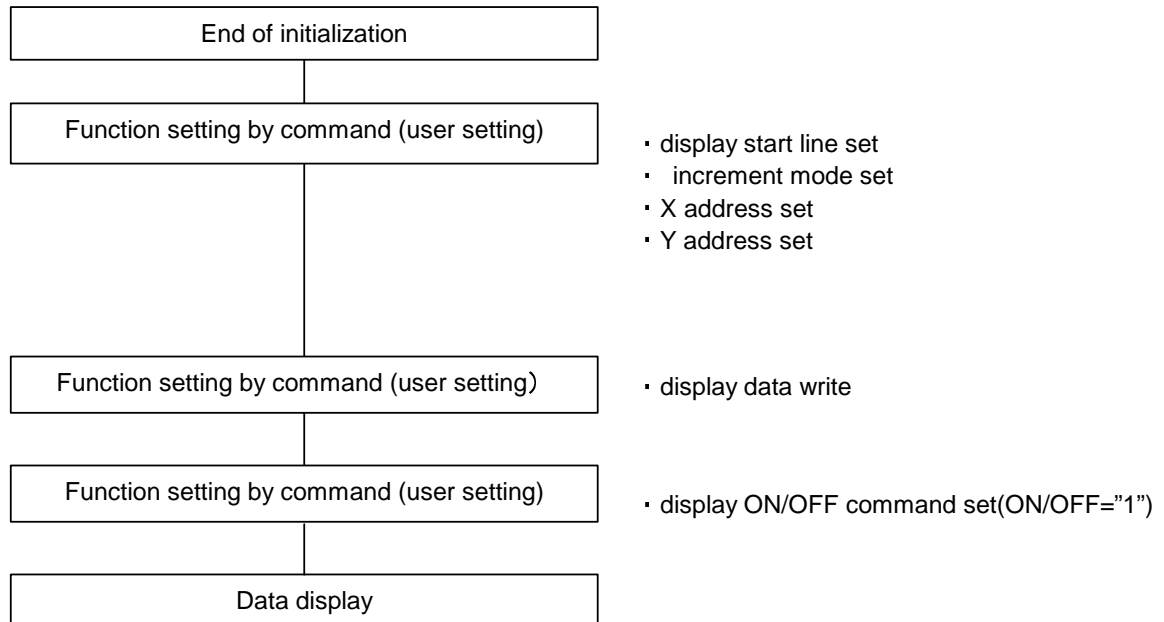
(32) COMMAND SETTING EXAMPLE

(32-1) initial setting

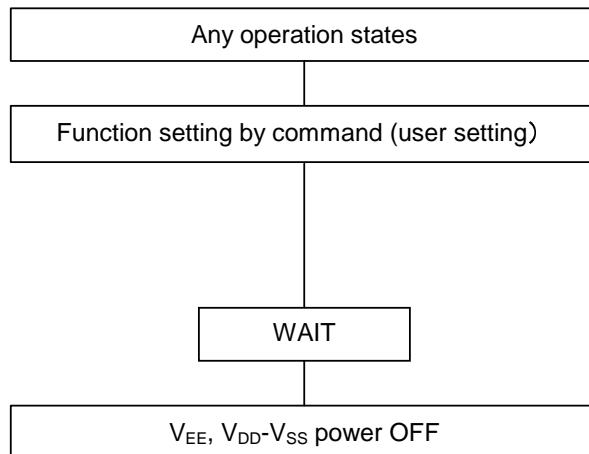


(notice) If the voltage level of VEE and VDD are different, VDD should be inputted first.

(32-2) DATA DISPLAY



(32-3) POWER OFF



- HALT command set or reset operation (all LCD driver output is V_{SS} level)
- Discharge command set (discharge of V_{LCD} , V_1 ~ V_4 capacitor)

Before turning off the power, be sure to execute HALT or RESET command to make LCD driver output OFF state.

And if V_{DD} and V_{EE} have different potential (V_{DD} and V_{EE} are not common), be sure to turn off V_{EE} first during V_{DD} is supplied.

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(33) INSTRUCTION

INSTRUCTION TABLE (1)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	CS	RS	RD	WR	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
display data write in	0	0	1	0	0/1	0/1	0/1	Write Data								Write in to display RAM
display data read out.	0	0	0	1	0/1	0/1	0/1	Read Data								Read out from display RAM
X address (lower) [0 _H]	0	1	1	0	0	0	0	0	0	0	0	AX ₃	AX ₂	AX ₁	AX ₀	Display RAM X direction set
X address (upper) [1 _H]	0	1	1	0	0	0	0	0	0	1	*	AX ₆	AX ₅	AX ₄	AX ₃	Display RAM X direction set
Y address (lower) [2 _H]	0	1	1	0	0	0	0	0	0	1	0	AY ₃	AY ₂	AY ₁	AY ₀	Display RAM Y direction set
Y address (upper) [3 _H]	0	1	1	0	0	0	0	0	0	1	1	*	AY ₆	AY ₅	AY ₄	Display RAM Y direction set
display start line set (lower) [4 _H]	0	1	1	0	0	0	0	0	1	0	0	LA ₃	LA ₂	LA ₁	LA ₀	RAM Y address setting corresponds to scan start line of common driver.
display start line set (upper) [5 _H]	0	1	1	0	0	0	0	0	1	0	1	*	LA ₆	LA ₅	LA ₄	RAM Y address setting corresponds to scan start line of common driver.
N line inversion set (lower) [6 _H]	0	1	1	0	0	0	0	0	1	1	0	N ₃	N ₂	N ₁	N ₀	quantity setting of line inversion
N line inversion set (upper) [7 _H]	0	1	1	0	0	0	0	0	1	1	1	*	N ₆	N ₅	N ₄	quantity setting of line inversion
display control (1) [8 _H]	0	1	1	0	0	0	0	1	0	0	0	SHI FT	MO N	ALL ON	ON/ OFF	SHIFT: common shift direction set, MON: BW/gradation display, ALLON: all on , ON/OFF: display ON/OFF control
display control (2) [9 _H]	0	1	1	0	0	0	0	1	0	0	1	RE V	NL IN	SW AP	RE F	REV: display positive / negative, NLIN: n line inversion ON/OFF, SWAP: display data swap, REF: segment positive / negative
increment control [A _H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: window selection, AIM: increment timing selection, AYI: Y increment, AXI: X increment
power control [B _H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HA LT	DC ON	AC L	AMPON: internal OP Amp. ON, HALT: power save DCON: boosting circuit ON, ACL: reset
LCD duty set [C _H]	0	1	1	0	0	0	0	1	1	0	0	*	DS ₂	DS ₁	DS ₀	LCD driver duty ratio set
boosting coefficient set [D _H]	0	1	1	0	0	0	0	1	1	0	1	*	VU ₂	VU ₁	VU ₀	Boosting times set
bias ratio set [E _H]	0	1	1	0	0	0	0	1	1	1	0	*	B ₂	B ₁	B ₀	LCD drive bias set
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (2)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A ₀ set (lower) [0 _H]	0	1	1	0	0	0	1	0	0	0	0	PA ₀₃	PA ₀₂	PA ₀₁	PA ₀₀	Set value to gradation palette A ₀
Gradation palette A ₀ set (upper) [1 _H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA ₀₄	Set value to gradation palette A ₀
Gradation palette A ₁ set (lower) [2 _H]	0	1	1	0	0	0	1	0	0	1	0	PA ₁₃	PA ₁₂	PA ₁₁	PA ₁₀	Set value to gradation palette A ₁
Gradation palette A ₁ set (upper) [3 _H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA ₁₄	Set value to gradation palette A ₁
Gradation palette A ₂ set (lower) [4 _H]	0	1	1	0	0	0	1	0	1	0	0	PA ₂₃	PA ₂₂	PA ₂₁	PA ₂₀	Set value to gradation palette A ₂
Gradation palette A ₂ set (upper) [5 _H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA ₂₄	Set value to gradation palette A ₂
Gradation palette A ₃ set (lower) [6 _H]	0	1	1	0	0	0	1	0	1	1	0	PA ₃₃	PA ₃₂	PA ₃₁	PA ₃₀	Set value to gradation palette A ₃
Gradation palette A ₃ set (upper) [7 _H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA ₃₄	Set value to gradation palette A ₃
Gradation palette A ₄ set (lower) [8 _H]	0	1	1	0	0	0	1	1	0	0	0	PA ₄₃	PA ₄₂	PA ₄₁	PA ₄₀	Set value to gradation palette A ₄
Gradation palette A ₄ set (upper) [9 _H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA ₄₄	Set value to gradation palette A ₄
Gradation palette A ₅ set (lower) [A _H]	0	1	1	0	0	0	1	1	0	1	0	PA ₅₃	PA ₅₂	PA ₅₁	PA ₅₀	Set value to gradation palette A ₅
Gradation palette A ₅ set (upper) [B _H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA ₅₄	Set value to gradation palette A ₅
Gradation palette A ₆ set (lower) [C _H]	0	1	1	0	0	0	1	1	1	0	0	PA ₆₃	PA ₆₂	PA ₆₁	PA ₆₀	Set value to gradation palette A ₆
Gradation palette A ₆ set (upper) [D _H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA ₆₄	Set value to gradation palette A ₆
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

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INSTRUCTION TABLE (3)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	CS	RS	RD	WR	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A ₇ set (lower) [0 _H]	0	1	1	0	0	1	0	0	0	0	0	PA ₇₃	PA ₇₂	PA ₇₁	PA ₇₀	Set value to gradation palette A ₇
Gradation palette A ₇ set (upper) [1 _H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA ₇₄	Set value to gradation palette A ₇
Gradation palette B ₀ set (lower) [2 _H]	0	1	1	0	0	1	0	0	0	1	0	PB ₀₃	PB ₀₂	PB ₀₁	PB ₀₀	Set value to gradation palette B ₀
Gradation palette B ₀ set (upper) [3 _H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB ₀₄	Set value to gradation palette B ₀
Gradation palette B ₁ set (lower) [4 _H]	0	1	1	0	0	1	0	0	1	0	0	PB ₁₃	PB ₁₂	PB ₁₁	PB ₁₀	Set value to gradation palette B ₁
Gradation palette B ₁ set (upper) [5 _H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB ₁₄	Set value to gradation palette B ₁
Gradation palette B ₂ set (lower) [6 _H]	0	1	1	0	0	1	0	0	1	1	0	PB ₂₃	PB ₂₂	PB ₂₁	PB ₂₀	Set value to gradation palette B ₂
Gradation palette B ₂ set (upper) [7 _H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB ₂₄	Set value to gradation palette B ₂
Gradation palette B ₃ set (lower) [8 _H]	0	1	1	0	0	1	0	1	0	0	0	PB ₃₃	PB ₃₂	PB ₃₁	PB ₃₀	Set value to gradation palette B ₃
Gradation palette B ₃ set (upper) [9 _H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB ₃₄	Set value to gradation palette B ₃
Gradation palette B ₄ set (lower) [A _H]	0	1	1	0	0	1	0	1	0	1	0	PB ₄₃	PB ₄₂	PB ₄₁	PB ₄₀	Set value to gradation palette B ₄
Gradation palette B ₄ set (upper) [B _H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB ₄₄	Set value to gradation palette B ₄
Gradation palette B ₅ set (lower) [C _H]	0	1	1	0	0	1	0	1	1	0	0	PB ₅₃	PB ₅₂	PB ₅₁	PB ₅₀	Set value to gradation palette B ₅
Gradation palette B ₅ set (upper) [D _H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB ₅₄	Set value to gradation palette B ₅
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

INSTRUCTION TABLE (4)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette B ₆ set (lower) [0 _H]	0	1	1	0	0	1	1	0	0	0	0	PB ₆₃	PB ₆₂	PB ₆₁	PB ₆₀	Set value to gradation palette B ₆
Gradation palette B ₆ set (upper) [1 _H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB ₆₄	Set value to gradation palette B ₆
Gradation palette B ₇ set (lower) [2 _H]	0	1	1	0	0	1	1	0	0	1	0	PB ₇₃	PB ₇₂	PB ₇₁	PB ₇₀	Set value to gradation palette B ₇
Gradation palette B ₇ set (upper) [3 _H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB ₇₄	Set value to gradation palette B ₇
Gradation palette C ₀ set (lower) [4 _H]	0	1	1	0	0	1	1	0	1	0	0	PC ₀₃	PC ₀₂	PC ₀₁	PC ₀₀	Set value to gradation palette C ₀
Gradation palette C ₀ set (upper) [5 _H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC ₀₄	Set value to gradation palette C ₀
Gradation palette C ₁ set (lower) [6 _H]	0	1	1	0	0	1	1	0	1	1	0	PC ₁₃	PC ₁₂	PC ₁₁	PC ₁₀	Set value to gradation palette C ₁
Gradation palette C ₁ set (upper) [7 _H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC ₁₄	Set value to gradation palette C ₁
Gradation palette C ₂ set (lower) [8 _H]	0	1	1	0	0	1	1	1	0	0	0	PC ₂₃	PC ₂₂	PC ₂₁	PC ₂₀	Set value to gradation palette C ₂
Gradation palette C ₂ set (upper) [9 _H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC ₂₄	Set value to gradation palette C ₂
Gradation palette C ₃ set (lower) [A _H]	0	1	1	0	0	1	1	1	0	1	0	PC ₃₃	PC ₃₂	PC ₃₁	PC ₃₀	Set value to gradation palette C ₃
Gradation palette C ₃ set (upper) [B _H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC ₃₄	Set value to gradation palette C ₃
Gradation palette C ₄ set (lower) [C _H]	0	1	1	0	0	1	1	1	1	0	0	PC ₄₃	PC ₄₂	PC ₄₁	PC ₄₀	Set value to gradation palette C ₄
Gradation palette C ₄ set (upper) [D _H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC ₄₄	Set value to gradation palette C ₄
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input. But electric volume is effective after upper and lower register setting.

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INSTRUCTION TABLE (5)

INSTRUCTION	CODE (80 series I/F)							CODE								FUNCTION
	CS	RS	RD	WR	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D _{3z}	D ₂	D ₁	D ₀	
Gradation palette C ₅ set (lower) [0 _H]	0	1	1	0	1	0	0	0	0	0	0	PC ₅₃	PC ₅₂	PC ₅₁	PC ₅₀	Set value to gradation palette C ₅
Gradation palette C ₅ set (upper) [1 _H]	0	1	1	0	1	0	0	0	0	1	*	*	*	PC ₅₄	Set value to gradation palette C ₅	
Gradation palette C ₆ set (lower) [2 _H]	0	1	1	0	1	0	0	0	0	1	0	PC ₆₃	PC ₆₂	PC ₆₁	PC ₆₀	Set value to gradation palette C ₆
Gradation palette C ₆ set (upper) [3 _H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC ₆₄	Set value to gradation palette C ₆
Gradation palette C ₇ set (lower) [4 _H]	0	1	1	0	1	0	0	0	1	0	0	PC ₇₃	PC ₇₂	PC ₇₁	PC ₇₀	Set value to gradation palette C ₇
Gradation palette C ₇ set (upper) [5 _H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC ₇₄	Set value to gradation palette C ₇
Display start command set [6 _H]	0	1	1	0	1	0	0	0	1	1	0	*	SC ₂	SC ₁	SC ₀	Common drive scan start line set
Serial extension CS control [7 _H]	0	1	1	0	1	0	0	0	1	1	1	*	*	*	EX CS	Serial I/F, extension CS port (EXCS) control
Display selection control [8 _H]	0	1	1	0	1	0	0	1	0	0	0	PWM	GL SB	*	*	Gradation display set
RAM data length set [9 _H]	0	1	1	0	1	0	0	1	0	0	1	*	*	CKS	WLS	RAM access data length set 8 bit/16 bit selection
Electric volume control (lower) [A _H]	0	1	1	0	1	0	0	1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀	Electric volume level set (lower bit)
Electric volume control (upper) [B _H]	0	1	1	0	1	0	0	1	0	1	1	*	DV ₆	DV ₅	DV ₄	Electric volume level set (upper bit)
Oscillator Rf control [D _H]	0	1	1	0	1	0	0	1	1	0	1	FFL	RF ₂	RF ₁	RF ₀	RF: oscillator feed back resistor set FFL: oscillator frequency control
discharge [E _H]	0	1	1	0	1	0	0	1	1	1	0	*	*	*	DIS	V _{LCD} , V ₁ ~V ₄ capacitor discharge
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set
Internal register read address set [C _H]	0	1	1	0	1	0	0	1	1	0	0	Register read address			Internal register read out address set	
Internal register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data			Internal register read out	

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input.

But electric volume is effective after upper and lower register setting.

Notice 4) CKS=0: internal oscillation mode

CKS=1: external oscillation mode

Default CSK=0

INSTRUCTION TABLE (6)

INSTRUCTION	CODE (80 series I/F)							CODE							FUNCTION	
	CS	RS	RD	WR	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁		D ₀
Window end X address(lower) [0 _H]	0	1	1	0	1	0	1	0	0	0	0	EX ₃	EX ₂	EX ₁	EX ₀	Window mode X direction end address set
Window end X address(upper) [1 _H]	0	1	1	0	1	0	1	0	0	0	1	*	EX ₆	EX ₅	EX ₄	Window mode X direction end address set
Window end Y address(lower) [2 _H]	0	1	1	0	1	0	1	0	0	1	0	EY ₃	EY ₂	EY ₁	EY ₀	Window mode Y direction end address set
Window end Y address(upper) [3 _H]	0	1	1	0	1	0	1	0	0	1	1	*	EY ₆	EY ₅	EY ₄	Window mode Y direction end address set
Line inversion start Address (lower) [4 _H]	0	1	1	0	1	0	1	0	1	0	0	LS ₃	LS ₂	LS ₁	LS ₀	Line inversion start address set
Line inversion start address (upper) [5 _H]	0	1	1	0	1	0	1	0	1	0	1	*	LS ₆	LS ₅	LS ₄	Line inversion start address set
Line inversion end Address (lower) [6 _H]	0	1	1	0	1	0	1	0	1	1	0	LE ₃	LE ₂	LE ₁	LE ₀	Line inversion end address set
Line inversion end Address (upper) [7 _H]	0	1	1	0	1	0	1	0	1	1	1	*	LE ₆	LE ₅	LE ₄	Line inversion end address set
Line inversion control [8 _H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LR EV	LREV,BT: line inversion display set
Dummy segment driver address set [9 _H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	DM Y	Dummy segment driver address selection
PWM mode control [A _H]	0	1	1	0	1	0	1	1	0	1	0	PW MS	PW MA	PW MB	PW MC	PWM mode selection
RE register set [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Notice 1) * mark is Don't Care

Notice 2) [] The inner side number is an address for internal register read.

Notice 3) The commands that upper/lower register settings are demanded are effective at the point of commands input.
But electric volume is effective after upper and lower register setting.

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(34) INSTRUCTION DESCRIPTION

As shown in instruction table, HM17CM256 has abundant command set.

All the data code and command code are valid only when the chip select signal \overline{CS} is at "0" state. The left side of the following command code and data table are the setting of 80 series CPU interface. Do not use undefined command code.

(34-1) Write display data on RAM

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display RAM write data							

Writing the 8-bit display RAM data at specified X, Y address.

(34-2) Read display data from RAM

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display RAM read data							

Reading out the 8-bit display RAM data from specified X, Y address. One Dummy read cycle is needed after X, Y address is set.

(34-3) X address register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX ₃	AX ₂	AX ₁	AX ₀

(reset :AX₃~AX₄=0_H, read address :0_H)

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	AX ₆	AX ₅	AX ₄

(reset :AX₆~AX₄=0_H, read address :1_H) * : "Don't care"

Setting the X direction address address set. The lower 4-bits are set first, and then upper 3-bits are set later. Please set from lower bit.

(34-4) Y address register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY ₃	AY ₂	AY ₁	AY ₀

(reset :AY₃~AY₀=0_H, read address :2_H)

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	AY ₆	AY ₅	AY ₄

(reset :AY₆~AY₄=0_H, read address :3_H) * : "Don't care"

Setting the Y address of display RAM. The lower 4-bits are set first, and then upper 3-bits are set later. Please set from lower bit.

00_H~51_H is valid range at Y address (AY₆~AY₀). Do not use 52_H~FF_H range. The Y address (AY₆~AY₀) of 50_H, 51_H is used for ICON display data address.

(34-5) Display start line register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

(reset: LA₃~LA₀=0_H, read address: 4_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA ₃	LA ₂	LA ₁	LA ₀

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

(reset: LA₆~LA₄=0_H, read address: 5_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LA ₆	LA ₅	LA ₄

Setting the line address of COM₀. The address stored at the start line register becomes display line at COM₀ line of LCD panel.

The display of LCD panel is done from line address value to the direction of increase.

LA ₆	LA ₅	LA ₄	LA ₃	LA ₂	LA ₁	LA ₀	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
⋮							⋮
1	0	0	1	1	1	1	79

(34-6) n line inversion register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

(reset : N₃~N₀=0_H, read address : 6_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N ₃	N ₂	N ₁	N ₀

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

(reset : N₆~N₄=0_H, read address : 7_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	N ₆	N ₅	N ₄

Setting line number to be inversed to register. Setting range is from 2 to 80. N line inversion register can be effective only when N line inversion command NLIN='1'.

If NLIN="0", the polarity of LCD driving voltage is inverted by every other frame.

N ₆	N ₅	N ₄	N ₃	N ₂	N ₁	N ₀	Inversion line number
0	0	0	0	0	0	0	Forbidden *
0	0	0	0	0	0	1	2
⋮							⋮
1	0	0	1	1	1	1	80

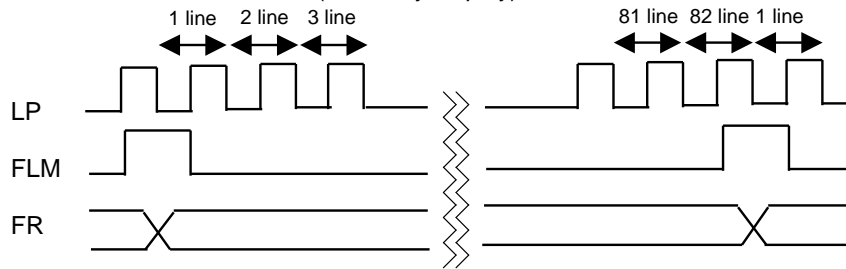
n=N-1

* : N₀~N₆="0" is forbidden.

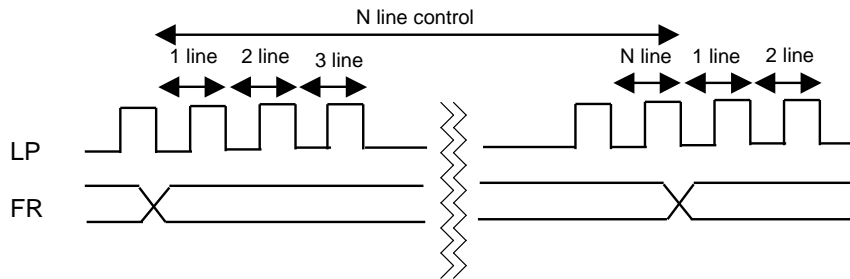
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. Inversion timing

a) when n-line inversion function is OFF(1/82 duty display)



b) when n-line inversion function is ON



(34-7) display control (1) register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

(reset : {SHIFT, MON, ALLON, ON/OFF}=0_H, read address : 8_H)

various control setting of display

a) ON/OFF command

Display ON/OFF control

ON/OFF="0": display OFF (all ports are V_{SS} level)

ON/OFF="1": display ON

b) ALLON command

Setting display data to "1" with independence of RAM data. This command has higher priority than positive display/negative display command. RAM data is not changed.

ALLON="0": normal display state

ALLON="1": turn on all the pixel

c) MON command

BW display / gradation display selection

MON="0": gradation display mode

MON="1": BW display mode

d) SHIFT command

Selection of the shift direction of scan data of common driver output

SHIFT="0": COM₀→COM₇₉ shift

SHIFT="1": COM₇₉→COM₀ shift

(34-8) Display control (2) register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	REF

(reset : {REV, NLIN, SWAP, REF}=0_H, read address :9_H)

various control setting of display

a) REF command

When CPU tries to access display RAM, the relation between X address and write data is changed by command, normal or headfirst.

The output sequence of display data to segment driver can be controlled by register setting. The IC can be placed in panel with less constraint at application.

b) SWAP command

When CPU tries to access display RAM, the display data can be swapped.

SWAP="0": Normal state, D₇~D₀ or D₁₅~D₀ are written to the RAM.

SWAP="1": SWAP mode on : The swapped data of D₇~D₀ or D₁₅~D₀ are written to the RAM.

	SWAP="0"	SWAP="1"
Write data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀
	↓ ↓	↙ ↘
Internal data	d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀	d ₀ d ₁ d ₂ d ₃ d ₄ d ₅ d ₆ d ₇
	↓ ↓	↓ ↓
Read data	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀

c) NLIN command

n line inversion ON/OFF control.

NLIN="0": n line inversion OFF. Polarity signal, FR is inverted every other frame.

NLIN="1": n line inversion ON. The n lines are inverted according to the contents of n line inversion register

d) REV command

The relation between RAM data and display data is defined by this command.

REV="0": The display data are reflected the RAM data until that time.

REV="1": The display data are reflected the opposite data from RAM data.

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(34-9) Increment control register set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI

(reset : {WIN, AIM, AYI, AXI}=0_H, read address : A_H) * : "Don't care"

Sets the display RAM address to increment mode when RAM data is accessed.

Per RAM write or read access, the increment or non-increment settings of X and Y address counter are possible by AIM, AYI, AXI register setting. When accessing consecutive RAM areas by read or write, the address increment operation is possible without setting the read or write address by this register setting.

After setting the auto increment register, the X, Y address should be set lower bits first.

Please revise X, Y address register after increment register setting.

When WIN register is set to "1", the CPU accesses specified area of display RAM. In this case X, Y address should be used with auto increment mode set (AXI="1", AYI="1"). Do not revise X, Y address register when it is not auto increment mode.

WIN="0": normal display RAM access

WIN="1": window area access at display RAM

The window to be accessed is defined by setting the start X, Y address and end X, Y address.

When accessing display with window area mode, please set X, Y start address and then X, Y window end address.

When accessing consecutive RAM area, it is possible to access next location without setting the address by using this command. X, Y address is unknown after auto increment setting. When WIN register is set to "1", the RAM should be accessed after setting start point address and end point address.

And address setting should be done in sequence of start point of X address and Y address, and then end point of X address and Y address after WIN command setting (WIN="1").

The relationship between AIM, AYI, AXI register and X, Y address increment mode is as follow.

AIM	Increment timing selection	Remark
0	Both case of writing in and read out display RAM	①
1	Only when writing in display RAM(read modify)	②

notice①) This mode is valid when read or write is performed on consecutive RAM location.

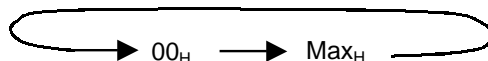
notice②) This mode is valid when read out consecutive data and modifying the data and then write them in again or read → write per access.

AYI	AXI	Increment timing selection	Remark
0	0	No increment	①
0	1	X address auto increment	②
1	0	Y address auto increment	③
1	1	X, Y address auto increment	④

notice①) Regardless of AIM setting, no auto increment for X and Y address

notice②) According to AIM setting, auto increment only for X address.

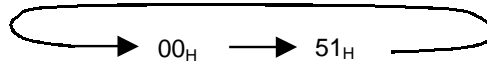
And X address is increased as followed loop according to REF register(SEG output direction setting register) value.



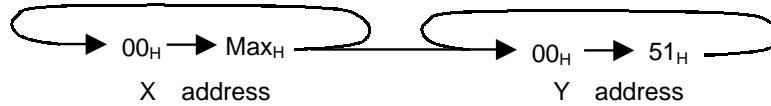
*) Please refer to 「RAM address bitmap」 in 「(10) relation between display RAM and address」

notice③) According to AIM setting, auto increment only for Y address

Y address is increased as followed loop regardless of REF register.



notice④) According to AIM setting, auto increment for X and Y address
 X address is increased to Max_H first and then Y address is increased later.
 You should set X address, Y address in sequence, anything else is forbidden.



*) Please refer to 「RAM address bitmap」 in 「(10) relation between display RAM and address」

And when X, Y auto increment mode operating, window access is possible. When window mode is selected (WIN = "1"), address is increased as following loop.



- a) 8 bit access mode
 The increment operating is as above description.
- b) 16 bit access mode
 Two-byte access is done by single RAM access.
 Address is increased after access.
 X address is increased as (00_H, 01_H, ..., 3E_H, 3F_H) sequence.

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(34-10) Power control register set

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

(reset : {AMPON, HALT, DCON, ACL} = 0_H, read address : B_H)

a) ACL command

This command initializes internal circuit and it is valid only at master operating.

ACL="0": normal state

ACL="1": initialization ON

Just after the execution of ACL command (ACL="1"), D₀ bit is set to 1. But as the initialization process goes on internally, D₀ is reset to "0".

When ACL command is executed, internal reset signal is produced by using local display clock (clock from internal oscillator or from external resistor oscillation mode).

So, after ACL command is executed, it needs to WAIT at least 2 period of the clock for next process beginning.

ACL command is effective only at master mode operation because it uses original oscillator clock.

It is prohibited for slave mode operation to use the internal oscillator or external oscillator.

So, ACL command is impossible at slave mode. Please reset the slave device at \overline{RES} terminal, when needed.

b) DCON command

ON/OFF the internal voltage boosting circuit.

DCON="0": boosting circuit OFF

DCON="1": boosting circuit ON

c) HALT command

Power save mode ON/OFF control

HALT="0": normal state

HALT="1": power save state

The power consumption is decreased near static current at power save mode.

States of each sub-block in power save mode are as follow.

- Oscillator, built-in power supply block stop.
- Stop driving LCD panel, segment drive, the outputs of common driver are all set to V_{SS} level.
- Clock input from OSC₁ port is disabled.
- Display RAM data are conserved.
- Operational modes are preserved as those before power save command was executed.
- V_{LCD} , $V_1 \sim V_4$ become high impedance state.

Make display OFF state before power save mode by HALT command.

And when returning from power save mode, you should display ON after oscillator, power circuit is activated stably.

After display OFF and HALT command, if the display is turned ON before oscillator and power circuit is not activated stably, wrong display can be appeared.

d) AMPON command

ON/OFF the internal OP. amplifier circuit of power block (voltage regulator block, electric volume, voltage converting circuit).

AMPON="0": internal power circuit OP. Amplifier OFF

AMPON="1": internal power circuit OP. Amplifier ON

(34-11) LCD duty set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	*	DS ₂	DS ₁	DS ₀

(reset :{DS₂, DS₁, DS₀}=0_H, read address :C_H) *:"Don't care"

LCD display duty setting

DS ₂	DS ₁	DS ₀	duty
0	0	0	Y direction 80 dot width display, 1/82 duty
0	0	1	Y direction 75 dot width display, 1/77 duty
0	1	0	Y direction 64 dot width display, 1/66 duty
0	1	1	Y direction 45 dot width display, 1/47 duty
1	0	0	Y direction 30 dot width display, 1/32 duty
1	0	1	Y direction 15 dot width display, 1/17 duty
1	1	0	Y direction 36 dot width display, 1/38 duty
1	1	1	Y direction 24 dot width display, 1/26 duty

Partial display is possible by setting duty operation.

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(34-12) Boosting coefficient setting

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

(reset : $\{VU_2 \sim VU_0\} = 0_H$, read address : D_H) * : "Don't care"

coefficient setting of boosting circuit

VU_2	VU_1	VU_0	Boosting multiple
0	0	0	No boosting *
0	0	1	2 times boosting operation
0	1	0	3 times boosting operation
0	1	1	4 times boosting operation
1	0	0	5 times boosting operation
1	0	1	6 times boosting operation
1	1	0	7 times boosting operation
1	1	1	forbidden

* V_{REG} amplifier gain is 1.

(34-13) Bias setting register

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

(reset : $\{B_2 \sim B_0\} = 0_H$, read address : E_H) * : "Don't care"

The bias ratio is selected by this register. 1/10, 1/9, 1/8, 1/7, 1/6, 1/5 biases can be selected by B_2 , B_1 and B_0 register.

B_2	B_1	B_0	bias
0	0	0	Operating under 1/9 bias
0	0	1	Operating under 1/8 bias
0	1	0	Operating under 1/7 bias
0	1	1	Operating under 1/6 bias
1	0	0	Operating under 1/5 bias
1	0	1	Operating under 1/10 bias
1	1	0	forbidden
1	1	1	forbidden

(34-14) RE flag state register setting.

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(reset : $\{TST_0, RE_2, RE_1, RE_0\} = 0_H$, read address : F_H)

Setting the register of command extension register(RE_2 , RE_1 , RE_0). When accessing command register, the extension register corresponding flag should be set first, and then access it. The TST_0 register is that for test, and so please set to "0".

(34-15) Gradation palette register setting

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :0_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₀₃	PA ₀₂	PA ₀₁	PA ₀₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :1_H) *:"Don't care"
(reset :PA₀₄~PA₀₀="00000")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₀₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :2_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA ₁₃	PA ₁₂	PA ₁₁	PA ₁₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :3_H) *:"Don't care"
(reset :PA₁₄~PA₁₀="00101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA ₁₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :4_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA ₂₃	PA ₂₂	PA ₂₁	PA ₂₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :5_H) *:"Don't care"
(reset :PA₂₄~PA₂₀="01010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA ₂₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :6_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA ₃₃	PA ₃₂	PA ₃₁	PA ₃₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :7_H) *:"Don't care"
(reset :PA₃₄~PA₃₀="01110")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA ₃₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :8_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA ₄₃	PA ₄₂	PA ₄₁	PA ₄₀

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$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :9_H) * : "Don't care"
 (reset :PA₄₄~PA₄₀="10001")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA ₄₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :A_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA ₅₃	PA ₅₂	PA ₅₁	PA ₅₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :B_H) * : "Don't care"
 (reset :PA₅₄~PA₅₀="10101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA ₅₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :C_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA ₆₃	PA ₆₂	PA ₆₁	PA ₆₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	0	1

(read address :D_H) * : "Don't care"
 (reset :PA₆₄~PA₆₀="11010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA ₆₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :0_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA ₇₃	PA ₇₂	PA ₇₁	PA ₇₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :1_H) * : "Don't care"
 (reset :PA₇₄~PA₇₀="11111")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA ₇₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :2_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₀₃	PB ₀₂	PB ₀₁	PB ₀₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :3_H) * : "Don't care"
 (reset :PB₀₄~PB₀₀="00000")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₀₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :4_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB ₁₃	PB ₁₂	PB ₁₁	PB ₁₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :5_H) * : "Don't care"
(reset :PB₁₄~PB₁₀="00101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB ₁₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :6_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB ₂₃	PB ₂₂	PB ₂₁	PB ₂₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :7_H) * : "Don't care"
(reset :PB₂₄~PB₂₀="01010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB ₂₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :8_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB ₃₃	PB ₃₂	PB ₃₁	PB ₃₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :9_H) * : "Don't care"
(reset :PB₃₄~PB₃₀="01110")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB ₃₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :A_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB ₄₃	PB ₄₂	PB ₄₁	PB ₄₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :B_H) * : "Don't care"
(reset :PB₄₄~PB₄₀="10001")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB ₄₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :C_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB ₅₃	PB ₅₂	PB ₅₁	PB ₅₀

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$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	0

(read address :D_H) * : "Don't care"
 (reset :PB₅₄~PB₅₀="10101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB ₅₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :0_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB ₆₃	PB ₆₂	PB ₆₁	PB ₆₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :1_H) * : "Don't care"
 (reset :PB₆₄~PB₆₀="11010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB ₆₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :2_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB ₇₃	PB ₇₂	PB ₇₁	PB ₇₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :3_H) * : "Don't care"
 (reset :PB₇₄~PB₇₀="11111")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB ₇₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :4_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₀₃	PC ₀₂	PC ₀₁	PC ₀₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :5_H) * : "Don't care"
 (reset :PC₀₄~PC₀₀="00000")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₀₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :6_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC ₁₃	PC ₁₂	PC ₁₁	PC ₁₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :7_H) * : "Don't care"
 (reset :PC₁₄~PC₁₀="00101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC ₁₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :8_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC ₂₃	PC ₂₂	PC ₂₁	PC ₂₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :9_H) * : "Don't care"
(reset :PC₂₄~PC₂₀="01010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC ₂₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :A_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC ₃₃	PC ₃₂	PC ₃₁	PC ₃₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :B_H) * : "Don't care"
(reset :PC₃₄~PC₃₀="01110")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC ₃₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :C_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC ₄₃	PC ₄₂	PC ₄₁	PC ₄₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0	1	1

(read address :D_H) * : "Don't care"
(reset :PC₄₄~PC₄₀="10001")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC ₄₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :0_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC ₅₃	PC ₅₂	PC ₅₁	PC ₅₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :1_H) * : "Don't care"
(reset :PC₅₄~PC₅₀="10101")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC ₅₄

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :2_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC ₆₃	PC ₆₂	PC ₆₁	PC ₆₀

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\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :3H) * : "Don't care"
 (reset :PC₆₄~PC₆₀="11010")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC ₆₄

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :4H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC ₇₃	PC ₇₂	PC ₇₁	PC ₇₀

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(read address :5H) * : "Don't care"
 (reset :PC₇₄~PC₇₀="11111")

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC ₇₄

Setting each gradation palette. The gradation level is selected among 32 level.

GRADATION LEVEL TABLE

(palette Aj, palette Bj, palette Cj (j=0~7) 3 kinds)

Palette value	Gradation level	Remarks	Palette value	Gradation level	remarks
0 0 0 0 0	0	Initial value of palette 0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Initial value of palette 4
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Initial value of palette 1	1 0 1 0 1	21/31	Initial value of palette 5
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	Initial value of palette 2	1 1 0 1 0	26/31	Initial value of palette 6
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	Initial value of palette 3	1 1 1 1 0	30/31	
0 1 1 1 1	15/31		1 1 1 1 1	31/31	Initial value of palette 7

(34-16) Display start command set

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	*	SC ₂	SC ₁	SC ₀

(reset :{SC₂, SC₁, SC₀}=0_H, read address :6_H) * : "Don't care"

Setting the scan start output of common driver.

SC ₂	SC ₁	SC ₀	SHIFT=0 starting point of COM.	SHIFT=1 starting point of COM.
0	0	0	COM ₀ ~	COM ₇₉ ~
0	0	1	COM ₁₅ ~	COM ₆₄ ~
0	1	0	COM ₃₀ ~	COM ₄₉ ~
0	1	1	COM ₄₅ ~	COM ₃₄ ~
1	0	0	COM ₆₀ ~	COM ₁₉ ~
1	0	1	COM ₇₅ ~	COM ₄ ~
1	1	0	forbidden	forbidden
1	1	1	forbidden	forbidden

SHIFT=0:COM increasing direction scanning

SHIFT=1:COM decreasing direction scanning

(34-17) Serial extension CS control

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	EXCS

(reset :{EXCS}=1_H, read address :7_H) * : "Don't care"

Controlling the output of extension CS at serial interface application.

EXCS pin is I/O pin and used as output at master mode device thus can be controlled.

EXCS="0":EXCS pin output is set to "L".

EXCS="1":EXCS pin output is set to "H".

(34-18) display selection control

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	GLSB	*	*

(reset :{PWM, GLSB}=0_H, read address :8_H) * : "Don't care"

a) GLSB command

The segment driver outputs corresponding to 4 gradation display actually uses 3 bit data to select 4 gradation levels out of 8 gradation levels, 2 bit data out of RAM area and 1 bit out of Gradation LBS.

This command sets the supplement 1 bit Gradation LSB (GLSB) register.

GLSB="0": Set the LSB of segment driver corresponding to 4-gradataion display to "0".

GLSB="1": Set the LSB of segment driver corresponding to 4 gradataion display to "1".

b) PWM command

Selection gradation display mode.

PWM="0": Gradation mode is selected variable 8 gradation among 32 levels.

PWM="1": Fixed 8 gradation display mode.

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(34-19) RAM data length setting

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	CKS	WLS

(reset : {WLS}=0_H, read address : 9_H) * : "Don't care"

WLS: Selection 8 bit access or 16 bit access at RAM access. Access with 16 bits data length is effective only at RAM access. The other accesses are 8 bits access (command access).

WLS="0": RAM access is done by 8 bits data length.

WLS="1": RAM access is done by 16 bits data length

CKS: Selection the oscillator.

CKS="0": internal oscillation mode (default).

Internal oscillation mode should be used under condition of OSC₁ and OSC₂ open.

CKS="1": external oscillation mode.

External oscillation mode should be used under the condition of clock input by OSC₁ port or resistor connection between OSC₁ and OSC₂ port.

(34-20) Electric volume registers setting.

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

(read address : A_H)

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

(read address : B_H) * : "Don't care"

(reset : DV₆~DV₀=00_H)

Setting the electric volume code. The voltage range is divided into 127 levels by this register

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	Output voltage
0	0	0	0	0	0	0	low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	high

The output voltage of V_{REG} is determined by Eq. ①.

$$V_{\text{REG}} = V_{\text{REF}} \times N \quad \cdots \text{①}$$

(N: booster coefficient)

N=1 under the condition of boosting operation is not valid (booster coefficient register, VU=0_H).

The LCD driving voltage V_{LCD} is decided by V_{REG} level or electric volume value (Eq. ②).

$$V_{\text{LCD}} = 0.5 \times V_{\text{REG}} + M \times (V_{\text{REG}} - 0.5V_{\text{REG}}) / 127 \quad \cdots \text{②}$$

(M : DV₆~DV₀ register value)

To prevent over voltage from being generated by electric volume setting, when the register value is set to upper side of electric volume, voltage level is not changed immediately.

When the register value is set to lower side of electric volume, the voltage level is changed instantly.

(34-21) Oscillator circuit Rf control

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	FFL	Rf_2	Rf_1	Rf_0

(reset : {FFL, Rf_2 , Rf_1 , Rf_0 }=0_H, read address : D_H)

The feedback resistance of oscillator circuit can be changed by setting this register.

The frame frequency is changed according to the frequency of oscillator, and the oscillation frequency is determined by the resistor value.

When you set the frame rate, please check the state of LCD display.

Rf_2	Rf_1	Rf_0	Feedback resistance size
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	forbidden
1	1	0	forbidden
1	1	1	forbidden

FFL command : Setting oscillator frequency (frame frequency f_{FLM}). (refer to DC characteristic)

FFL=0 : normal oscillator frequency (set frame frequency, f_{FLM} to 73Hz(Typ))

FFL=1 : high speed oscillator frequency (set frame frequency, f_{FLM} to 150Hz(Typ))

* The value of typical frame frequency f_{FLM} Typ is under following condition.

- Display mode : variable gradation display
- 1/82 Duty
- { Rf_2 , Rf_1 , Rf_0 }=0_H

(34-22) Discharge control

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	*	DIS

(reset : {DIS}=0_H, read address : E_H) * : "Don't care"

The capacitors connected between $V_{LCD} \sim V_4$ and V_{SS} can be discharged by this control. Please refer to capacitor setting example.

DIS="0" : discharge stop

DIS="1" : start discharge

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(34-23) Set read address of internal register

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	0

(reset : {RA₃, RA₂, RA₁, RA₀} = B_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA ₃	RA ₂	RA ₁	RA ₀

Before executing the internal register data read command the address of register should be specified first. For example, when display control (1) is being read out, { RA₃, RA₂, RA₁, RA₀ } = 8_H should be specified first.

Because selected register is corresponded with RE flag, please set RE flag first and then read out the register.

Refer to the command function description and the lists of commands for the address of each register.

(34-24) Internal register data read

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	0/1	0/1	0/1

* : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data read			

This command is used to read out internal register data. Before executing this command, RE flag and the address for internal register to read should be set first.

(34-25) Window end X address set

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset : {EX₃~EX₀} = 0_H, read address : 0_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX ₃	EX ₂	EX ₁	EX ₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset : {EX₆~EX₄} = 0_H, read address : 1_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	EX ₆	EX ₅	EX ₄

When the window area of RAM is specified(WIN="1") to access, the end X address of the window is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later

(34-26) Window end Y address set

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset : {EY₃~EY₀} = 0_H, read address : 2_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY ₃	EY ₂	EY ₁	EY ₀

$\overline{\text{CS}}$	RS	$\overline{\text{RD}}$	$\overline{\text{WR}}$	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset : {EY₆~EY₄} = 0_H, read address : 3_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	EY ₆	EY ₅	EY ₄

When window area of RAM is specified(WIN="1") to access, the end Y address of the window is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later.

(34-27) Line inversion start address set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset :{LS₃~LS₀}=0_H, read address :4_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS ₃	LS ₂	LS ₁	LS ₀

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset :{LS₆~LS₄}=0_H, read address :5_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LS ₆	LS ₅	LS ₄

When the start address of negative display is set on, it is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later. The possible range is LS=00_H~4F_H.

The other values are forbidden. Please set the value under the condition, LS≤LE.

(34-28) Line inversion end address set

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset :{LE₃~LE₀}=0_H, read address :6_H)

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE ₃	LE ₂	LE ₁	LE ₀

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset :{LE₆~LE₄}=0_H, read address :7_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	LE ₆	LE ₅	LE ₄

When the end address of negative display is set on, it is set by this command. The lower 4 bits of address should be set first and then upper 3 bits are set later.

The possible range is LS=00_H~4F_H. The other values are forbidden. Please set the value under the condition, LS≤LE.

(34-29) Line inversion control

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀
0	1	1	0	1	0	1

(reset :{PSC, BT, LREV}=0_H, read address :8_H) * : "Don't care"

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

Setting the status of line inversion display tone.

LREV command : line inversion display ON/OFF setting.

LREV="0": normal display

LREV="1": line inversion display ON. The area specified by line inversion start/stop address is blinked.

The blink type display is controlled by BT command.

When line inversion display is ON(LREV="1"), line inversion start address(LSi) and line inversion stop address(LEi) should be set as following condition.

$$LSi \leq LEi \quad - (1)$$

And following condition is forbidden.

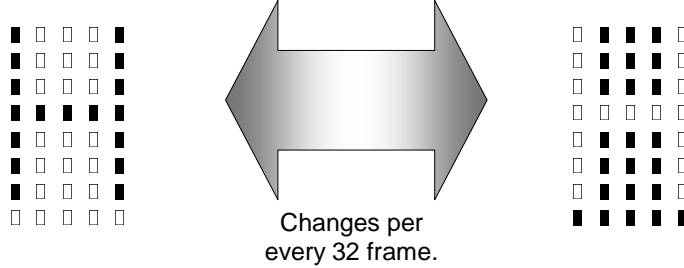
$$LEi < LSi \quad - (2)$$

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BT command : inversion timing selection at line inversion display

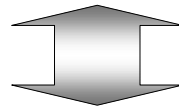
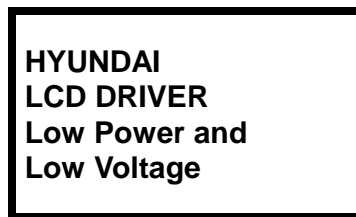
BT="0": Negative tone display in specified area

BT="1": The image of specified area is blinked by every 32 frame.

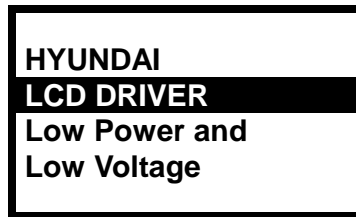


Display example (BT="1")

And be cautious that LREV and BT commands have no influence on dummy segment driver circuit. And the image selected by COMI₀, COMI₁ is excluded.



Changes per every 32 frame.



- ← line inversion start address
- ← line inversion end address

Line inversion display example (LREV="1",BT="1")

(34-30) Dummy segment driver address selection (Refer to dummy segment drive related description.)

\overline{CS}	\overline{RS}	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	1	0	1	1	0	0	1	*	*	*	DMY

(reset : {DMY}=0_H, read address : 8_H) * : "Don't care"

When data is to be written to dummy segment driver, this register is active (DMY="1").

DMY="0": normal display RAM access

DMY="1": display data access to dummy segment driver

Normal segment drivers acquire display data from display RAM, but dummy segment drivers acquire display data from corresponding register not from display RAM. The capacity of register is 4 bytes.

That is correspond to SEGSA₀~SEGSA₃、SEGSB₀~SEGSB₃、SEGSC₀~SEGSC₃ output.

When accessing with DMY = "1", address setting is valid by only X address. There is 4 byte capacity, and so 00_H, 01_H, 02_H, 03_H is valid at 8 bits mode and 00_H, 01_H is valid at 16 bits mode. There is no

relation with Y address setting value.

To access with DMY = "1", register data write-in is possible with increment mode.

(34-31) PWM mode control

\overline{CS}	RS	\overline{RD}	\overline{WR}	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC

(reset :{PWMS, PWMA, PWMB, PWMC}=0_H, read address :8_H) * : "Don't care"

PWM mode selection. (Refer to following wave diagram.)

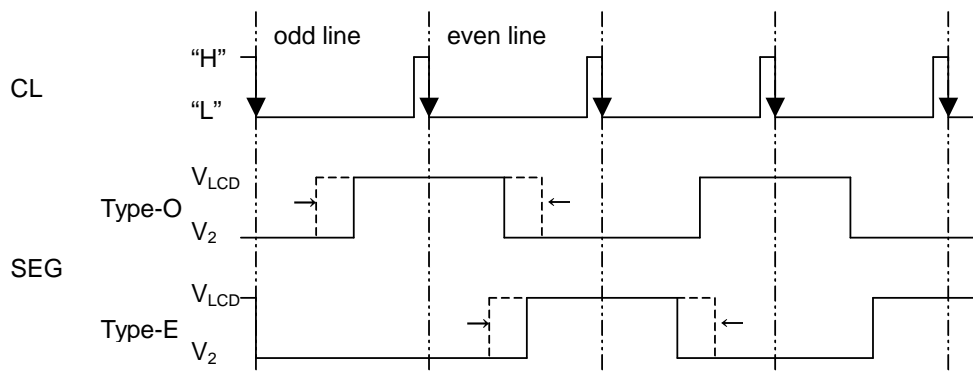
PWMS="0": Selection PWM type1.

PWMA, PWMB, PWMC="0" : PWM type1-O is selectable for each A, B, C data.

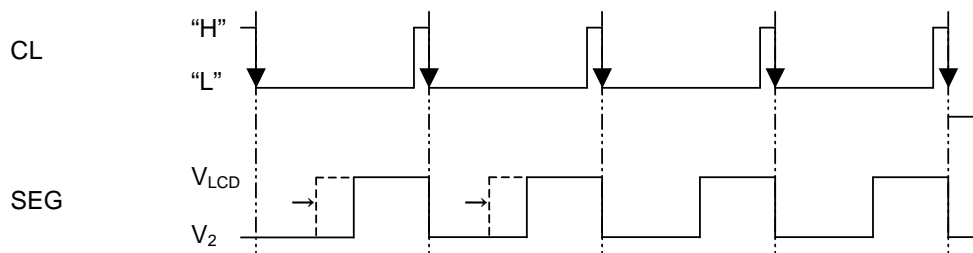
PWMA, PWMB, PWMC="1" : PWM type1-E is selectable for each A, B, C data.

PWMS="1": Selection PWM type2.

a) PWM type1 (PWMS="0")



b) PWM type2 (PWMS="1")



(35) Relation between each setting and COM / display RAM

The COM port number corresponds to Y address of display RAM by SHIFT command, LCD duty command, common display start position command and display start line setting command.

- When display start address was set to "0".

According to LCD duty and display start common line address, the port of COM line and display RAM address (MY) is changed by 15 line unit.

When SHIFT register is set to "0" common line shift to upward direction, and when the value is "1", common line shift to downward direction. When display start address (LA₆~LA₀) is set to "0", the "MY" corresponds to starting position is "0". The MY shift upward direction as display goes on.

In any case, COMI₀=MY80, COMI₁=MY81 .

- When display start line was set except for "0"

According to LCD duty and display start common line address, the port of COM line and display RAM address, MY is changed by 15 line unit.

When SHIFT register is set to "0" common line shift to upward direction, and when the value is "1", common line shift to downward direction. When display start address (LA₆~LA₀) is set to except for "0", the "MY" corresponds to starting position is shift by the amount of set value. The MY shift upward direction as display goes on but MY is set to "0" after MY=79.

In any case, COMI₀=MY80, COMI₁=MY81 .

① display start line set to "0", 1/82 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"000" (1/82 duty)						"000" (1/82 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000000" (display start point 0)						"0000000" (display start point 0)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0	65	50	35	20	5	79	64	49	34	19	4
COM ₂									▲	▲	▲	▲	▲	▲
COM ₃														
COM ₄														0
COM ₅														79
COM ₆														▲
COM ₇														
COM ₈														
COM ₉														
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄				▼										
COM ₁₅				79										
COM ₁₆				0										
COM ₁₇														
COM ₁₈														
COM ₁₉														0
COM ₂₀														79
COM ₂₁														▲
COM ₂₂														
COM ₂₃														
COM ₂₄														
COM ₂₅														
COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉														79
COM ₃₀														0
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄														0
COM ₃₅														79
COM ₃₆														
COM ₃₇														▲
COM ₃₈														
COM ₃₉														
COM ₄₀														
COM ₄₁														
COM ₄₂														
COM ₄₃														
COM ₄₄														79
COM ₄₅														0
COM ₄₆														
COM ₄₇														
COM ₄₈														
COM ₄₉														0
COM ₅₀														79
COM ₅₁														
COM ₅₂														▲
COM ₅₃														
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COM ₅₅														
COM ₅₆														
COM ₅₇														
COM ₅₈														
COM ₅₉														79
COM ₆₀														0
COM ₆₁														
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COM ₆₃														
COM ₆₄														0
COM ₆₅														79
COM ₆₆														▲
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COM ₇₃														79
COM ₇₄														0
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COM ₇₇														
COM ₇₈														
COM ₇₉														
COM ₈₀														
COM ₈₁														

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

③ display start line set to "0", 1/66 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"010" (1/66 duty)					"010" (1/66 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆		"0000000" (display start point 0)					"0000000" (display start point 0)						
COM ₀	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM ₁	0		50	35	20	5			63	49	34	19	4	
COM ₂									63	49	34	19	4	
COM ₃														
COM ₄														0
COM ₅														
COM ₆														
COM ₇														
COM ₈														
COM ₉														
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅			0											
COM ₁₆									63					
COM ₁₇														
COM ₁₈														
COM ₁₉													0	
COM ₂₀														
COM ₂₁														63
COM ₂₂														
COM ₂₃														
COM ₂₄														
COM ₂₅														
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COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄													0	
COM ₃₅														
COM ₃₆														
COM ₃₇														63
COM ₃₈														
COM ₃₉														
COM ₄₀														
COM ₄₁														
COM ₄₂														
COM ₄₃														
COM ₄₄														
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COM ₇₆														
COM ₇₇														
COM ₇₈														
COM ₇₉														
COM ₁	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

HM17CM256

④ display start line set to "0", 1/47 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"011" (1/47 duty)						"011" (1/47 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆		"0000000" (display start point 0)						"0000000" (display start point 0)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0			35	20	5				34	19	4
COM ₂												▲	▲	▲
COM ₃														
COM ₄														0
COM ₅											44			
COM ₆											▲			
COM ₇														
COM ₈						▼								
COM ₉						44								
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅			0											
COM ₁₆														
COM ₁₇														
COM ₁₈														0
COM ₁₉														
COM ₂₀													44	
COM ₂₁														
COM ₂₂														
COM ₂₃													▼	
COM ₂₄													44	
COM ₂₅														
COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉														
COM ₃₀						0								
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄													0	
COM ₃₅														
COM ₃₆														
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COM ₇₇														
COM ₇₈														
COM ₇₉														
COM ₈₀														
COM ₈₁														
			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑤ display start line set to "0", 1/32 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common back scan)					
DS ₂	DS ₁	DS ₀	"100" (1/32 duty)						"100" (1/32 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000000" (display start point 0)						"0000000" (display start point 0)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0					20	5					
COM ₂														
COM ₃														
COM ₄														
COM ₅												29		
COM ₆														
COM ₇														
COM ₈														
COM ₉								29						
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅				0										
COM ₁₆														
COM ₁₇														
COM ₁₈														
COM ₁₉														
COM ₂₀														
COM ₂₁												29		
COM ₂₂														
COM ₂₃														
COM ₂₄														
COM ₂₅														
COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉				29										
COM ₃₀					0									
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄														
COM ₃₅														
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COM ₇₈														
COM ₇₉														
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

HM17CM256

⑥ display start line set to "0", 1/17 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"101" (1/17 duty)					"101" (1/17 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000000" (display start point 0)					"0000000" (display start point 0)						
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0					5						4
COM ₂														
COM ₃														
COM ₄														0
COM ₅													14	
COM ₆														
COM ₇														
COM ₈														
COM ₉								14						
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄			14											
COM ₁₅				0										
COM ₁₆														
COM ₁₇														
COM ₁₈														
COM ₁₉														0
COM ₂₀													14	
COM ₂₁														
COM ₂₂														
COM ₂₃														
COM ₂₄														
COM ₂₅														
COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉													14	
COM ₃₀														
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄														0
COM ₃₅													14	
COM ₃₆														
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COM ₄₉														0
COM ₅₀													14	
COM ₅₁														
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COM ₇₁														
COM ₇₂														14
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COM ₇₄														
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COM ₇₆														
COM ₇₇														
COM ₇₈														
COM ₇₉														5
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑦ display start line set to "0", 1/38 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"110" (1/38 duty)						"110" (1/38 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000000" (display start point 0)						"0000000" (display start point 0)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0				35	20	5					
COM ₂														
COM ₃														
COM ₄														
COM ₅														
COM ₆														
COM ₇														
COM ₈														
COM ₉														
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅				0			35				35			
COM ₁₆														
COM ₁₇														
COM ₁₈														
COM ₁₉													0	
COM ₂₀														
COM ₂₁														
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COM ₂₅														
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COM ₂₇														
COM ₂₈														
COM ₂₉														
COM ₃₀				0			35			35				
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄													0	
COM ₃₅			35											
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COM ₄₂														
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COM ₄₄														
COM ₄₅							0			35				
COM ₄₆														
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COM ₄₈														
COM ₄₉														
COM ₅₀			35								0			
COM ₅₁														
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COM ₆₁							0							
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COM ₆₃														
COM ₆₄														
COM ₆₅				35						0				35
COM ₆₆														
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COM ₇₇														
COM ₇₈														
COM ₇₉							34	19	4	0		35	20	5
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

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⑧ display start line set to "0", 1/26 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"111" (1/26 duty)						"111" (1/26 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000000" (display start point 0)						"0000000" (display start point 0)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			0					5						
COM ₂														
COM ₃							23							
COM ₄														0
COM ₅														
COM ₆														
COM ₇														
COM ₈														
COM ₉														
COM ₁₀														
COM ₁₁												23		
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅			0											
COM ₁₆								23						
COM ₁₇														
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COM ₁₉													0	
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COM ₈₀														
COM ₈₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑨ display start line set to "5", 1/82 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"000" (1/82 duty)						"000" (1/82 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆		"0000101" (display start point 5)						"0000101" (display start point 5)					
COM ₀	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM ₁	5	70	55	40	25	10			4	69	54	39	24	9
COM ₂									▲	▲	▲	▲	▲	▲
COM ₃														
COM ₄									0					5
COM ₅									79					▲
COM ₆									▲					
COM ₇														
COM ₈			▼											
COM ₉			79											0
COM ₁₀			0											79
COM ₁₁														▲
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅			5											
COM ₁₆														
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COM ₈₀	4	69	54	39	24	9	5	70	55	40	25	10		
COM ₈₁	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

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⑩ display start line set to "5", 1/77 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"001" (1/77 duty)					"001" (1/77 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆		"0000101" (display start point 5)					"0000101" (display start point 5)						
COM ₀	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM ₁	5	70	55	40	25	10			69	54	39	24	9	
COM ₂									▲	▲	▲	▲	▲	
COM ₃														
COM ₄														
COM ₅														5
COM ₆									▲					
COM ₇														
COM ₈														
COM ₉			79											
COM ₁₀														79
COM ₁₁														▲
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅			5											
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COM ₁₉													5	
COM ₂₀														
COM ₂₁														
COM ₂₂														
COM ₂₃														
COM ₂₄						79								
COM ₂₅														
COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉														
COM ₃₀						5								
COM ₃₁														
COM ₃₂														
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COM ₃₄													5	
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COM ₄₂														
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COM ₄₄														
COM ₄₅														
COM ₄₆						5								
COM ₄₇														
COM ₄₈														
COM ₄₉														
COM ₅₀													5	
COM ₅₁														
COM ₅₂														
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COM ₇₆														
COM ₇₇														
COM ₇₈														
COM ₇₉														
COM ₈₀														
COM ₈₁	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑪ display start line set to "5", 1/66 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"010" (1/66 duty)					"010" (1/66 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000101" (display start point 5)					"0000101" (display start point 5)						
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			5			55	40	25	10					
COM ₂														
COM ₃														
COM ₄														
COM ₅														
COM ₆														
COM ₇														
COM ₈														
COM ₉														
COM ₁₀														
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COM ₇₉														
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

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⑫ display start line set to "5", 1/47 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"011" (1/47 duty)						"011" (1/47 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000101" (display start point 5)						"0000101" (display start point 5)					
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			5			40	25	10						
COM ₂														
COM ₃														
COM ₄														
COM ₅														
COM ₆														
COM ₇														
COM ₈														
COM ₉						49								
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅				5										
COM ₁₆														
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COM ₇₉														
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑬ display start line set to "5", 1/32 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"100" (1/32 duty)					"100" (1/32 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀		"0000101" (display start point 5)					"0000101" (display start point 5)						
COM ₀	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM ₁	5					25	10						24	9
COM ₂														
COM ₃														
COM ₄														5
COM ₅											34			
COM ₆														
COM ₇														
COM ₈														
COM ₉						34								
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅		5												
COM ₁₆														
COM ₁₇														
COM ₁₈														
COM ₁₉													5	
COM ₂₀														
COM ₂₁												34		
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COM ₂₆														
COM ₂₇														
COM ₂₈														
COM ₂₉			34											
COM ₃₀				5										
COM ₃₁														
COM ₃₂														
COM ₃₃														
COM ₃₄													5	
COM ₃₅														
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COM ₈₀														
COM ₈₁	81	81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

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⑭ display start line set to "5", 1/17 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)					SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"101" (1/17 duty)					"101" (1/17 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000101" (display start point 5)					"0000101" (display start point 5)						
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80
COM ₁			5					10						9
COM ₂														
COM ₃														
COM ₄														5
COM ₅													19	
COM ₆														
COM ₇														
COM ₈														
COM ₉								19						
COM ₁₀														
COM ₁₁														
COM ₁₂														
COM ₁₃														
COM ₁₄			19											
COM ₁₅				5										
COM ₁₆														
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COM ₁₈														
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COM ₂₀													19	
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COM ₈₀														
COM ₈₁			81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

⑮ display start line set to "5", 1/38 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)						
DS ₂	DS ₁	DS ₀	"110" (1/38 duty)						"110" (1/38 duty)						
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"	
LA ₆	LA ₀	"0000101" (display start point 5)						"0000101" (display start point 5)						
COM ₀			80	80	80	80	80	80	80	80	80	80	80	80	
COM ₁			5				40	25	10						
COM ₂															
COM ₃															
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COM ₁₄															
COM ₁₅				5			40			40					
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COM ₁₉													5		
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COM ₂₈															
COM ₂₉															
COM ₃₀					5			40		40					
COM ₃₁															
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COM ₃₃															
COM ₃₄													5		
COM ₃₅			40												
COM ₃₆															
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COM ₄₂															
COM ₄₃															
COM ₄₄															
COM ₄₅							5			40					
COM ₄₆															
COM ₄₇															
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COM ₅₀			40										5		
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COM ₇₈															
COM ₇₉							39	24	9	5			40	25	10
COM ₁			81	81	81	81	81	81	81	81	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

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⑩ display start line set to "5", 1/26 duty by DS₂~DS₀ register

SHIFT set value			SHIFT="0" (common forward scan)						SHIFT="1" (common backward scan)					
DS ₂	DS ₁	DS ₀	"111" (1/26 duty)						"111" (1/26 duty)					
SC ₂	SC ₁	SC ₀	"000"	"001"	"010"	"011"	"100"	"101"	"000"	"001"	"010"	"011"	"100"	"101"
LA ₆	LA ₀	"0000101" (display start point 5)						"0000101" (display start point 5)					
COM ₀	80	80	80	80	80	80	80	80	80	80	80	80	80	80
COM ₁	5						25	10						
COM ₂														
COM ₃							28							
COM ₄														5
COM ₅														
COM ₆														
COM ₇														
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COM ₉														
COM ₁₀														
COM ₁₁													28	
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COM ₁₃														
COM ₁₄														
COM ₁₅		5												
COM ₁₆														
COM ₁₇								28						
COM ₁₈														
COM ₁₉														5
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COM ₂₃			28											
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COM ₇₉														
COM ₁	81	81	81	81	81	81	24	9	5	81	81	81	81	81

The number on the table means MY (Y direction shift address).
 The COM electrodes without MY number are driving with non-selection level signal.
 The Marked line is display start line.

■ ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	CONDITION	PORT	RATINGS	UNIT
supply voltage (1)	V_{DD}	$V_{SS}(0V)$ reference $T_a = +25^\circ C$	V_{DD}	-0.3 ~ +4.0	V
supply voltage (2)	V_{EE}		V_{EE}	-0.3 ~ +4.0	V
supply voltage (3)	V_{OUT}		V_{OUT}	-0.3 ~ +20.0	V
supply voltage (4)	V_{REG}		V_{REG}	-0.3 ~ +20.0	V
supply voltage (5)	V_{LCD}		V_{LCD}	-0.3 ~ +20.0	V
supply voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 ~ $V_{LCD} + 0.3$	V
input voltage	V_I		*1	-0.3 ~ $V_{DD} + 0.3$	V
Storage temperature	T_{stg}			-45 ~ +125	°C

*1 $\overline{D_0} \sim \overline{D_{15}}, \overline{CS}, RS, M/S, \overline{RD}, \overline{WR}, OSC_1, LP, FLM, FR, CLK, \overline{RES}, TEST$ port

■ RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	PORT	MIN	TYP	MAX	UNIT	REMARK
supply voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Recommended operating voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operation temperature	T_{opr}		-30		85	°C	

- *1 The case when internal reference voltage generation circuit (V_{BA} output) is not used.
The voltage compare to V_{SS} port.
- *2 The case when internal reference voltage generation circuit (V_{BA} output) is used.
The voltage compare to V_{SS} port.
- *3 When the boosting circuit is used, supply voltage V_{EE} should be used within the limit.
When driving LCD panel by use of internal boosting circuit, it is possible to short V_{DD} and V_{EE} .
- *4 Please keep the relation, $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} \leq V_{OUT}$.
- *5 When the internal voltage regulator circuit is used, reference voltage V_{REF} should be used within the limit.
Please keep the relation $V_{REF} \leq V_{EE}$.

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ELECTRICAL CHARACTERISTICS

DC Characteristics 1

Unless otherwise noted $V_{SS} = 0V$, $V_{DD} = +1.7 \sim +3.3V$, $T_a = -30 \sim +85^\circ C$

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	PORT	
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1	
Low level input voltage	V_{IL}		0		$0.22 V_{DD}$	V	*1	
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2	
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2	
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3	
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3	
Input leakage current	I_{L1}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*4	
Output leakage current	I_{L0}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	*5	
LCD driver output ON resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$		1	k Ω	*6	
			$V_{LCD} = 6V$		2			4
Static current	I_{STB}	$\overline{CS} = V_{DD}$, $T_a = 25^\circ C$	$V_{DD} = 3V$			15	μA	*7
Oscillator frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^\circ C$	FFL = "0" (normal mode)	TBD	372	TBD	kHz	*8
	f_{OSC2}				84			*9
	f_{OSC3}				12			*10
	f_{OSC4}		FFL = "1" (high speed mode)	TBD	762.6	TBD	*8	
	f_{OSC5}				172.2		*9	
	f_{OSC6}				24.6		*10	
oscillator frequency by External resistor	fr_1	$R_f = 6.2k\Omega$	TBD	TBD	775.2	TBD	kHz	
	fr_2	$R_f = 20k\Omega$			373.9			
	fr_3	$R_f = 51k\Omega$			167.8			
	fr_4	$R_f = 110k\Omega$			84.3			
	fr_5	$R_f = 390k\Omega$			25.8			
	fr_6	$R_f = 820k\Omega$			12.6			
Boosting output voltage	V_{OUT}	N x boosting (N=2~7) $R_L = 30k\Omega$ (between V_{OUT} , V_{SS})	$N * V_{EE}$ * 0.95			V	*11	
Current consumption (1)	I_{DD1}	$V_{DD} = 2.5V$	FFL = "0"	TBD	TBD	μA	*12	
Current consumption (2)	I_{DD2}	7 x boosting (all ON)	FFL = "1"	TBD	TBD			
Current consumption (3)	I_{DD3}	$V_{DD} = 2.5V$ 7x	FFL = "0"	TBD	TBD			
Current consumption (4)	I_{DD4}	boosting(cross check)	FFL = "1"	TBD	TBD			
Current consumption (5)	I_{DD5}	$V_{DD} = 3.0V$	FFL = "0"	TBD	TBD			
Current consumption (6)	I_{DD6}	6 x boosting (all ON)	FFL = "1"	TBD	TBD			
Current consumption (7)	I_{DD7}	$V_{DD} = 3.0V$ 6x	FFL = "0"	TBD	TBD			
Current consumption (8)	I_{DD8}	boosting(cross check)	FFL = "1"	TBD	TBD			
Current consumption (9)	I_{DD9}	$V_{DD} = 3.0V$	FFL = "0"	TBD	TBD			
Current consumption (10)	I_{DD10}	5 x boosting (all ON)	FFL = "1"	TBD	TBD			
Current consumption (11)	I_{DD11}	$V_{DD} = 3.0V$ 5x	FFL = "0"	TBD	TBD			
Current consumption (12)	I_{DD12}	boosting(cross check)	FFL = "1"	TBD	TBD			
Current consumption (13)	I_{DD13}	$V_{DD} = 3.0V$	FFL = "0"	TBD	TBD			
Current consumption (14)	I_{DD14}	4 x boosting (all ON)	FFL = "1"	TBD	TBD			
Current consumption (15)	I_{DD15}	$V_{DD} = 3.0V$ 4x	FFL = "0"	TBD	TBD			
Current consumption (16)	I_{DD16}	boosting(cross check)	FFL = "1"	TBD	TBD			
V_{BA} output voltage	V_{BA}	$V_{EE} = 2.4 \sim 3.3V$	TBD	$0.9 V_{EE}$	TBD	V	*13	
V_{REG} output voltage	V_{REG}	$V_{EE} = 2.4 \sim 3.3V$ $V_{REF} = 0.9 * V_{EE}$ N x boosting (N=2~7)	TBD	$(V_{REF} * N)$	TBD	V	*14	

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics 1

Unless otherwise noted $V_{SS} = 0V$, $V_{DD} = +1.7 \sim +3.3V$, $T_a = -30 \sim +85^\circ C$

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	PORT
Output voltage	V_{LCD}	TBD	TBD	TBD	TBD	V	
	V_1	TBD	TBD	TBD	TBD	V	
	V_2	TBD	TBD	TBD	TBD	V	
	V_3	TBD	TBD	TBD	TBD	V	
	V_4	TBD	TBD	TBD	TBD	V	

• Oscillator frequency, f_{OSC} at each mode, relation external clock frequency, f_{CK} to LCD frame frequency, f_{FLM}

ITEM	Used clock	Display mode	Display duty (1/D)			PORT
			1/82, 1/77, 1/66	1/47, 1/38, 1/32, 1/26	1/17	
Using internal oscillator circuit	f_{OSC}	Variable gradation display	$f_{OSC} / (62 * D)$	$f_{OSC} / (62 * D * 2)$	$f_{OSC} / (62 * D * 4)$	FLM
		Fixed gradation display	$f_{OSC} / (14 * D)$	$f_{OSC} / (14 * D * 2)$	$f_{OSC} / (14 * D * 4)$	
		BW display	$f_{OSC} / (2 * D)$	$f_{OSC} / (2 * D * 2)$	$f_{OSC} / (2 * D * 4)$	
Input external clock	f_{CK}	Variable gradation display	$f_{CK} / (62 * D)$	$f_{CK} / (62 * D * 2)$	$f_{CK} / (62 * D * 4)$	
		Fixed gradation display	$f_{CK} / (14 * D)$	$f_{CK} / (14 * D * 2)$	$f_{CK} / (14 * D * 4)$	
		BW display	$f_{CK} / (2 * D)$	$f_{CK} / (2 * D * 2)$	$f_{CK} / (2 * D * 4)$	

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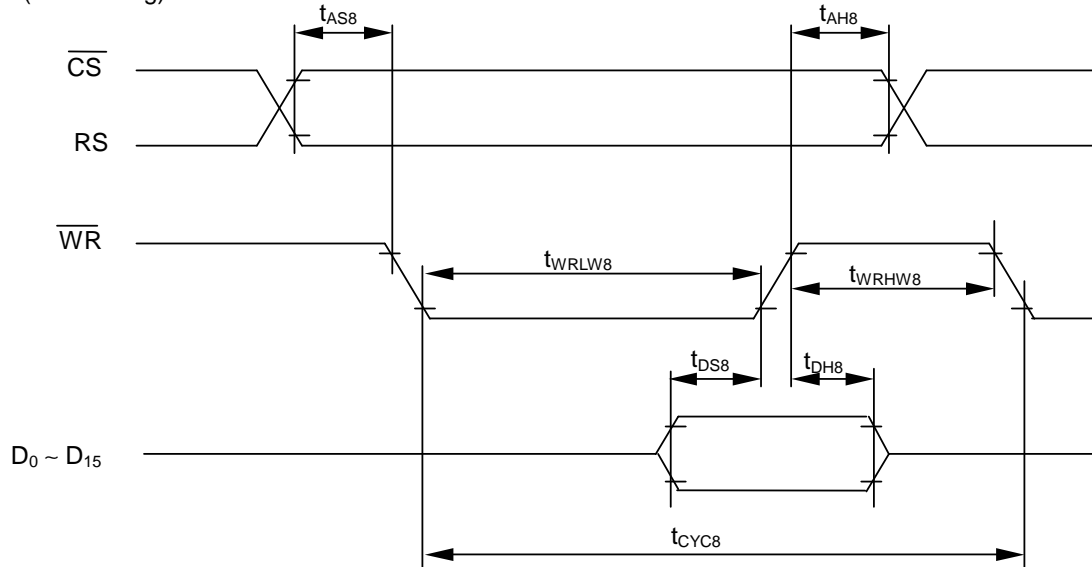
Applied port (* Remark Solves)

- *1 $D_0\sim D_{15}$, \overline{CS} , RS, M/S, \overline{RD} , \overline{WR} , P/S, SEL68, CLK, CL, FLM, FR, \overline{RES} ports
- *2 $D_0\sim D_{15}$ ports
- *3 CL, FLM, FR, CLK ports
- *4 \overline{CS} , RS, M/S, SEL68, \overline{RD} , \overline{WR} , P/S, \overline{RES} , OSC₁ ports
- *5 applicable at $D_0\sim D_{15}$, CL, FLM, FR, CLK = high impedance state
- *6 SEGA₀~SEGA₁₂₇, SEGB₀~SEGB₁₂₇, SEGC₀~SEGC₁₂₇, COM₀~COM₇₉, COMI₀, COMI₁ ports
resistance when being supplied 0.5V between each output ports and power port (V_{LCD} , V_1 , V_2 , V_3 , V_4)
applicable under bias ratio = 1/9
- *7 V_{DD} ports
 V_{DD} current when source clock is stopped, chip selection ($\overline{CS}=V_{DD}$) is non-selection state and no load.
- *8 oscillator frequency when internal oscillator circuit is used (gradation display mode).
applicable under Rf register of oscillator circuit, {Rf₂, Rf₁, Rf₀} = "000"
- *9 oscillator frequency when internal oscillator circuit is used (fixed gradation display mode).
applicable under Rf register of oscillator circuit, {Rf₂, Rf₁, Rf₀} = "000"
- *10 oscillator frequency when internal oscillator circuit is used (BW display mode).
applicable under Rf register of oscillator circuit, {Rf₂, Rf₁, Rf₀} = "000"
- *11 V_{OUT} port
N x boosting (N=2~7). applicable under internal oscillator circuit and internal power circuit are ON state
 $V_{EE} = 2.4\sim 3.3V$, electric volume is MAX("1111111").
bias = 1/5~1/10, 1/82 duty, no load at LCD driver port.
RL = 30k Ω (between V_{OUT} , V_{SS}), CA₁= CA₂=1.0 μF , CA₃=0.1 μF , DCON="1", AMPON="1"
- *12 applicable under internal oscillator circuit and internal power circuit are ON state and no access from CPU.
electric volume is "1111111".
Display is all ON and cross check pattern display (variable gradation display mode), and no load at LCD driver port.
Test condition : $V_{DD}=V_{EE}=V_{REF}$, CA₁=CA₂=1.0 μF , CA₃=0.1 μF , DCON="1", AMPON="1", NLIN="0", 1/82 duty.
- *13 V_{REG} output voltage when V_{BA} output is connected to V_{REF} input, V_{REG} gain is N=1.
- *14 V_{REG} port
 $V_{EE}= 2.4\sim 3.3V$, $V_{REF}= 0.9 V_{EE}$, bias= 1/5~1/10, 1/82 duty, electric volume is "1111111".
Cross hatch state and no load at LCD driver port.
Boosting coefficient N is 2~7 times
Test condition : CA₁=CA₂=1.0 μF , CA₃=0.1 μF , DCON="1", AMPON="1", NLIN="0".

AC CHARACTERISTICS

- SYSTEM BUS READ / WRITE TIMING (80 series CPU interface)

(write timing)



($V_{DD}=2.7\sim 3.3V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	\overline{WR}
Write "L" pulse width	t_{WRLW8}		TBD		ns	\overline{WR}
Write "H" pulse width	t_{WRHW8}		TBD		ns	\overline{WR}
Data setup timing	t_{DS8}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD		ns	$D_0 \sim D_{15}$

($V_{DD}=2.4\sim 2.7V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	\overline{WR}
Write "L" pulse width	t_{WRLW8}		TBD		ns	\overline{WR}
Write "H" pulse width	t_{WRHW8}		TBD		ns	\overline{WR}
Data setup timing	t_{DS8}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD		ns	$D_0 \sim D_{15}$

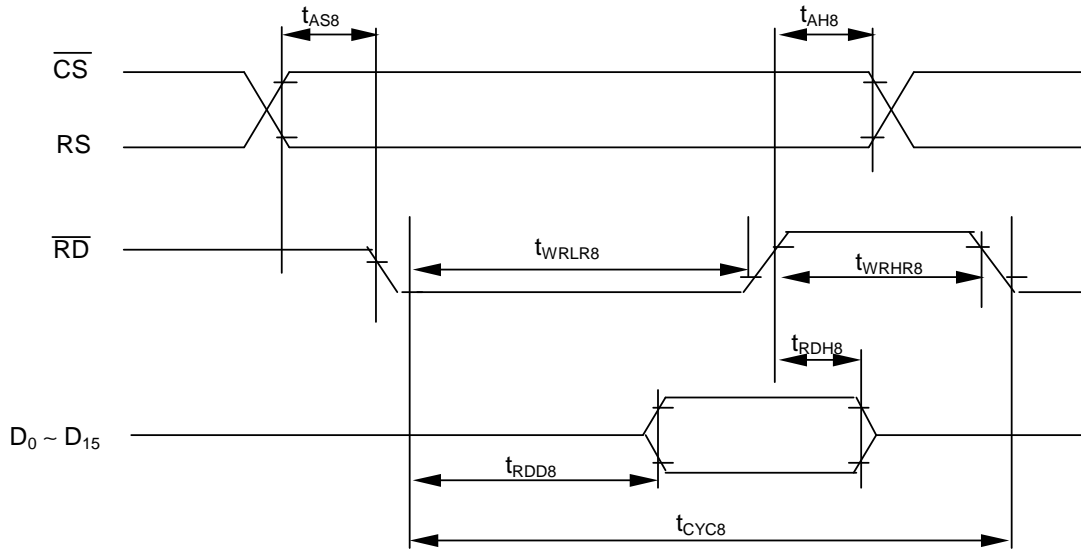
($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	\overline{WR}
Write "L" pulse width	t_{WRLW8}		TBD		ns	\overline{WR}
Write "H" pulse width	t_{WRHW8}		TBD		ns	\overline{WR}
Data setup timing	t_{DS8}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD		ns	$D_0 \sim D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

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(read timing)



($V_{DD}=2.7\sim 3.3V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	
Write "L" pulse width	t_{WRLR8}		TBD		ns	\overline{RD}
Write "H" pulse width	t_{WRHR8}		TBD		ns	\overline{RD}
Data setup timing	t_{DS8}		TBD	TBD	ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD	TBD	ns	$D_0 \sim D_{15}$

($V_{DD}=2.4\sim 2.7V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	
Write "L" pulse width	t_{WRLR8}		TBD		ns	\overline{RD}
Write "H" pulse width	t_{WRHR8}		TBD		ns	\overline{RD}
Data setup timing	t_{DS8}		TBD	TBD	ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD	TBD	ns	$D_0 \sim D_{15}$

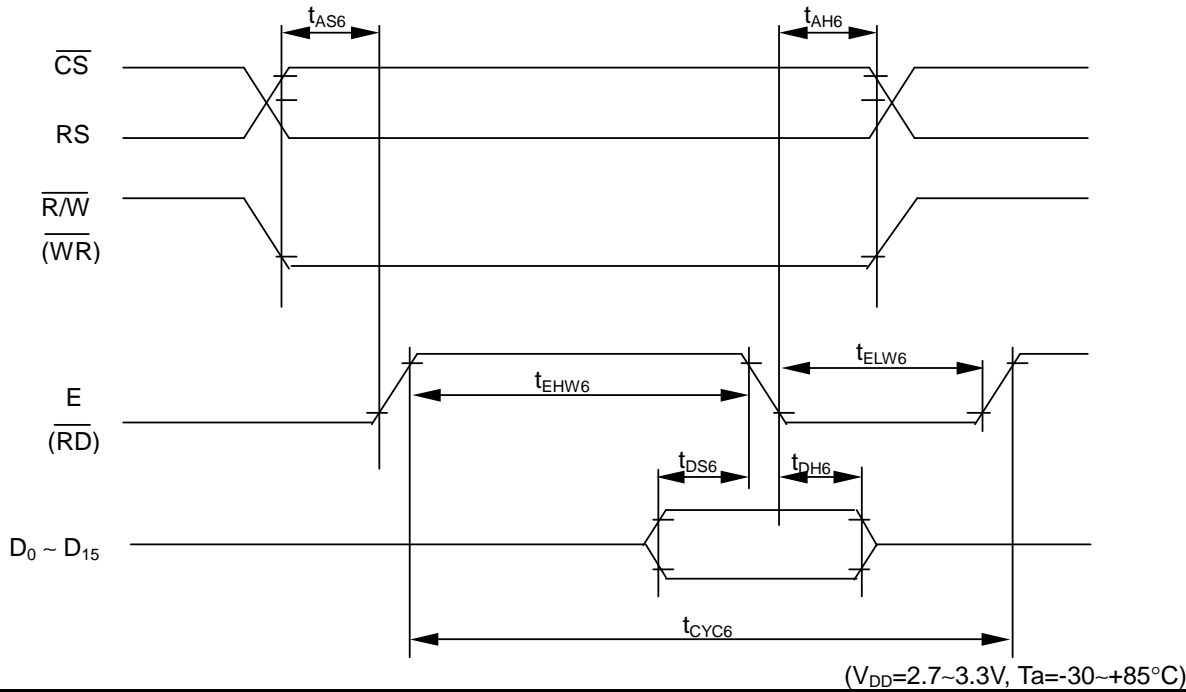
($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH8}		TBD		ns	\overline{CS}
Address setup timing	t_{AS8}		TBD		ns	\overline{RS}
System cycle timing	t_{CYC8}		TBD		ns	
Write "L" pulse width	t_{WRLR8}		TBD		ns	\overline{RD}
Write "H" pulse width	t_{WRHR8}		TBD		ns	\overline{RD}
Data setup timing	t_{DS8}		TBD	TBD	ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH8}		TBD	TBD	ns	$D_0 \sim D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

• SYSTEM BUS READ / WRITE TIMING (68 series CPU interface)

(write timing)



ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	
Enable "L" pulse width	t_{ELW6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHW6}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD		ns	$D_0 \sim D_{15}$

($V_{DD}=2.4\sim 2.7V, T_a=-30\sim +85^\circ C$)

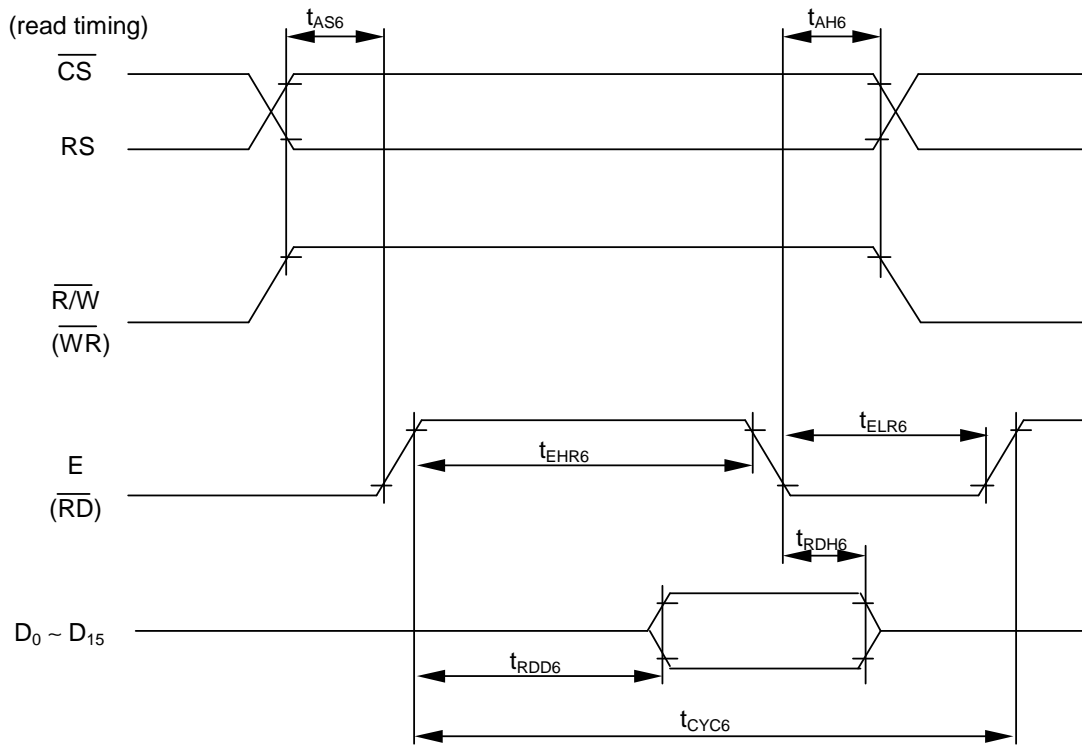
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	
Enable "L" pulse width	t_{ELW6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHW8}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD		ns	$D_0 \sim D_{15}$

($V_{DD}=1.7\sim 2.4V, T_a=-30\sim +85^\circ C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	
Enable "L" pulse width	t_{ELW6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHW6}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD		ns	$D_0 \sim D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

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($V_{DD}=2.7\sim 3.3V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	\overline{E}
Enable "L" pulse width	t_{ELR6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHR6}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD	TBD	ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD	TBD	ns	$D_0 \sim D_{15}$

($V_{DD}=2.4\sim 2.7V$, $T_a=-30\sim +85^{\circ}C$)

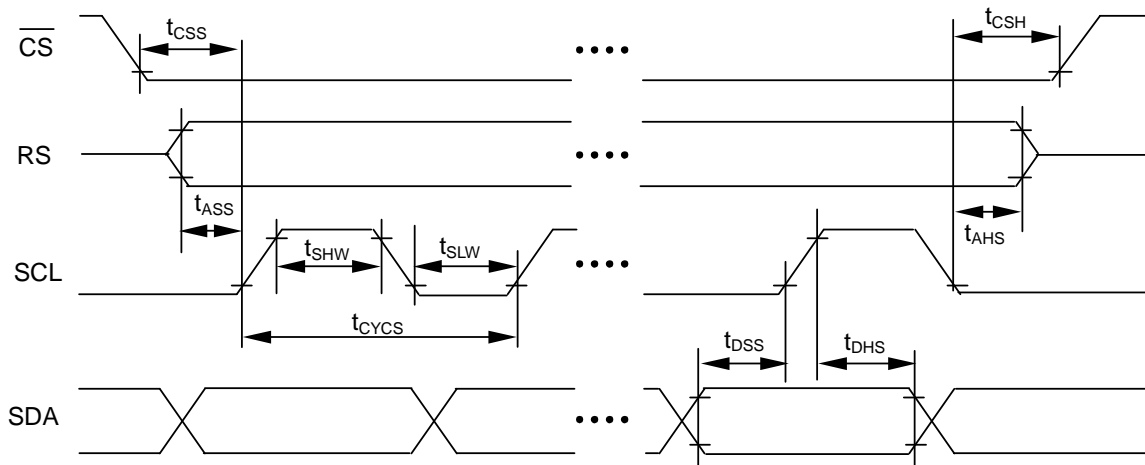
ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	\overline{E}
Enable "L" pulse width	t_{ELR6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHR8}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD	TBD	ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD	TBD	ns	$D_0 \sim D_{15}$

($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Address hold timing	t_{AH6}		TBD		ns	\overline{CS}
Address setup timing	t_{AS6}		TBD		ns	RS
System cycle timing	t_{CYC6}		TBD		ns	\overline{E}
Enable "L" pulse width	t_{ELR6}		TBD		ns	\overline{E}
Enable "H" pulse width	t_{EHR6}		TBD		ns	\overline{E}
Data setup timing	t_{DS6}		TBD		ns	$D_0 \sim D_{15}$
Data hold timing	t_{DH6}		TBD		ns	$D_0 \sim D_{15}$

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

• SERIAL INTERFACE TIMING



($V_{DD}=2.7\sim 3.3V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		TBD		ns	
SCL "H" pulse width	t_{SHW}		TBD		ns	SCL
SCL "L" pulse width	t_{SLW}		TBD		ns	
Address setup timing	t_{ASS}		TBD		ns	RS
Address hold timing	t_{AHS}		TBD		ns	
Data setup timing	t_{DSS}		TBD		ns	SDA
Data hold timing	t_{DHS}		TBD		ns	
\overline{CS} - SCL timing	t_{CSS}		TBD		ns	\overline{CS}
\overline{CS} hold timing	t_{CSH}		TBD		ns	

($V_{DD}=2.4\sim 2.7V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		TBD		ns	
SCL "H" pulse width	t_{SHW}		TBD		ns	SCL
SCL "L" pulse width	t_{SLW}		TBD		ns	
Address setup timing	t_{ASS}		TBD		ns	RS
Address hold timing	t_{AHS}		TBD		ns	
Data setup timing	t_{DSS}		TBD		ns	SDA
Data hold timing	t_{DHS}		TBD		ns	
\overline{CS} - SCL timing	t_{CSS}		TBD		ns	\overline{CS}
\overline{CS} hold timing	t_{CSH}		TBD		ns	

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

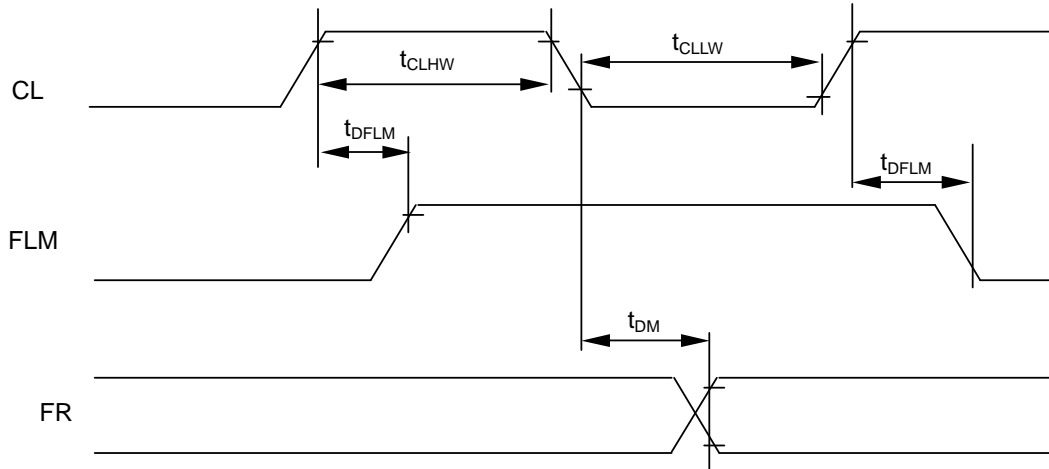
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($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Serial clock cycle	t_{CYCS}		TBD		ns	SCL
SCL "H" pulse width	t_{SHW}		TBD		ns	
SCL "L" pulse width	t_{SLW}		TBD		ns	
Address setup timing	t_{ASS}		TBD		ns	RS
Address hold timing	t_{AHS}		TBD		ns	
Data setup timing	t_{DSS}		TBD		ns	SDA
Data hold timing	t_{DHS}		TBD		ns	
CS – SCL timing	t_{CSS}		TBD		ns	\overline{CS}
\overline{CS} hold timing	t_{CSH}		TBD		ns	

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

• DISPLAY CONTROL TIMING



INPUT TIMING (slave mode)

($V_{DD}=2.4\sim 3.3V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
CL "H" pulse width	t_{CLHW}		80		μs	CL
CL "L" pulse width	t_{CLLW}		80		μs	CL
FLM delay time	t_{DFLM}		-1.0	1.0	μs	FLM
FR delay time	t_{FR}		-1.0	1.0	μs	FR

INPUT TIMING (slave mode)

($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
CL "H" pulse width	t_{CLHW}		80		μs	CL
CL "L" pulse width	t_{CLLW}		80		μs	CL
FLM delay time	t_{DFLM}		-1.0	1.0	μs	FLM
FR delay time	t_{FR}		-1.0	1.0	μs	CL

OUTPUT TIMING (master mode)

($V_{DD}=2.4\sim 3.3V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	CL=15pF	10	500	ns	FLM
FR delay time	t_{FR}		10	500	ns	FR

OUTPUT TIMING (master mode)

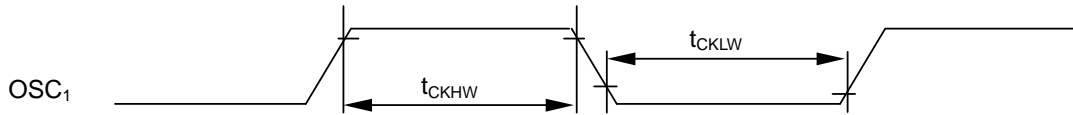
($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
FLM delay time	t_{DFLM}	CL=15pF	10	1000	ns	FLM
FR delay time	t_{FR}		10	1000	ns	FR

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

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• SOURCE CLOCK INPUT TIMING



(V_{DD}=2.4~3.3V, T_a=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC ₁ "H" pulse width (1)	t _{CKHW1}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (1)	t _{CKLW1}		TBD	TBD	μs	*1
OSC ₁ "H" pulse width (2)	t _{CKHW2}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (2)	t _{CKLW2}		TBD	TBD	μs	*2
OSC ₁ "H" pulse width (3)	t _{CKHW3}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (3)	t _{CKLW3}		TBD	TBD	μs	*3

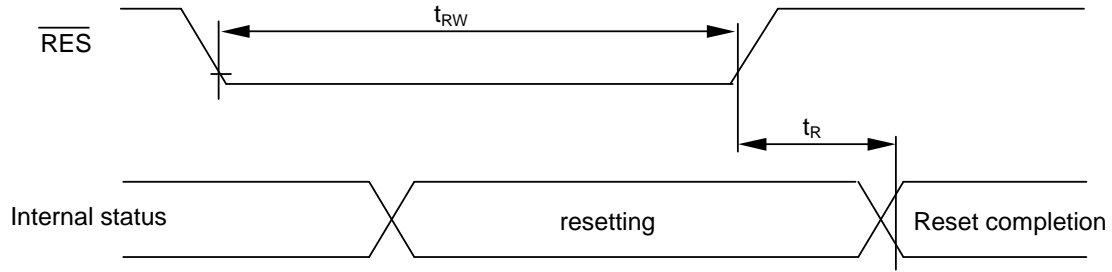
(V_{DD}=1.7~2.4V, T_a=-30~+85°C)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
OSC ₁ "H" pulse width (1)	t _{CKHW1}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (1)	t _{CKLW1}		TBD	TBD	μs	*1
OSC ₁ "H" pulse width (2)	t _{CKHW2}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (2)	t _{CKLW2}		TBD	TBD	μs	*2
OSC ₁ "H" pulse width (3)	t _{CKHW3}		TBD	TBD	μs	OSC ₁
OSC ₁ "L" pulse width (3)	t _{CKLW3}		TBD	TBD	μs	*3

notice) All timing reference is 20% and 80% of V_{DD} and 80%.

- *1 applicable under gradation display , MON="0", PWM="0"
- *2 applicable under fixed gradation display , MON="0", PWM="1"
- *3 applicable under BW display , MON="1"

• RESET INPUT TIMING



($V_{DD}=2.4\sim 3.3V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.0	μs	
\overline{RES} "L" pulse width	t_{RW}		10.0		μs	\overline{RES}

($V_{DD}=1.7\sim 2.4V$, $T_a=-30\sim +85^{\circ}C$)

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT	PORT
Reset time	t_R			1.5	μs	
\overline{RES} "L" pulse width	t_{RW}		10.0		μs	\overline{RES}

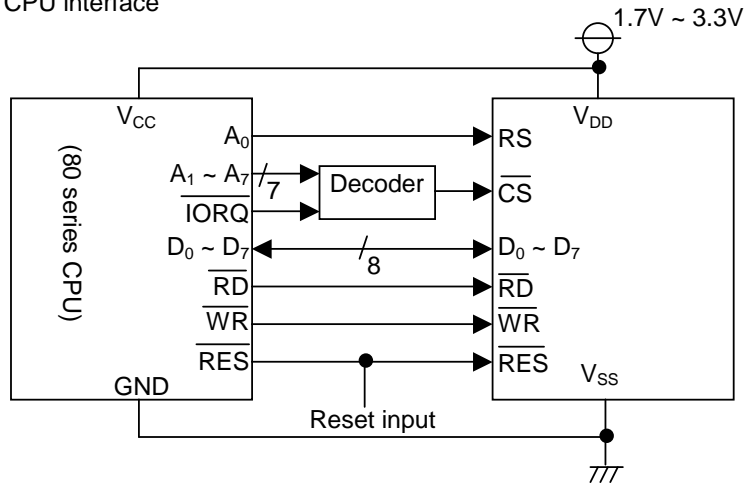
notice) All timing reference is 20% and 80% of V_{DD} and 80%.

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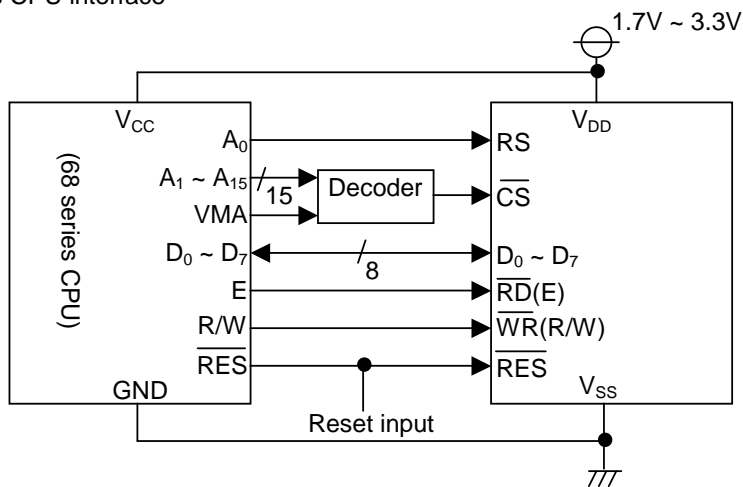
APPLICATION EXAMPLE (reference)

(1) connection with CPU

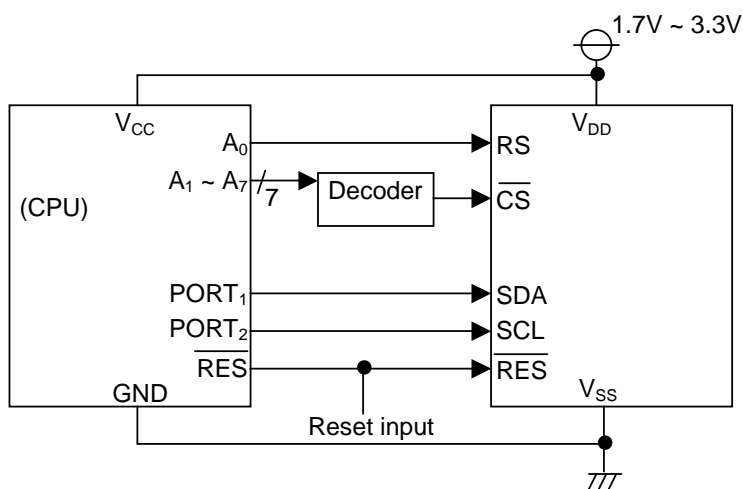
a) 80 series CPU interface



b) 68 series CPU interface



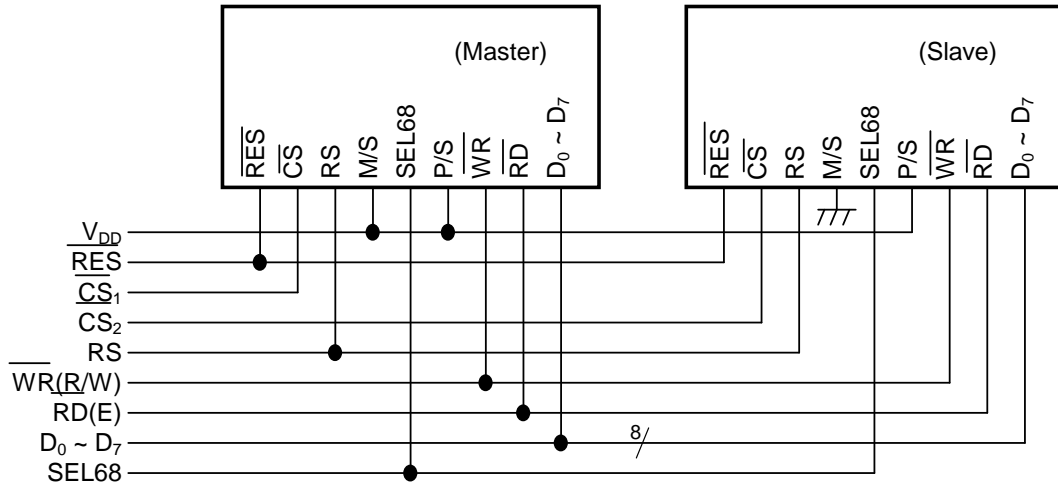
c) CPU connection with serial interface



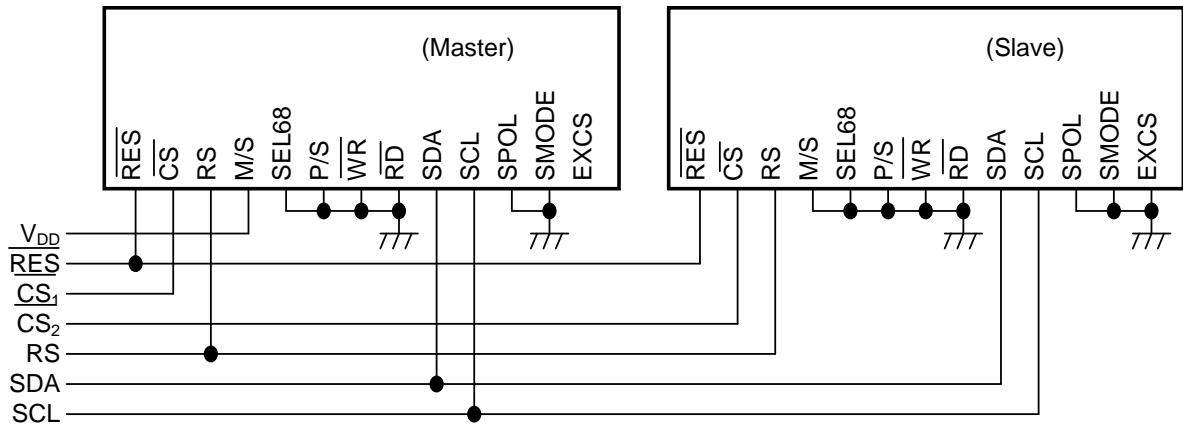
(2) MULTI CHIP INTERFACE

a) connection example of input interface

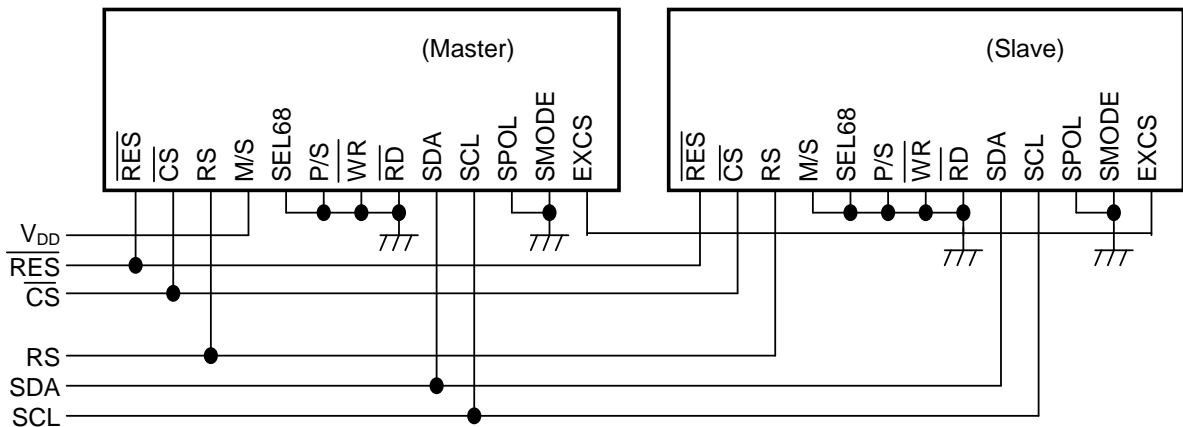
(parallel interface)



(4-line type serial interface)

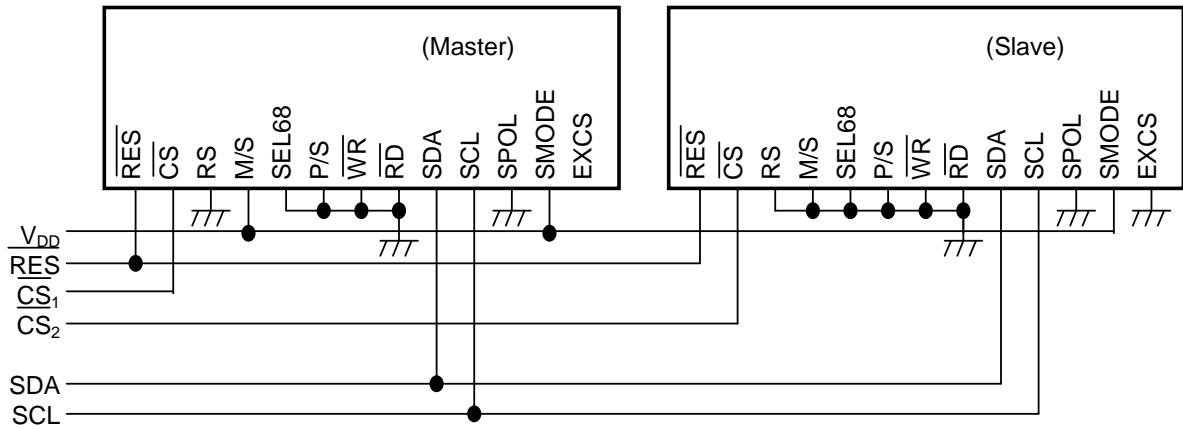


(4-line type serial interface, \overline{CS}_1 common)

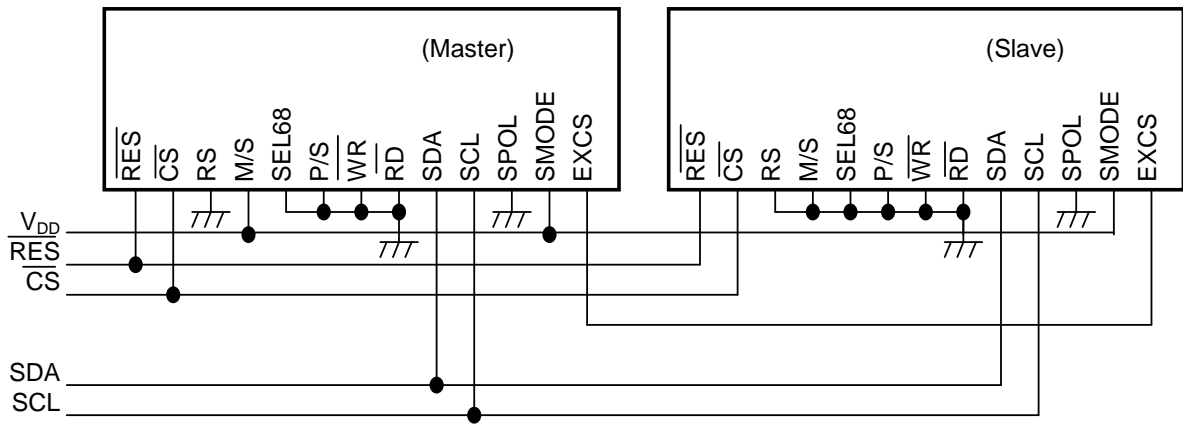


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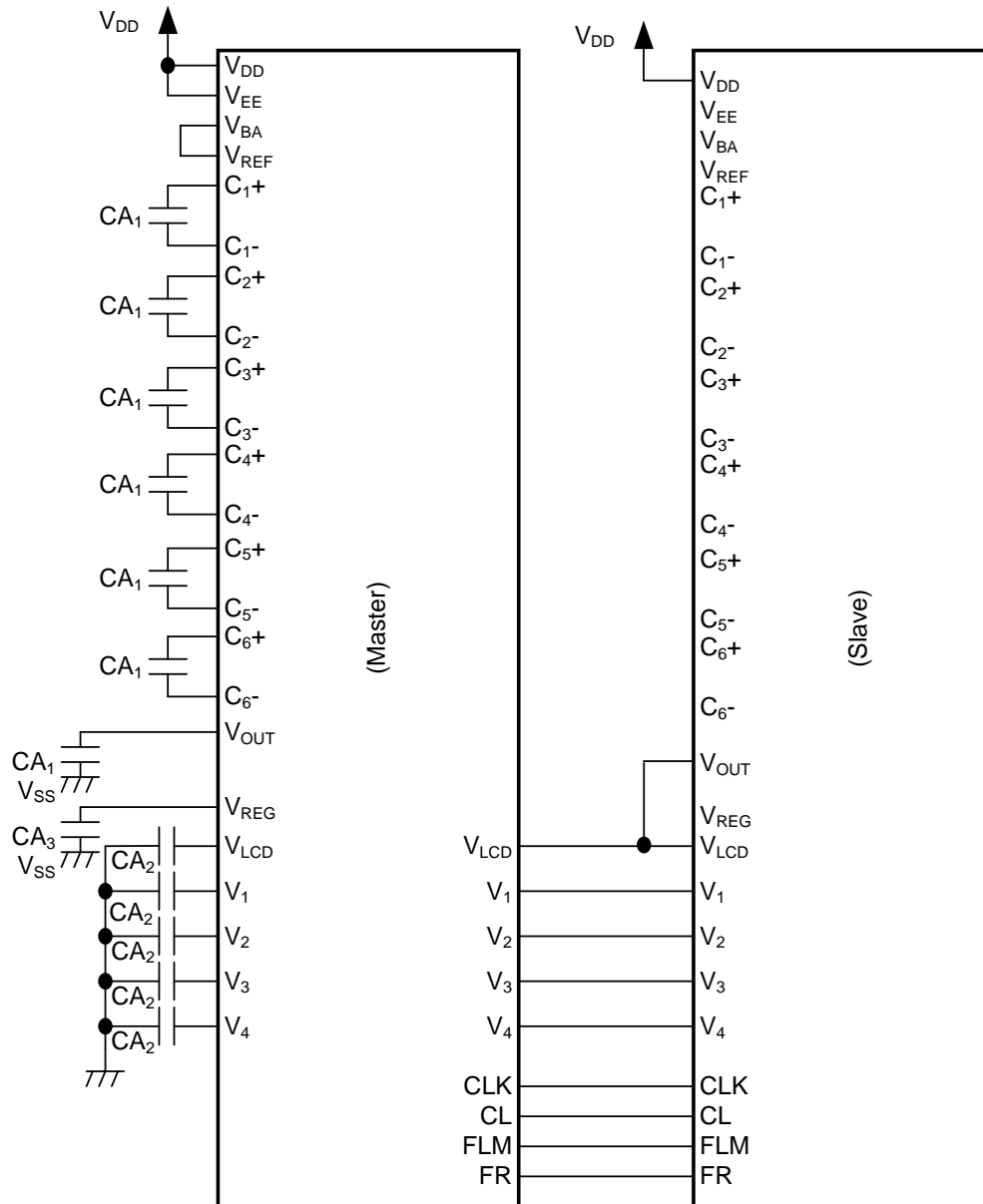
(3-line type serial interface)



(3-line type serial interface, \overline{CS}_1 common)



a) connection example of power supply



Be cautious of using as following description when LCD panel is connected with master/slave structure.

- 1) Display timing is controlled by master chip. The CL, FLM, FR, CLK signals are stopped when master chip is display OFF. When you are going to OFF the display, please OFF the display of slave chip first before master chip display is OFF.
- 2) Boosting circuit and voltage converting circuit is OFF after execution HALT command at master chip, then LCD driving output is V_{SS} level and so display is OFF. And Voltage common is stopped. Because the voltage common of slave chip is stopped, please run slave chip display OFF first and then run master chip HALT command.
- 3) The electric volume setting is valid at master chip only(at upper structure).
- 4) To protect that V_{OUT} is being floated, please connect V_{OUT} with V_{LCD} voltage level.
- 5) Please use under condition that OSC_1 and OSC_2 port of slave chip is OFF.

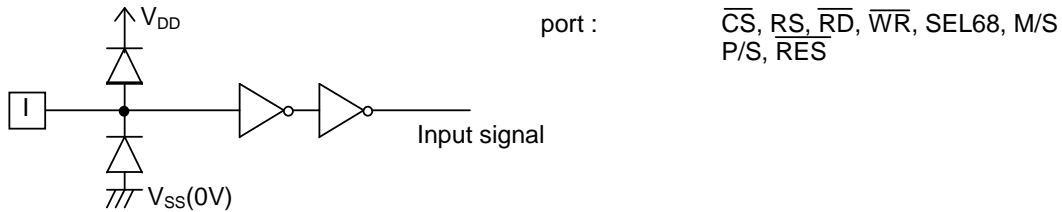
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• Typical characteristic

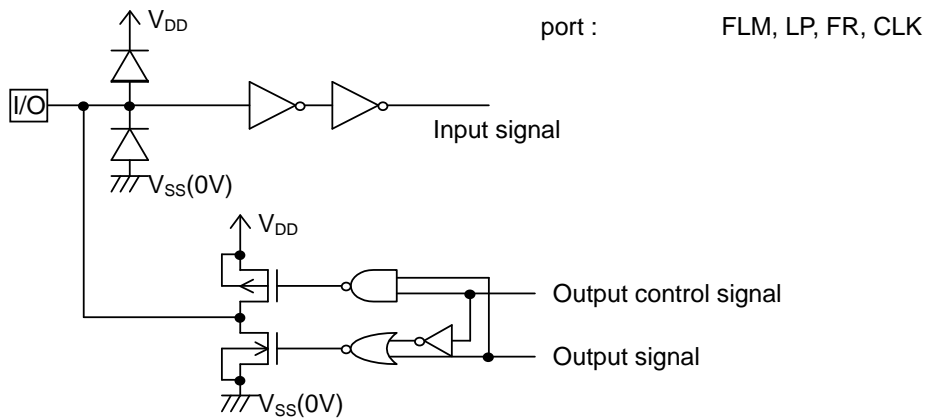
ITEM	CONDITION	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V _{SS} =0V, V _{DD} =3.0V		10		ns

• IN/OUTPUT CIRCUIT STRUCTURE

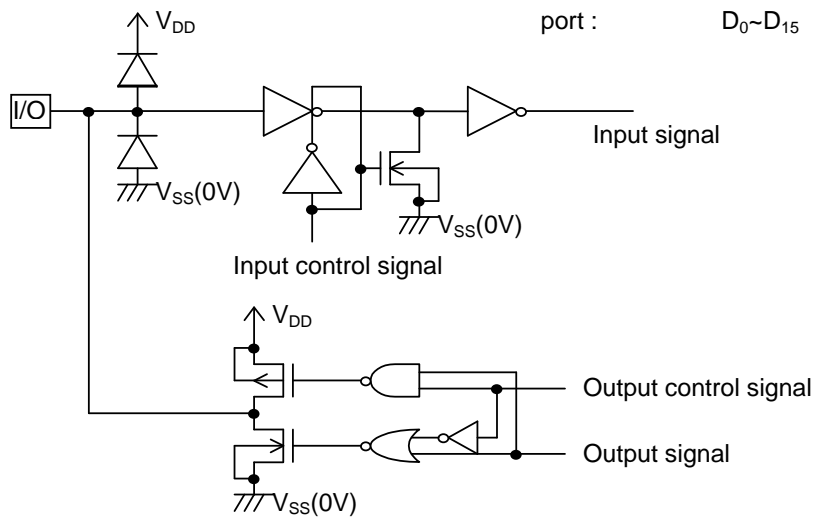
(a) input circuit 1



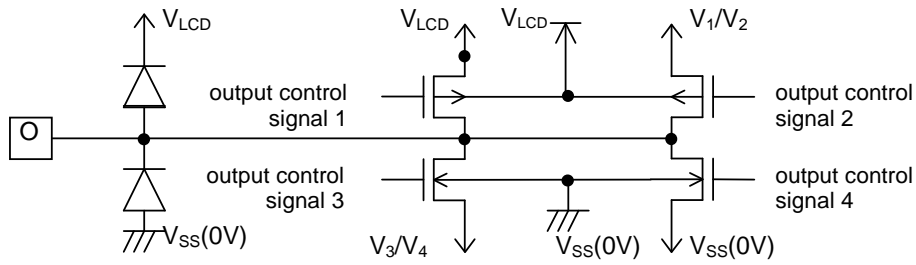
(b-1) in/out circuit 1



(b-2) in/out circuit 2



(c) LCD driver output circuit



Port :
 SEGA₀~SEGA₁₂₇
 SEGB₀~SEGB₁₂₇
 SEGC₀~SEGC₁₂₇
 COM₀~COM₇₉
 COMI₀, COMI₁
 SEGSA₀, SEGSR₁
 SEGSB₀, SEGSB₁
 SEGSC₀, SEGSC₁

<precautions>

The details of this specification was written sincerely, but it is not a letter of guarantee of legal. Especially, the application circuit is just for reference.

This specification do not guarantee that we did not use others patent or intellectual property.