YAMAR Electronics Ltd
Preliminary *Data Sheet*

ISL40 - Independent DC-LIN Slave For Asynchronous Communication Over Noisy Lines

This information is preliminary and may be changed without notice

1 GENERAL

The ISL40 is an innovative VLSI solution for low cost network of I/O peripheral devices communicating over a noisy single wire or a battery power line using the LIN protocol. It provides the means for an economical network of multiple slave devices for applications as controlling motors, reading sensors etc., eliminating the need for a dedicate controller for slave modules.

The device operates as an independent LIN slave in a network controlled by a SIG40 master device, which transmits five types of messages to each one of its slaves; Read, Read Change, Write, Sleep and Change Frequency.
The ISL40 slave device identifies a LIN message addressed to its predefined ID. When a Write message is received, the data part of the message is directed to the corresponding 4 or 8 output pins. When a Read or Read Change message is detected, the slave responds with a LIN2.0 message that contains information on all its 8 inputs or 4 input pins and 4 output pins.
A Sleep command enables power saving. Wakeup messages awaken remote devices.

The device is based on an original multiplex signaling technology. The ISL40 has a LIN message handler, a unique signaling modem and coder/decoder that overcome the hostile communication environment over vehicle battery lines.

The ISL40 capability of communicating over battery-powered line is useful for a wide range of vehicular and industrial applications, such as doors, seats, mirrors, climate control, lights etc.

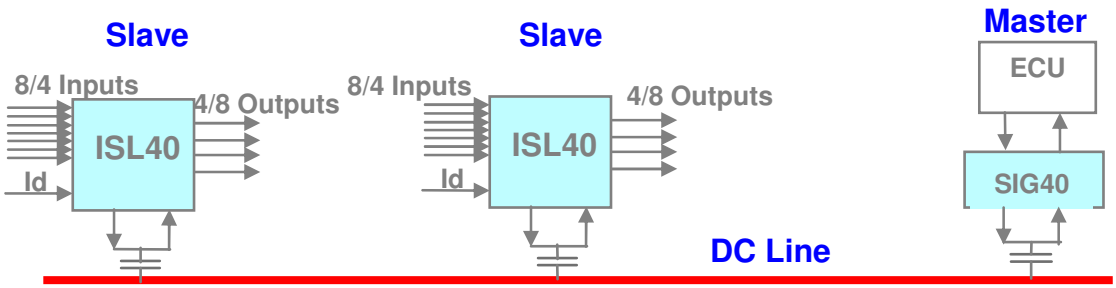


Figure 1.1 - Typical ISL40 Applications

2 OVERVIEW

2.1 Signaling System

The ISL40 device operates as an independent slave in a network controlled by a SIG40 master device that can transmit asynchronous LIN messages to any one of its 15 slave devices. An ISL40 slave device which identifies a Write message addressed to its ID, takes the data part of the message and outputs it to its output pins, while a master Read message is responded by the slave with a message consisting of its sampled input pins. The device receives and transmits special narrow band signaling carrier, which can be differentiated from noise. The receiver receives the signaling patterns, extracting them into the original bits. The rest of the spectrum is reserved for additional communication channels over the same DC noisy lines.

2.2 Channels and Network

The ISL40 operates over one of two preset selectable channels (frequencies) using a single line such as the vehicle's battery power line. A SIG40 master and up to 15 ISL40 slave devices can be connected to each of the channels over the same line. Each of them can receive a message that controls either 4 output pins and returns a message consisting of its 8 input pins status or control 8 output pins and return status of its 4 input pins according to the device setup. By selecting other channels, more than one network may be used over same line for different applications.

Channel frequencies: 3.58MHz to 6.5MHz.
Data transfer rate: up to 57.6Kbps.
Cable length: Depends on external loads connected to the DC line.

2.3 The ISL40 Device

Figure 2.1 outlines the building blocks of the ISL40 device.

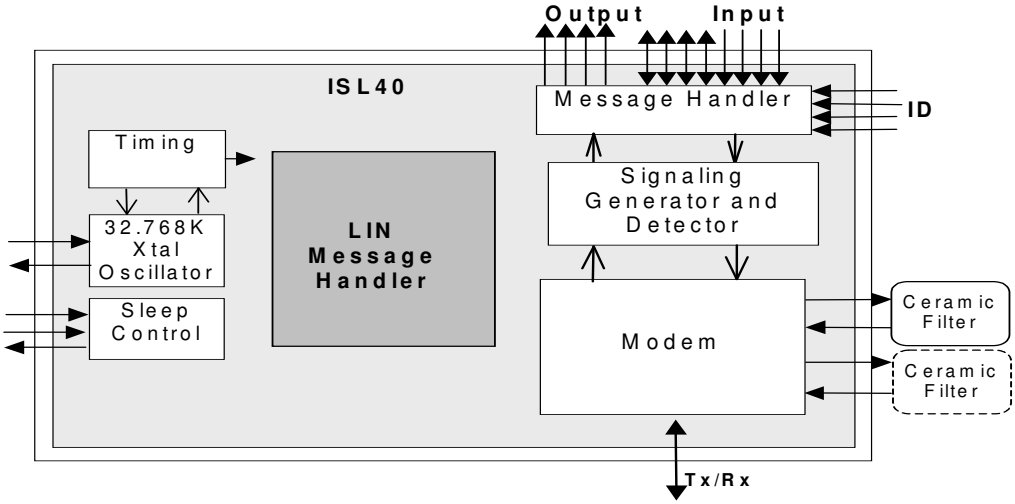


Figure 2.1 - ISL40 Logical Blocks

2.4 Power Management

Sleep Mode, controlled by the host, saves power by disabling most of the circuits.
During Sleep Mode, the device is switched on for a short period to detect Signaling activity on the bus. If no activity is detected, the device is switched off.

3 OPERATION

The following paragraph describes the operation of the ISL40 device.

3.1 Protocol

The device responds to five types of LIN messages: Write, Read, Read Change, Sleep and Change Frequency.
When receiving a Write message with the correct ID, the device outputs to its Output pins the data indicated by the message.
When receiving a Read massage with the correct ID, the device responds to the LIN message with the content of it's Input pins followed by the appropriate checksum according to LIN 2.0 protocol.
When receiving a Read Change massage with the correct ID, the device responds to the LIN message with the first detected change on its input pins followed by the appropriate checksum according to LIN 2.0 protocol.
When receiving a Sleep message the device enters into low power-consumption sleep mode. A wakeup message generated by the master or by any of the slaves, wakes up all the devices on the network.
When receiving Change-Frequency message, the device switch between its two selected frequencies.

3.1.1 Message Construction

The construction of the five types of messages is as follows:

Write message:

The Write message consists of five bytes - sync break, sync field, Identifier, data and checksum.
The identifier byte begins with the device four ID bits, followed by 00 bits and 2 protection bits.
If checksum calculation is successful, the data byte content is transferred to the corresponding output pins. If the device is set to 4 outputs, the four low significant bits (sent first) are transferred to the four output SigOx pins. Otherwise, all 8 bits are transferred. The checksum is calculated according to LIN2.0 specifications. Figure 3.1 shows a generic write message.

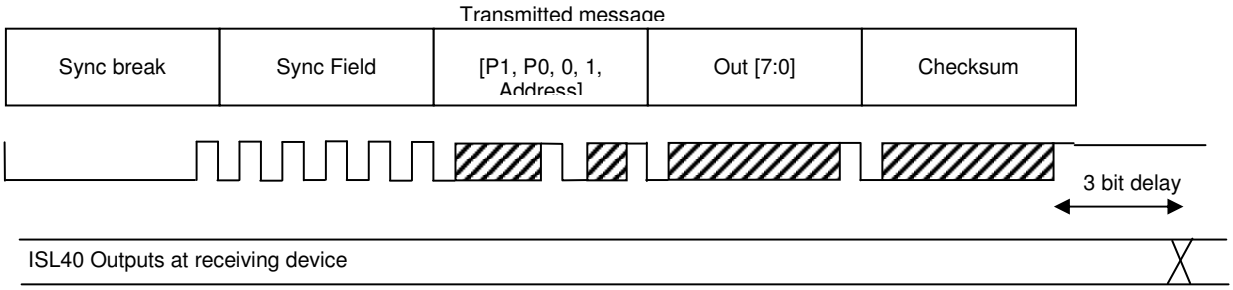


Figure 3.1 Write message

Read message:

The read message gets the status of the ISL40 input pins.
The Read command can either get 4 input pins and 4 MSB's of the output pins or 8 input pins status according to the device setup pins. The Read command can request the current state of the input pins or detect any change caused on the pins since the last read command. If the ISL40 configured to have only 4 input pins, the 4 most significant bits of the data byte would be a read back of the 4 MSB's output pins.

Read-state:

Detecting Read-state header causes the ISL40 to send its input pins current state.
The Read-state message from the master consists of 3 bytes - sync break, sync field and identifier. The identifier of this message begins with the four-bit ID of the device, 00, followed by the 2 protection bits.
The ISL40 responds with a data byte containing its eight input Signal pins followed by the checksum byte. The checksum is the sum of the protected identifier and of the data byte as in LIN2.0.
Figure 3.2 shows a generic read state message.

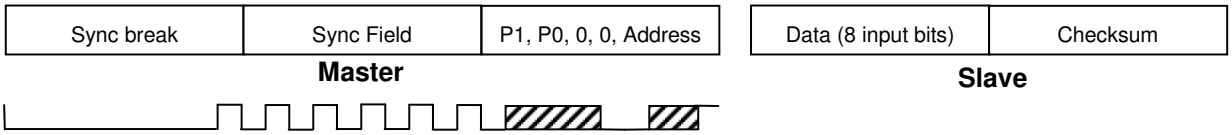


Figure 3.2 Read State message

Read-change:

This header from the master causes the ISL40 to send information on changes of its input pins since the last Read message. The first change on the pin after the Read message switches its sent value. This command enables a detection of a pulse like change that accord between two consecutive Read commands.
Figure 3.3 shows the process of determining the sent value of an input pin.

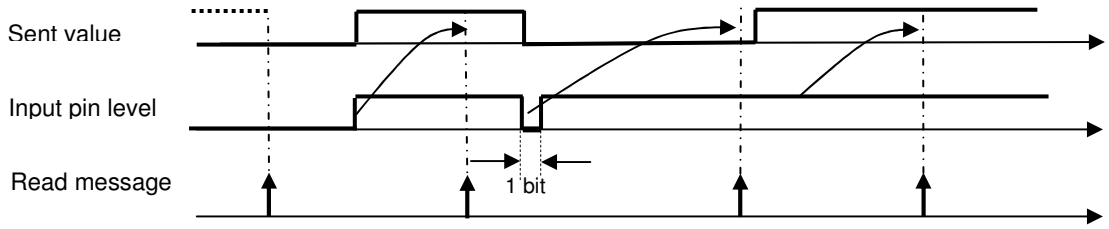


Figure 3.3 - Determining the recent changed value of an input pin

The Read-change message from the master has 3 bytes - sync break, sync field and identifier.
The identifier begins with the destination device four-bit ID, followed by 01 and terminating with 2 protection bits. The response for this Read-changes message is a data byte containing the ISL40`s input pins recent changed value, followed by the checksum byte. The checksum is according to LIN2.0 specifications. Figure 3.4 shows a Read-changes message.

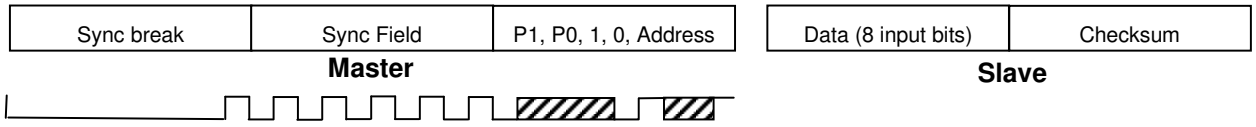


Figure 3.4 Read-changes message

Sleep message:

This type of message consist of 5 bytes - sync break, sync field, “3C” Hex, “00” Hex and checksum.
The sleep message identifier is “3C”Hex as in LIN2.0 specifications and the following data byte “00”Hex.
Upon reception of sync break, sync field, “3C”Hex and “00”Hex bytes, the device enters sleep mode immediately, therefore, as a result its following bytes and checksum are ignored.

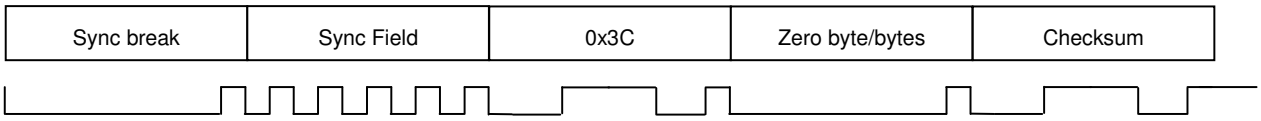


Figure 3.5 Sleep message

Change Frequency message:

This type of message consists of 5 bytes - sync break, sync field, “FE” Hex, “00” Hex and checksum.
The change frequency message identifier is “FE” Hex and the following data byte “00”Hex.
Upon reception of sync break, sync field, “FE” Hex and “00” Hex bytes the frequency changes from F1 to F0 or vise versa.

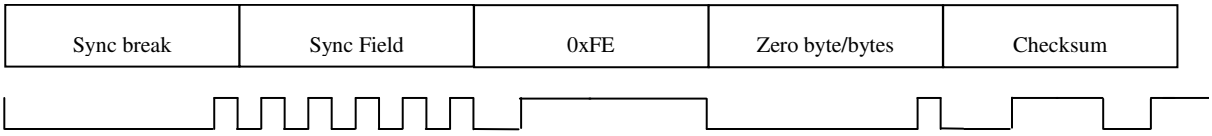


Figure 3.6 Frequency Change message

3.2 Power Management

The device features Sleep mode for power saving. Entering Sleep and waking up are done either locally by dedicated pins, or remotely through activity over the bus.

3.2.1 Entering Sleep mode

The ISL40 can enter sleep mode in the following ways:
1. Local device lowers its nSleep pin.
2. Remote master SIG40 device can enter the ISL40 device into Sleep Mode from Normal mode by transmitting the remote sleep message.
3. The AutoSleep pin is high and no reception occurred for about 8 seconds.

3.2.2 Remote wake up process

The ISL40 can wakeup by a remote SIG40 master or ISL40 device transmits a wakeup message over the bus. During Sleep Mode, the ISL40 wakes up periodically to sense the bus for activity every 32mSec. If a wakeup message is detected, the ISL40 device raises pin INH and lowers pin HDO. If nSleep pin is low upon remote waking up, the local device that lowered it must raise the nSleep back high. Figure 3.6 shows the signals description.

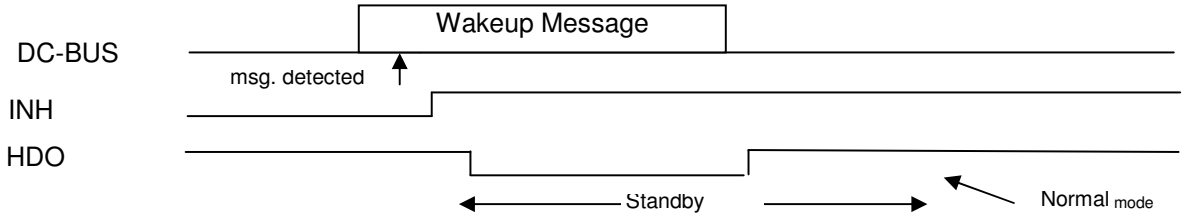


Figure 3.7 - Wakeup from bus message

3.2.3 Wakeup from pin Wake

A transition on pin Wake (caused by an external switch of the application) is used to wake the device. The device then enters Standby mode, raises pin INH, and transmits a wakeup message to the bus. While transmitting the wakeup message to the bus, the device lowers pin HDO. After the transmission is complete the device raises pin HDO. After the transmission is completed the device enters Normal

mode. If nSleep pin is low upon waking up, the local device that lowered it must raise the nSleep back high.

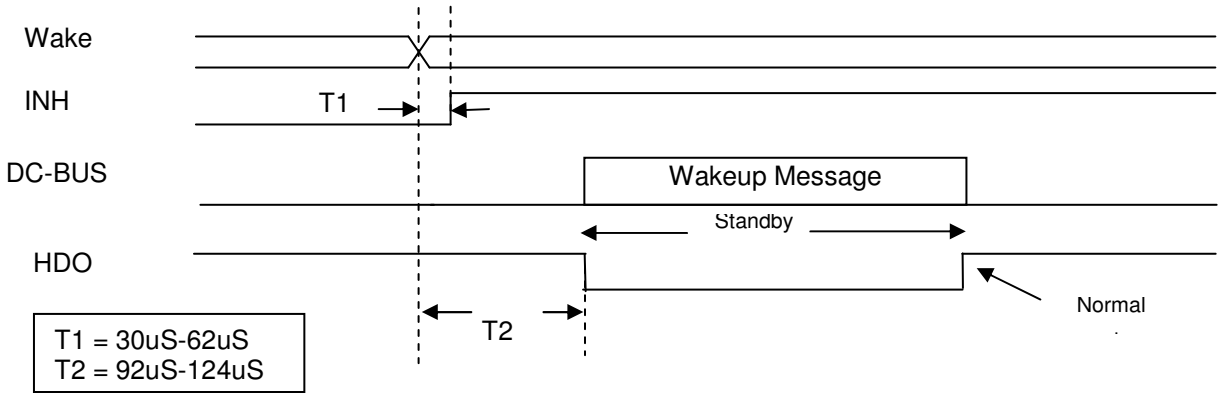


Figure 3.8 - Wakeup from Wake

3.3 ISL40 Configuration

Pins Mode 4 and Mode 3 should be connected to Vcc. The ISL40 operates at default with the following parameters:
Bit rate: 19.2 Kbps
F0=5.5MHz
The following configuration pins enable changing of the default values.

F0F1-3-0 [4]	F0	F1
1111	3.58Mhz	4.5Mhz
1110	3.58Mhz	5.5Mhz
1101	3.58Mhz	6Mhz
1100	3.58Mhz	6.5Mhz
1011	4.5Mhz	5.5Mhz
1010	4.5Mhz	6Mhz
1001	4.5Mhz	6.5Mhz
1000	4.5Mhz	Reserved
0111	10.7Mhz	Reserved
0110	5.5Mhz	Reserved
0101	5.5Mhz	Reserved
0100	6Mhz	Reserved
0011	6Mhz	Reserved
0010	6.5Mhz	Reserved
0001	6.5Mhz	Reserved
0000(default)	5.5Mhz	6.5Mhz

BitRate1-0 [2]	10 = 57.6Kbps 01 = Reserved	11 = 38.4Kbps 00 = 19.2Kbps

Signal	High (“1”)	Low (“0”)
AutoSleep	Auto Sleep On	Auto Sleep Off
nExtendIn	SIG[7:4] are outputs	SIG[7:4] are inputs
ID[3:0]	Defines device ID	
InterHop	InterHop On	InterHop Off

4 ISL40 SIGNALS

Device signals are defined in table 4.1.

Table 4.1 - Device signals

Control signals

HDO	CMOS	O	20
nSleep	CMOS	I	28
INH	CMOS	I	24
Wake	CMOS	I	33
nReset	CMOS_Reset+PU	I	32
InterfHop	CMOS + PD	I	36
Interfer	CMOS	O	21

Front-end signals

RxOn	CMOS	O	16
DRxP	CMOS	I	6
DRxN	CMOS	I	5
MF0nF1	CMOS	O	41
TxOn	CMOS	O	14
DTxO	Buf+Slew+3 State	B	13
OscIn	CMOS	I	1
OscOut	CMOS	O	2

Configuration signals

F0F1-0	CMOS+PD	I	42
F0F1-1	CMOS+PD	I	43
F0F1-2	CMOS+PD	I	34
F0F1-3	CMOS+PD	I	35
BitRate0	CMOS+PD	I	45
BitRate1	CMOS+PD	I	46
Mode3 =1	CMOS+PD	I	4
Mode4 =1	CMOS+PD	I	7
nExtendIn	CMOS+PD	I	40
AutoFreqCh	CMOS+PD	I	26
AutoSleep	CMOS+PD	I	27

Power signals

Vcc	Power	P	48
Vcc	Power	P	3
Gnd	Power	P	12
Gnd	Power	P	19
VccPLL	Power	P	37
GndPLL	Power	P	47

Sig I/O signals

SigIn0	CMOS+PD	I	38
SigIn1	CMOS+PD	I	39
SigIn2	CMOS+PD	I	25
SigIn3	CMOS+PD	I	29
SigIO4	BiDirectional+PD	B	23
SigIO5	BiDirectional+PD	B	15
SigIO6	BiDirectional+PD	B	17
SigIO7	BiDirectional+PD	B	18
SigO0	CMOS	O	8
SigO1	CMOS	O	9
SigO2	CMOS	O	10
SigO3	CMOS	O	11
ID0	CMOS+PD	I	30
ID1	CMOS+PD	I	31
ID2	CMOS+PD	I	44
ID3	CMOS+PD	I	22

***PD** = internal pull down resistor*

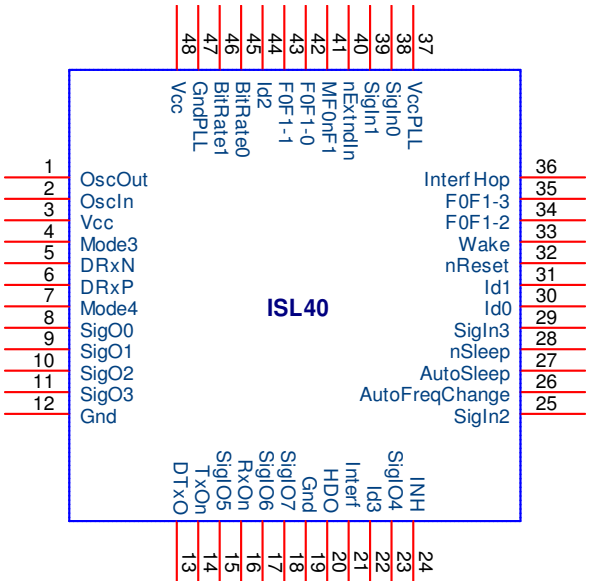


Figure 4.1 - ISL40 Pinout

4.1 Application interface

4.1.1 HDO

The HDO pin outputs the data that is being received from the DC-BUS. It can be used to monitor the incoming data.

4.1.2 SigIn[0:3]

Four input signals to the ISL40. On a Read or Read Change command the pins status is being send back to the Master in the lower nibble of the returned data byte.

4.1.3 SigO[0:3]

Four output signals from ISL40. The pins state is changed when the Master issues a Write command. The pins status is defined in the lower nibble of the Write command's OUT byte.

4.1.4 SigIO[4:7]

Four input or output signals of the ISL40, depending on the nExtendIn pin. When configured as inputs their status is being send back to the Master in the upper nibble of the return data byte. When they are configured as outputs their state is defined in the upper nibble of the Write command's OUT byte.

4.1.5 nExtendIn

Determines if the SigIO[4:7] pins are inputs or outputs. 1= outputs, 0 = inputs.

4.1.6 ID[1:4]

Four ID address input pins. Using the ID address each ISL40 on the network or a specified group of ISL40 can receive individual commands.

4.2 Sleep control

4.2.1 AutoSleep

When AutoSleep pin is set to High the device will automatically enters sleep mode after about 8 seconds without reception.

4.2.2 nSleep

Sleep control input from external signal. Should be connected to High (Vcc).

4.2.3 Wake

Local wakeup input. Negative or positive edge triggered. This pin can be connected to an external switch in the application. When the pin is triggered the device will wake up and send a wake up message to all the devices on the network.

4.2.4 INH

Inhibit output for enabling the host (or an external voltage regulator powering the host. This output is LOW when in Sleep Mode, and HIGH in normal operation and after a wakeup event.

4.3 Frequency control

4.3.1 AutoFreqCh

When high, the device automatically switches frequency after about 4 seconds without bus activity.

4.3.2 InterfHop

When high, a detection of interference, switches the operating frequency. If at the new frequency, no reception occurred for 2 sec, the operating frequency is switched back.
For designs with a single channel this pin should be tied to ground.

4.3.3 Interfer

Output signal is raised while interference is detected on the DC-BUS.

4.3.4 MF0nF1

Indicates the operating frequency, this is the configured frequency unless automatic frequency change has been enabled and caused.

4.4 Line Interface

4.4.1 DTxO

Modulated transmit signal output.

4.4.2 TxOn

High when the device is transmitting a message.

4.4.3 RxP

Input to the internal comparator positive pin. It swings around RxN.

4.4.4 RxN

Input to the internal comparator negative pin. Its value should be about Vcc/2.

4.4.5 RxOn

High when the device is in receive mode.

4.4.6 Power Signals

There are three sets of power signals, (Vcc, Gnd)*2 and VccPLL, GndPLL. See 4.7 for details.

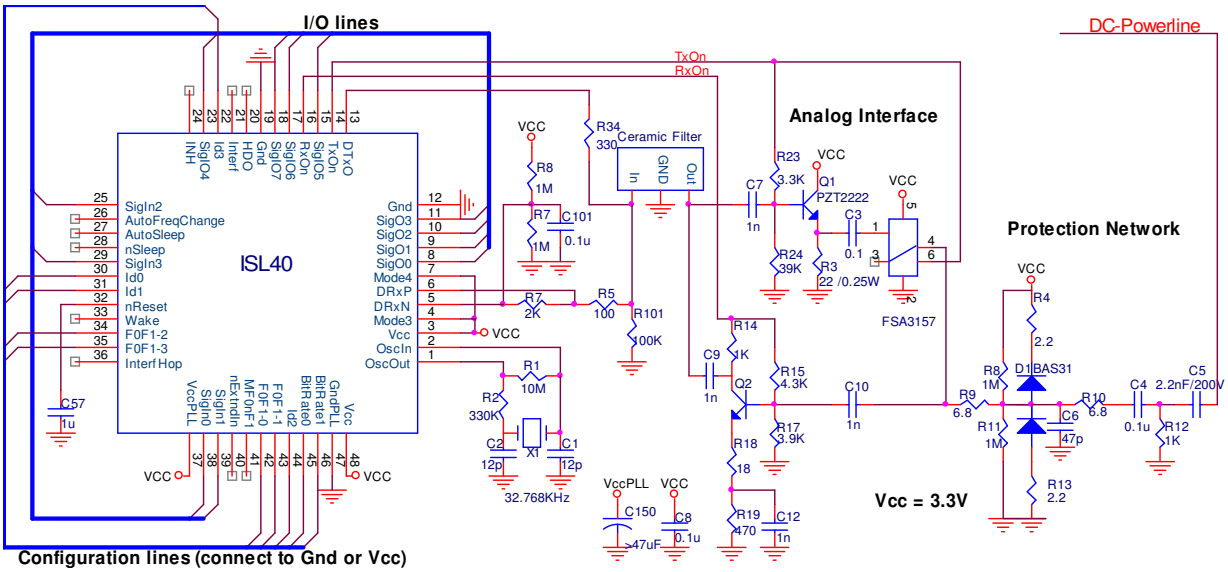


Figure 4.2 – Typical single channel line interface circuit

Note: The FSA3157 can be replaced with an analog switch.

4.5 Ceramic Filter

The ISL40 is designed to operate with one ceramic filter for transmission and reception. However, if switching between two channels is desired, two ceramic filters are required. The minimum allowable bandwidth of the ceramic filters is +/-70 kHz @ 3dB. Narrower bandwidth limits the maximal bit rate.

The ISL40 selectable frequencies are designed according to the market available ceramic filters.

Nominal freq.	3 db BW	20db BW	Insertion loss	Stop band attenuation	In/Out imped.	Murata part #	Oscilent part #
MHz	KHz min.	KHz max.	dB max.	dB min.	Ohm		
*3.58	+/-40	530	6.0	25	530	SFSH3.58MCB	
4.5	+/-70	750	6.0	30	1000	SFSL4.5MDB	773-0045
5.5	+/-80	750	6.0	30	600	SFSL5.5MDB	773-0055
6.0	+/-80	750	6.0	30	470	SFSL6.0MDB	773-0060
6.5	+/-80	800	6.0	30	470	SFSL6.5MDB	773-0065

- The 3.58MHz frequency can be operated with 9.6Kbps and 19.2Kbps only

4.6 Oscillator

The ISL40 is designed to operate with a low cost 32.768KHz crystal connected between OscIn and OscOut pins. This type of crystal has the advantage of very low power consumption and low cost. However there are also drawbacks. It is very sensitive to noise and has a temperature dependency that should be carefully considered when selecting the crystal.

The following guidelines should be used when designing the PCB:

1. Design the trace length as short as possible.
2. Avoid thin line on resonator traces (< 0.010"), keep them as wide as possible.
3. To avoid noise, protect these signals with Ground shields.

The exact values of C1, C2, R1 and R2 should be determined according to the crystal manufacturer.

4.7 Recommended 32.768KHz Crystal Specifications

Type	Value
Nominal Frequency:	32.768KHz
Frequency tolerance @25ºC	+/-20 ppm
Load capacitance	12.5 pF
Serial resistance	50K Ohm (max.)
Drive level	1uW (max.)
Quality factor	50,000 (max.)
Turnover temperature	+25ºC +/- 5ºC
Parabolic constant	-0.04 ppm/ºC² (max.)
Aging	+/-3 ppm in first year (max.)
Operating temperature	-40ºC to + 85ºC
Storage temperature	-55ºC to + 125ºC

The overall frequency tolerance should not exceed 200ppm.

4.8 Communication performance

The maximal cable length between extreme devices depends mainly on the AC impedance of loads connected to that line and number of nodes. The DC cable length has less effect on communication. The SIG40 needs at least 20mVpp for proper reception. Good communication should be achieved if an oscilloscope at the SIG40 receiver can see the transmitted signal within the noise.

4.9 PLL Power Pins

VccPLL should be connected to Vcc. GndPLL should be connected to ground. The PLL supply has to be sufficiently powered, to avoid any fluctuations of power supply. A capacitor of at least 47uF should be connected as close as possible to these pins. It is recommended to keep the lines between 3.3V power supply and the Vcc pins as short as possible with wide PCB traces for Vcc, VccPLL, Gnd and GndPLL.

5 ELECTRICAL PARAMETERS

5.1 Absolute Maximal Rating

Ambient Temperature under bias	-40°C to 125°C
Storage Temperature	-65°C to 150°C
Voltage on any pin with respect to Vss (except Vdd and ~Reset)	-0.6V to Vdd+0.6V
Voltage on Vdd with respect to Vss	0 to +7.5V
Voltage on ~Reset pin with respect to Vss	0 to +14V
Total power Dissipation	1.0W
Maximum current out of Vss pin	300mA
Maximum current into Vdd pin	250mA
Maximum Output Current sunk by any I/O pin	25mA
Maximum Current source by any I/O pin	25mA

5.2 DC Characteristics

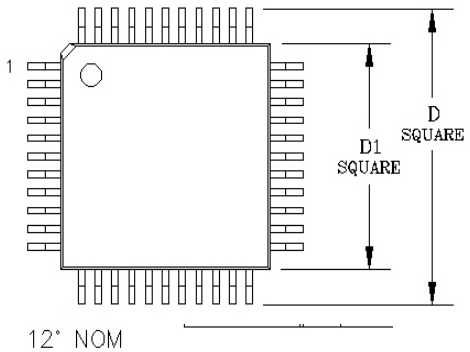
Symbol	Characteristics	Min	Typ	Max	Units	Conditions
Vdd	Supply Voltage	3.0	3.3	3.6	V	
Idd	Supply Current		35		mA	
Ipd	Power Down Current		70		uA	

5.3 Operating Temperature

Commercial: 0°C to 70°C

Industrial: -40°C to 85°C

5.4 Package - LQFP 48 pin



SYMBOL	LEADS / TOL.	48 LEAD
A	MAX.	1.60
A_1	MIN \ MAX	0.05 \ 0.15
A_2	MIN \ NOM \ MAX	1.35 \ 1.40 \ 1.45
D	BASIC	9.00
D_1	BASIC	7.00
L	±0.15	0.60
L1	REF	1.00
b	MIN \ MAX	0.17 \ 0.27
e	BASIC	0.50
ccc	MAX	0.08
ddd	NOM	0.08
JEDEC REF #		MS-026