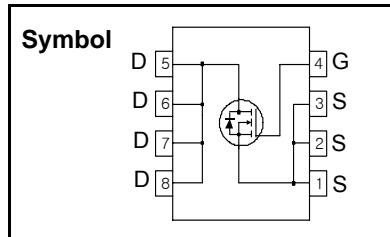


Logic N-Channel MOSFET

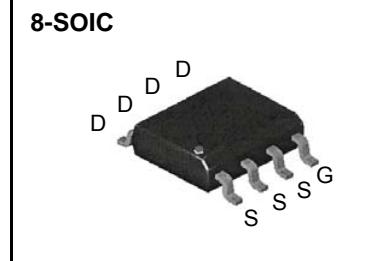
Features

- $R_{DS(on)}$ (Max 0.0135Ω)@ $V_{GS}=10V$
- $R_{DS(on)}$ (Max 0.020Ω)@ $V_{GS}=4.5V$
- Gate Charge (Typical 33nC)
- Maximum Junction Temperature Range (150°C)
- Available in Tape and Reel



General Description

This Power MOSFET is produced using Semiwell's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a low gate charge with superior switching performance, and rugged avalanche characteristics. This Power MOSFET is well suited for power management circuit or DC-DC converter.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain to Source Voltage	30	V
I_D	Continuous Drain Current(@ $T_A = 25^\circ C$)	10	A
I_{DM}	Drain Current Pulsed (Note 1)	50	A
V_{GS}	Gate to Source Voltage	± 20	V
P_D	Total Power Dissipation Single Operation ($T_A=25^\circ C$)	2.5	W
	Total Power Dissipation Single Operation ($T_A=70^\circ C$)	1.6	W
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	- 55 ~ 150	°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300	°C

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min.	Typ.	Max.	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 4)	-	-	50	°C/W

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Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C	-	12	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 55^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate-Source Leakage, Forward	$V_{GS} = 20\text{V}$, $V_{DS} = 0\text{V}$			100	nA
	Gate-Source Leakage, Reverse	$V_{GS} = -20\text{V}$, $V_{DS} = 0\text{V}$	-	-	-100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	1.0	-	-	V
$R_{DS(\text{ON})}$	Static Drain-Source On-state Resistance	$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 9\text{A}$	- -	0.011 0.016	0.0135 0.020	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 15\text{V}$, $f = 1\text{MHz}$	-	1100	-	pF
C_{oss}	Output Capacitance		-	550	-	
C_{rss}	Reverse Transfer Capacitance		-	150	-	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 25\text{V}$, $I_D = 1\text{A}$, $R_G = 50\Omega$ $V_{GS} = 10\text{V}$ (Note 2,3)	-	13	25	ns
t_r	Rise Time		-	30	60	
$t_{d(off)}$	Turn-off Delay Time		-	165	260	
t_f	Fall Time		-	65	120	
Q_g	Total Gate Charge	$V_{DS} = 15\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 10\text{A}$ (Note 2,3)	-	33	43	nC
Q_{gs}	Gate-Source Charge		-	5.2	-	
Q_{gd}	Gate-Drain Charge(Miller Charge)		-	8	-	

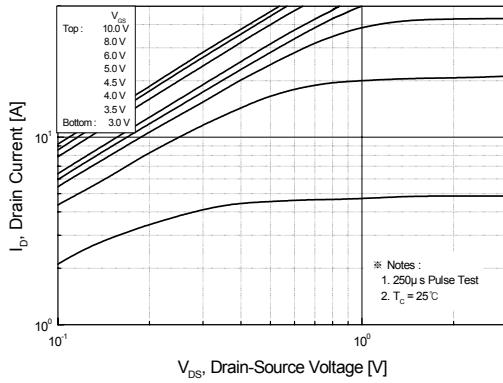
Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Diode Forward Current		-	-	2.1	A
V_{SD}	Diode Forward Voltage	$I_S = 2.1\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.2	V

* NOTES

1. Repeatability rating : pulse width limited by junction temperature
2. Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Essentially independent of operating temperature.
4. Surface mounted on 1 inch² Cu board.

Fig 1. On-State Characteristics



**Fig 3. On Resistance Variation vs.
Drain Current and Gate Voltage**

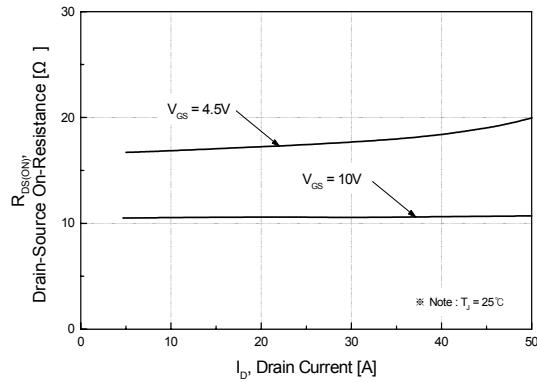


Fig 5. Capacitance Characteristics

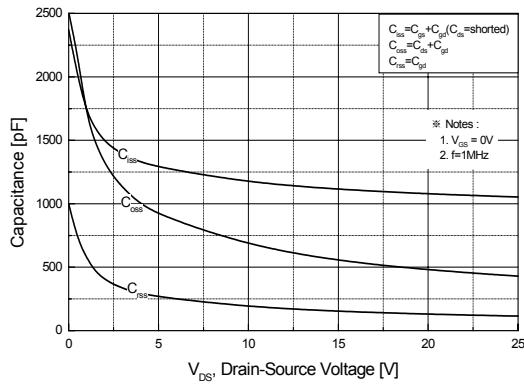
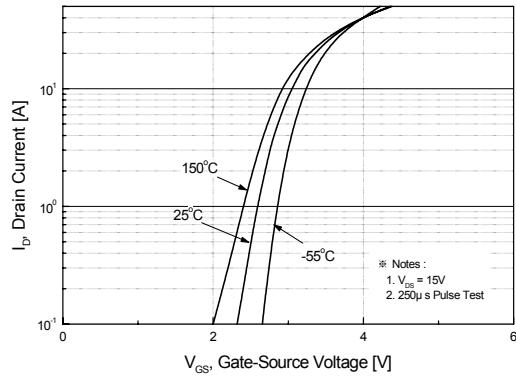


Fig 2. Transfer Characteristics



**Fig 4. On State Current vs.
Allowable Case Temperature**

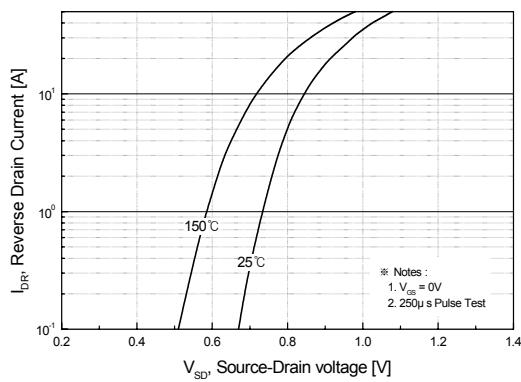
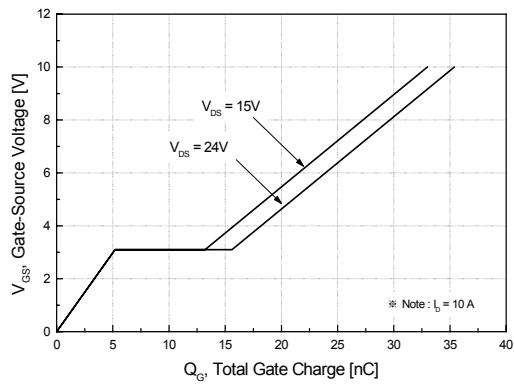


Fig 6. Gate Charge Characteristics



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Fig 7. Breakdown Voltage Variation vs. Junction Temperature

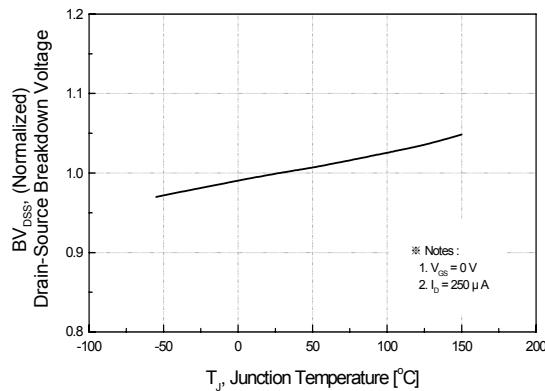


Fig 8. On-Resistance Variation vs. Junction Temperature

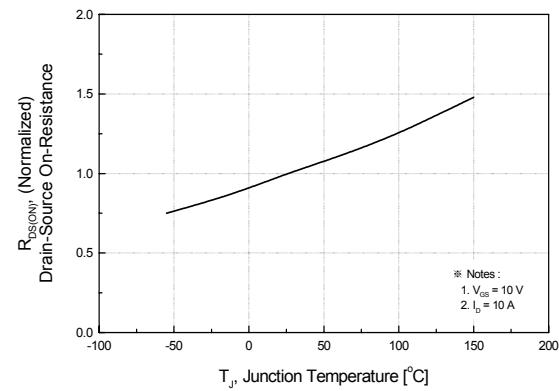


Fig 9. Normalized Transient Thermal Response Curve

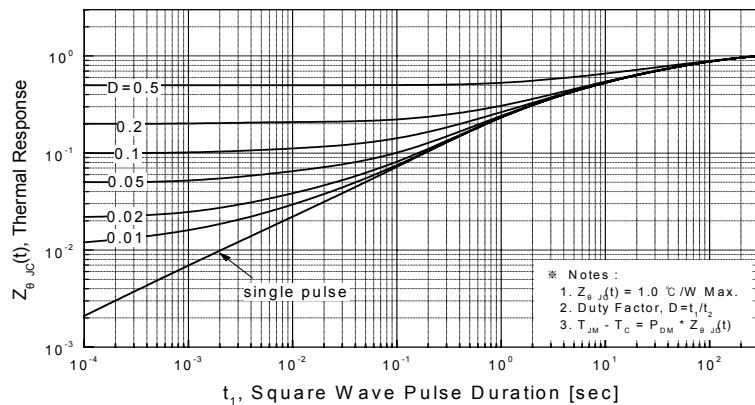


Fig. 10. Gate Charge Test Circuit & Waveforms

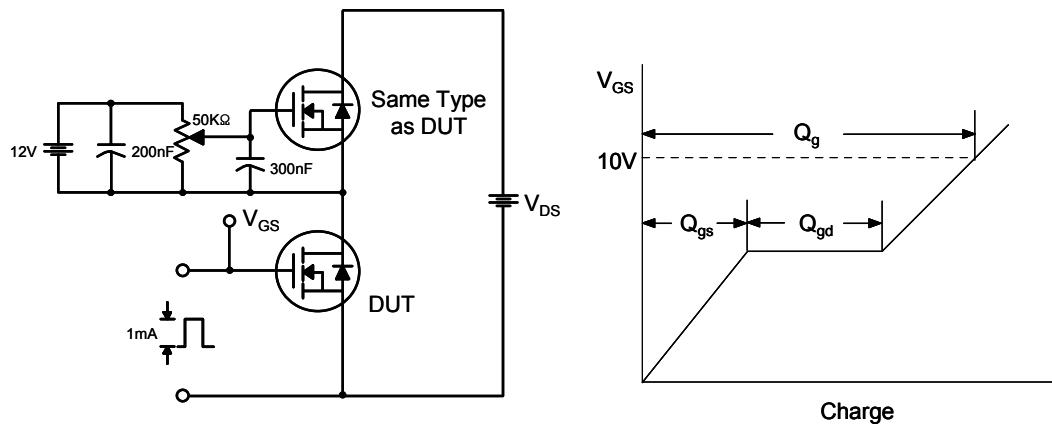
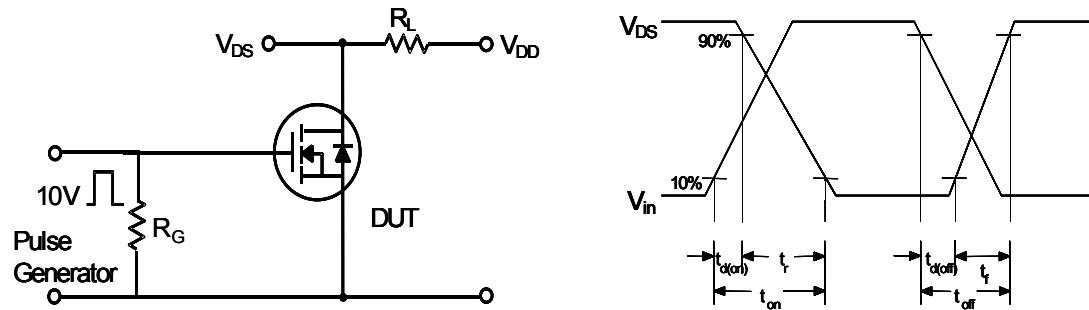


Fig 11. Switching Time Test Circuit & Waveforms



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8-SOIC Package Dimension

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35	1.55	1.75	0.053	0.061	0.069
B	0.1	0.175	0.25	0.004	0.007	0.010
C	0.38	0.445	0.510	0.015	0.018	0.020
D	0.19	0.22	0.25	0.007	0.009	0.010
E	4.8	4.9	5	0.189	0.193	0.197
F	3.8	3.9	4	0.150	0.154	0.157
G	1.27 BSC					
H	5.8	6	6.2	0.228	0.236	0.244
I	0.5	0.715	0.93	0.020	0.028	0.037
J	0'	4'	8'	0'	4'	8'
K	0.250	0.375	0.05	0.010	0.015	0.020

