MITEL
SEMICONDUCTOR

VP305/6

Satellite Channel Decoder

Preliminary Information

DM5009-1.0 09/07/98

TECHNICAL MANUAL

The VP305/6 is a decoder for digital satellite television transmissions to the European Broadcast Union ETS 300 421 specification (ref. 1). They receive digitised I and Q signals from the tuner, demodulate the QPSK data and provide a complete Forward Error Correction, (FEC) and de-scrambling function. The output is in the form of packetised MPEG2 transport stream data. The VP305/6 also provides automatic gain control and synchronising signals to the RF front end devices.

The VP305 has only a parallel interface port to the control microprocessor.

The VP306 has both a serial I^2C port and a parallel interface port to the control microprocessor.

MITEL CONFIDENTIAL INFORMATION

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PLEASE NOTE:

This manual has the following convention:

All numerical values are shown as decimal numbers, unless otherwise defined.

1. FUNCTIONAL DESCRIPTION.

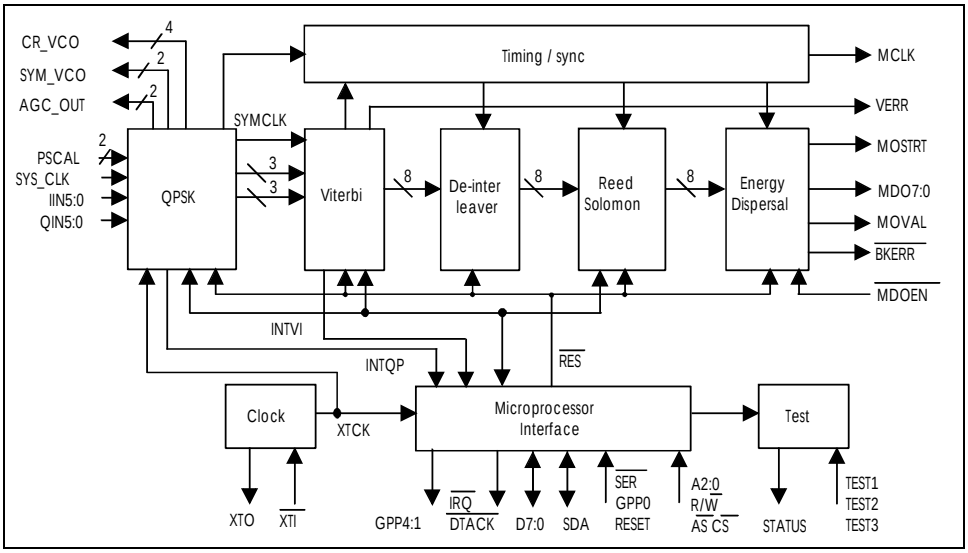


Fig. 1. VP305/6 Block Diagram.

1.1. System overview.

The VP305/6 decoder, together with the SL1710 I/Q down converter and the VP216/7 dual analog to digital converter (ADC) devices will provide a DVB compliant, satellite receiver system, see figure 2 on page 9. Before transmission, the data is processed using forward error correction techniques. Energy dispersal is added to even out 'ones' and 'zeros' for the power handling of the satellite output transmission devices. The VP305/6 device decodes the signal by reversing all these encoding techniques.

The VP305/6 contains three phase lock loop systems for control of the voltage controlled oscillators in the SL1710, the VP216/7 and an internal numerically controlled oscillator (NCO) in the VP305/6. The NCO can be set to provide a triangular wave form frequency search to establish symbol lock. There are also two AGC systems in the VP305/6, one controlling the SL1710 gain and a second internal AGC control of the output power levels from the QPSK block to the Viterbi block.

A crystal oscillator maintaining circuit is provided to sustain a stable frequency reference clock for the synthesiser loops. If a crystal is not used, the reference frequency signal may be input on the $\overline{\text{XTI}}$ pin.

A system clock (SYS_CLK) running at twice the symbol data rate is provided by the VCO on the VP216/7 ADC.

The dual ADC circuit digitises the In phase (I) and Quadrature phase (Q) analog signals providing two, six bit binary offset, data channels. The code range is, from 000000 = least positive valid output, to 111111 = most positive valid output.

These six bit data channels are input to the VP305/6 on the IIN and QIN pins to the QPSK demodulator block, see figure 2 on page 9. There the data is decimated and filtered to obtain the soft decision symbol data to pass to the Viterbi decoder. The QPSK block also generates a bit clock and resolves the $\pi/2$ demodulation phase ambiguity.

The Viterbi decoder recovers the data by a process of de-puncturing, probability analysis and bit error correction, to obtain the eight bit wide, data bit stream. It also rearranges the bit stream into bytes, providing a byte clock and packet start signal for the subsequent stages. An indication of the bit error rate in the data, is provided in the Viterbi block, by comparing the delayed input data bit stream with the decoded output data bit stream. An actual bit error count may be read from registers and a coarse indication of the number of errors is provided to facilitate satellite receiver dish alignment.

The data is then passed to the de-interleaver block where the data is reorganised in a series of FIFOs into the 204 byte blocks for the Reed Solomon decoder. The de-interleaver depth is 12.

The Reed Solomon decoder is able to correct up to eight byte errors found in the byte data stream. If there are too many errors to be corrected, the packet will be flagged as uncorrectable. The 16 check bytes are removed and the 188 byte packet is passed to the next block.

The final data processing block removes Energy Dispersion and inverts the inverted packet synchronisation byte which is used to mark every eighth 188 byte data packet.

The data output from the VP305/6 is in the form of MPEG2 transport stream data packets on the MDO7:0 data bus, together with clock, data start, data valid and block error signals. The data rate is automatically varied, according to the puncture rate, to reduce the instantaneous data rate and the inter packet period.

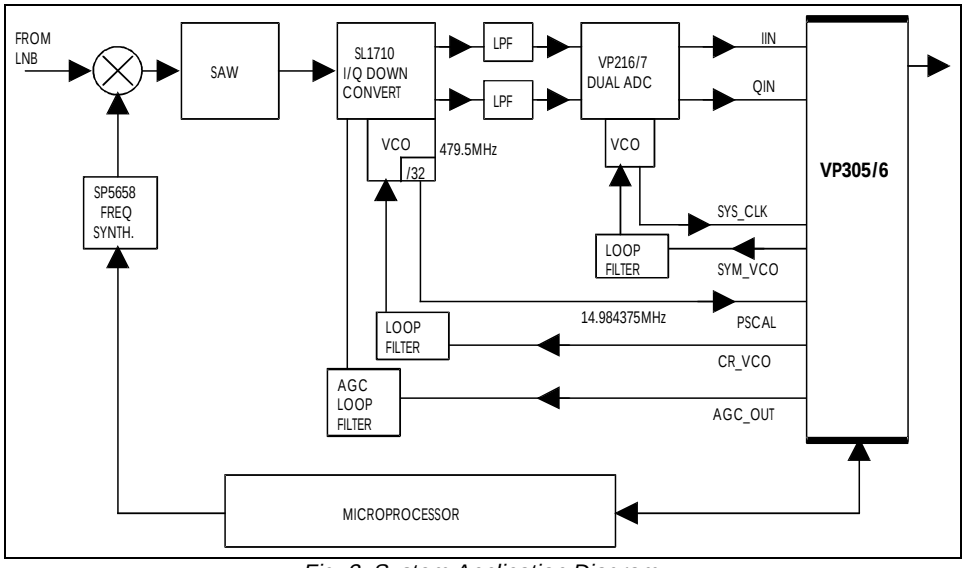


Fig. 2. System Application Diagram.

1.2. The QPSK Demodulator block.

The QPSK demodulator block performs the function of locking the receiver system to the incoming data stream. It controls the voltage controlled oscillators (VCO) in the SL1710 I/Q down converter and the VP216/7 dual analog to digital converter (ADC). The carrier frequency VCO is locked to maintain the intermediate frequency (IF) of 479.5MHz. The symbol frequency VCO synthesiser loop is locked to the twice the required symbol frequency (in the zero decimation case) and generates the system clock SYS_CLK which is running at the bit rate.

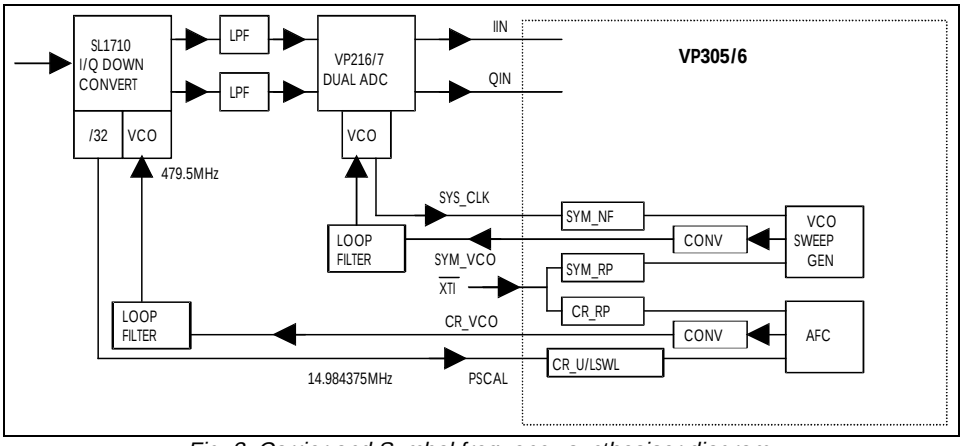


Fig. 3. Carrier and Symbol frequency synthesiser diagram.

1.2.1. Input requirements.

The data input is digitised six bit I and Q channel data in the form of either binary format or offset 2's complement data. The QPSK phase constellation representation is shown below.

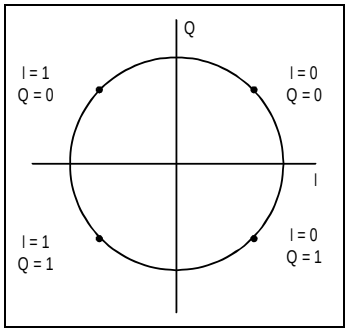


Fig. 4. QPSK constellation.

1.2.3. Matched filters

The Decimation filter and matched filter together have a 0.35 roll-off square-root-raised-cosine frequency response as in reference 1.

1.2.4. Decimation filters

In order to adjust to the wide range of symbol rates (5 to 30Msym/s), the I and Q data in may be decimated by varying degrees. The system also allows for the ADC sample clock to be adjusted to within the range 30 to 62MHz.

The sample rate at the input to the matched filter is equal to twice the symbol rate, 2Rs. The SYM_DR bits in the SYM_CONFIG register can be programmed to allow for the following filtered symbol rates at the input to the VP305/6:

2Rs, 3Rs, 4Rs, where Rs = symbol rate.

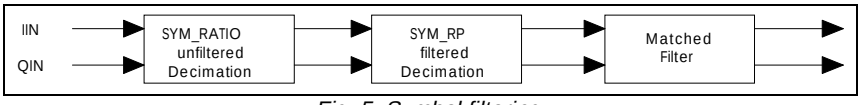


Fig. 5. Symbol filtering.

The SYM_RATIO register allows the input symbol rate to be extended further to cover 6Rs, 8Rs, 12Rs, 16Rs, 24Rs, 32Rs, 48Rs and 64Rs unfiltered decimation rates.

The number of samples / Symbol (M) can be calculated from the formula:

$$M = (\text{SYM\_DR over sample rate}) * (2^{\text{SYM\_RATIO}})$$

The range of values of M is shown in the table below.

SYM_RATIO	0	1	2	3	4
SYM_DR	M samples/Sym	M samples/Sym	M samples/Sym	M samples/Sym	M samples/Sym
0 - (over sample 2)	2	4	8	16	32
1 - (over sample 4)	4	8	16	32	64
2 - (over sample 3)	3	6	12	24	48

Table 1. Decimation ratios.

1.2.5. Carrier frequency synchronisation

The SL1710 local oscillator frequency of 479.5MHz is maintained by a frequency synthesis loop on the VP305/6. The SL1710 voltage controlled oscillator (VCO) frequency is divided internally by 32 to generate a push-pull feedback reference frequency signal. This is connected to the VP305/6 PSCAL PECL inputs and then to the CR_U/LSWL dividers. The output from the CR_U/LSWL dividers is compared with the crystal oscillator frequency divided by the CR_RP division ratio. A feedback signal (CR_VCO) is output to an active filter to complete the loop and control the SL1710 VCO, see Fig. 3 on page 9.

The internal frequency sweep generator is controlled by the CR_SWR, CR_USWL,CR_LSWL, CR_RP registers and turned on and off by the CR_SW bit in the CONFIG register. The diagram in Fig. 3 on page 9 shows the registers which set up the dividers for both the carrier and symbol phase locked loops.

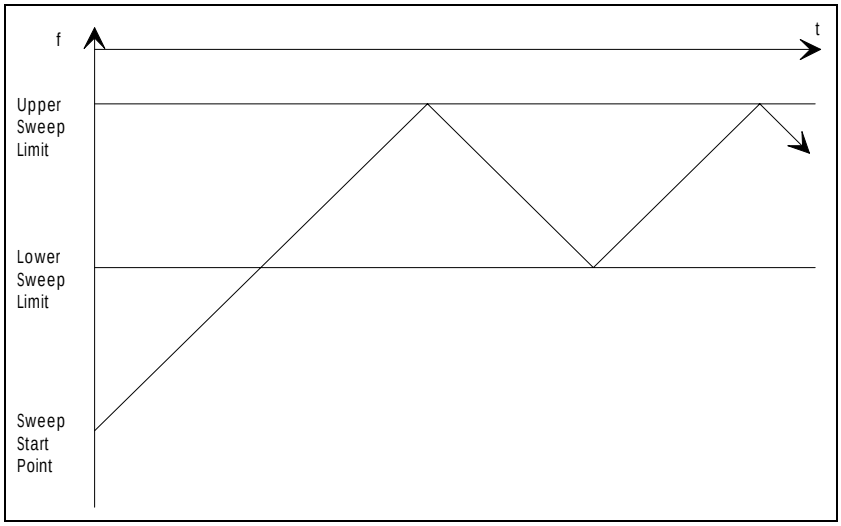


Fig. 6. Frequency sweep generator.

The carrier frequency reference period (CR_RP register) sets the count of the crystal clock cycles ($\overline{\text{XTI}}$ pin). This sets the reference for the measurement of the I/Q down converter VCO frequency (PSCAL pins). The register value sets the 4 most significant bits of a 14 bit counter. The actual count is CR_RP[3:0] * 1024.

The comparison frequency, $Fcomp = \frac{Fcrystal}{CR\_RP * 1024}$ MHz.

The upper and lower sweep boundaries are set by the CR_USWL and CR_LSWL respectively. These registers actually set the division ratios for dividing the I/Q down converter VCO frequency. The value programmed must take account of any fixed prescaler in the I/Q down converter, for the SL1710 this is divide by 32.

The comparison frequency, $Fcomp = \frac{Fvco}{32 * CR\_U/LSWL}$ MHz.

Therefore, $\frac{Fcrystal}{CR\_RP * 1024} = \frac{Fvco}{32 * CR\_U/LSWL}$

Therefore, $Fcrystal * 32 * CR\_U/LSWL = Fvco * CR\_RP * 1024$

Therefore, $\frac{Fvco}{Fcrystal} = \frac{32 * CR\_U/LSWL}{CR\_RP * 1024}$

The upper and lower sweep limits can be expressed in terms of the above equations together with two further terms including the delta variation in frequency.

Let the delta variation in frequency = ± δF.

Then the frequency limits are Fvco + δF and Fvco - δF.

Therefore, $CR\_USWL = \frac{(Fvco + \delta F) * CR\_RP * 1024}{Fcrystal * 32}$

and $CR\_LSWL = \frac{(Fvco - \delta F) * CR\_RP * 1024}{Fcrystal * 32}$

When the AFC circuit achieves lock, as indicated by the CR_FLOCK bit in the STATUS register going high, the scaled carrier frequency can be read from the CR_VCOF U & L registers.

The actual carrier frequency is found from the following formula:

$$Fvco = \frac{32 * Fcrystal}{CR\_RP * 1024} * CR\_VCOF \text{ MHz}$$

see page 30.

1.2.6. Symbol synchronisation and tracking

The VP216/7 local oscillator frequency must be programmed to be at least twice the required symbol rate and is maintained by a Phase Locked Loop on the VP305/6. The ADC sample frequency should be adjusted by setting the SYM_NF and SYM_RP division ratios to match the decimation rate chosen. The VP216/7 voltage controlled oscillator (VCO) frequency is connected to the VP305/6 SYS_CLK input and then to the SYM_NF divider. The output from the SYM_NF divider is compared with the crystal oscillator frequency divided by the SYM_RP division ratio. A push-pull feedback signal (SYM_VCO) is output to an active filter to complete the loop and control the VP216/7 VCO, see Fig. 3 on page 9.

1.3. The Viterbi Decoder block.

The Viterbi decoder input data format uses three bit, two's complement coding representation of the data in the following form, (binary numbers):

I or Q value	Interpretation
011	most likely one
010	
001	
000	least likely one
111	least likely zero
110	
101	
100	most likely zero

Table 2. Viterbi decoder input format.

The first task for the Viterbi decoder is to 'de-puncture' the data. This is a process of restoring data bits which have been removed (punctured), prior to transmission, to improve the transmission efficiency. The de-puncture code rate must be programmed into the VIT MODE register. The following patterns are used:

VITCR[2:0]	Code rate	Input bit stream	Output bit stream
0	1/2	$I = X_1$ $Q = Y_1$	X = 1 Y = 1
1	2/3	$I = X_1Y_2Y_3$ $Q = Y_1X_3Y_4$	X = 1010 Y = 1111
2	3/4	$I = X_1Y_2$ $Q = Y_1X_3$	X = 101 Y = 110
3	5/6	$I = X_1Y_2Y_4$ $Q = Y_1X_3X_5$	X = 10101 Y = 11010
4	7/8	$I = X_1Y_2Y_4Y_6$ $Q = Y_1Y_3X_5X_7$	X = 1000101 Y = 1111010

Table 3. Viterbi decoder code rate.

The zeros in the above table represent unknown data bit values, effectively error bits. The decoder uses a trace back trellis technique to remove the uncertainty and recover the correct data. The trace back depth is 128.

1.3.1. Viterbi error count measurement.

A measure of the effectiveness of the Viterbi decoder in removing bit errors is provided in the VP305/6. The incoming data bit stream is delayed and compared with the decoded bit stream to obtain a count of errors corrected by the decoder, see the Fig. 7 below.

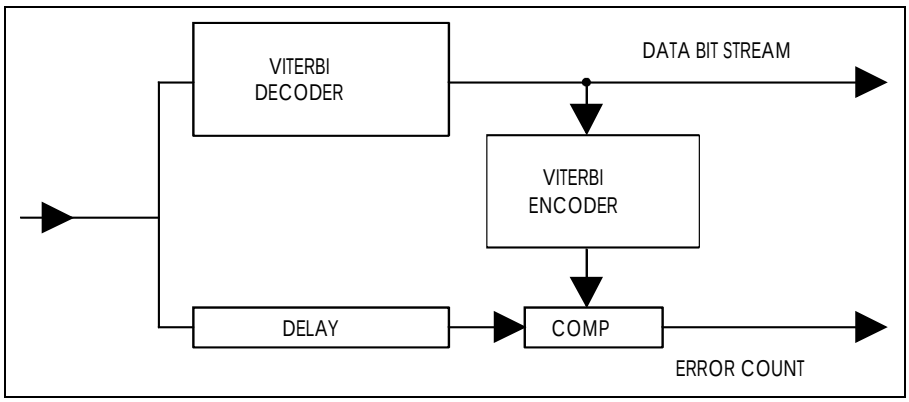


Fig. 7. Viterbi block diagram showing error count generation.

The measurement system has a programmable register to determine the number of data bits (the error count period) over which the count is being recorded. A read register indicates the error count result and an interrupt can be generated to inform the host microprocessor that a new count is available.

The VIT ERR H-M-L group of three registers is programmed with required number of data bits (the error count period) (VITEP[23:0]). The actual value is four times VITEP[23:0]. The count of errors found during this period is loaded by the VP305/6 into the VIT ERR C H-L pair of registers when the bit count VITEP[23:0] is reached. At the same time an interrupt is generated on the $\overline{\text{IRQ}}$ line. The actual error count value is four times VERRC[15:0]. If a value of 65535 is read out, the error count is too large for the VERRC[15:0] registers, so the error period in VITEP[23:0] should be reduced. The interrupt is enabled by setting the IE_FEC[2] bit in the IE_FEC register, see page 52. VERRC[15:0] is not cleared by reading the register, it is only loaded with the error count.

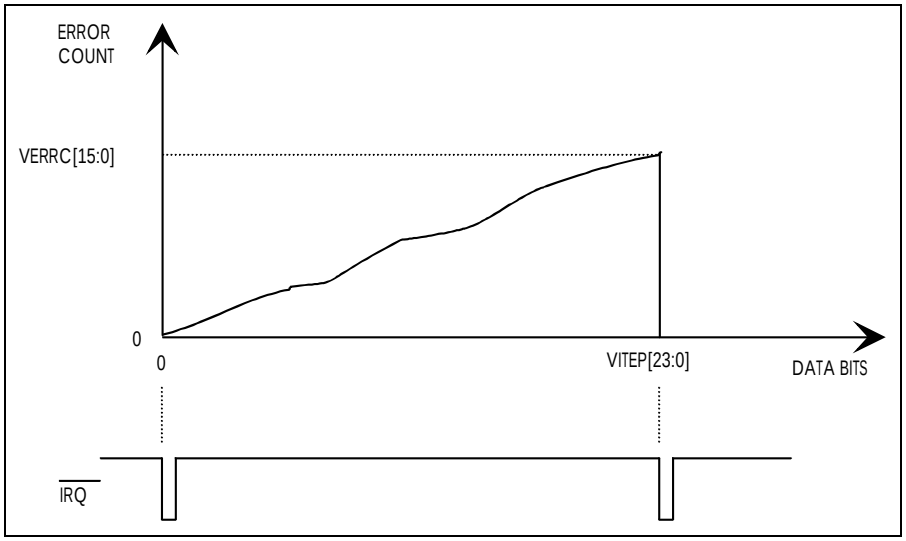


Fig. 8. Viterbi error count measurement.

Figure 8 above shows the bit errors rising until the maximum programmed value of VITEP[23:0] is reached, when an interrupt is generated on the $\overline{\text{IRQ}}$ line to advise the host microprocessor that a new value of bit error count has been loaded into the VERRC[15:0] register. The $\overline{\text{IRQ}}$ line will go high when the IE_FEC register is read by the host microprocessor.

The error count may be expressed as a ratio: $\frac{\text{VERRC[15:0]}}{\text{VITEP[23:0]}}$.

1.3.2. Viterbi error count coarse indication.

To assist in the process of aligning the receiver dish aerial, a coarse indication of the number of bit errors being received can be provided by monitoring the VERR line with the following set up conditions.

The frequency of the output wave form will be a function of the bit error count (triggering the maximum value programmed into the VI MAX ERR register (VMERR[7:0])) and the dish alignment on the satellite. This VERR mode is enabled by setting the INTVIS bit in the TEST2 register. Figure 9 below shows the bit errors rising to the maximum programmed value and triggering a change of state on the VERR line.

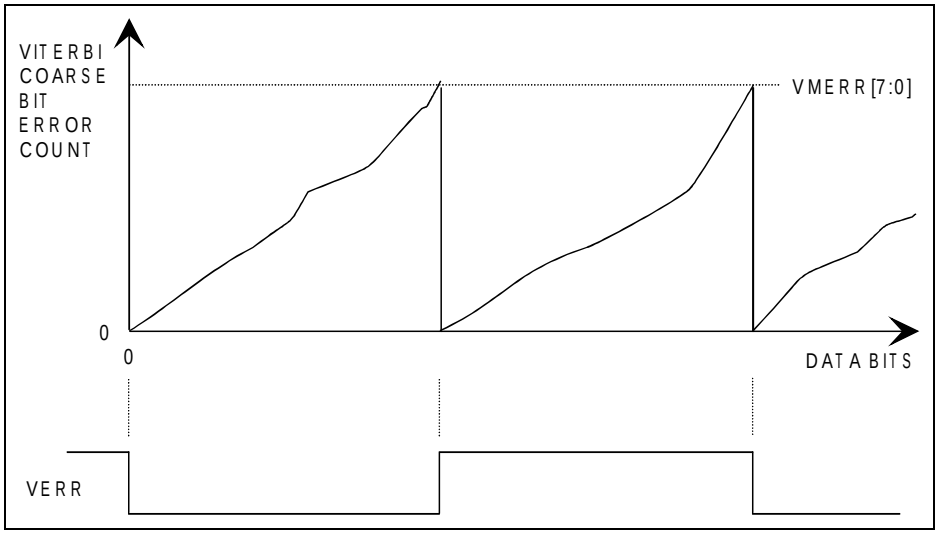


Fig. 9. Viterbi error count coarse indication.

1.4. The De-interleaver block.

Before transmission, the data bytes are interleaved with each other in a cyclic pattern of twelve. This ensures the bytes are spaced out, so that successive message bytes are transmitted with a separation of at least 12 bytes. This system is used to avoid the possibility of a noise spike corrupting a group of consecutive message bytes. The diagram below shows conceptually how the convolutional de-interleaving system works. The synchronisation byte is always loaded into the First-In-First-Out (FIFO) memory in branch 0. The switch is operated at regular byte intervals to write successively received bytes into the next branch. After 12 bytes have been received, byte 13 is written next to the synchronisation byte in branch 0, etc. Only when the FIFOs are full, will the read out of the 204 byte message be enabled. On the VP305/6, this function is realised in random access memory (RAM) with some spare capacity to avoid messages being over written before they are read out.

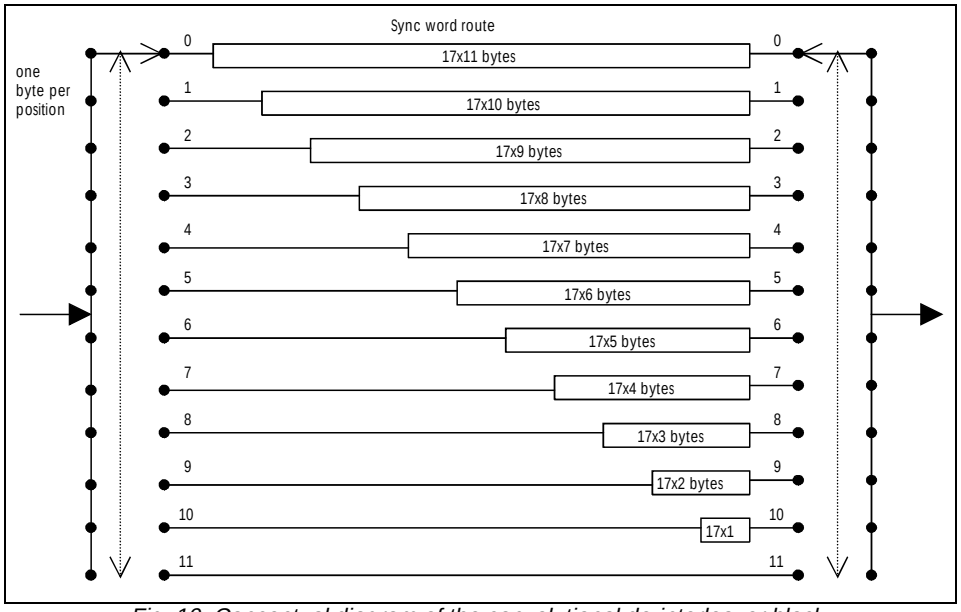


Fig. 10. Conceptual diagram of the convolutional de-interleaver block.

The byte sequence for the first 204 byte block is shown below. Each row represents one branch FIFO.

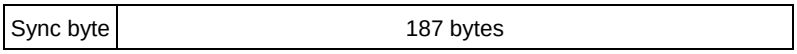
1	13	25	37	49	61	73	85	97	109	121	133	145	157	169	181	193
2	14	26	38	50	62	74	86	98	110	122	134	146	158	170	182	194
3	15	27	39	51	63	75	87	99	111	123	135	147	159	171	183	195
4	16	28	40	52	64	76	88	100	112	124	136	148	160	172	184	196
5	17	29	41	53	65	77	89	101	113	125	137	149	161	173	185	197
6	18	30	42	54	66	78	90	102	114	126	138	150	162	174	186	198
7	19	31	43	55	67	79	91	103	115	127	139	151	163	175	187	199
8	20	32	44	56	68	80	92	104	116	128	140	152	164	176	188	200
9	21	33	45	57	69	81	93	105	117	129	141	153	165	177	189	201
10	22	34	46	58	70	82	94	106	118	130	142	154	166	178	190	202
11	23	35	47	59	71	83	95	107	119	131	143	155	167	179	191	203
12	24	36	48	60	72	84	96	108	120	132	144	156	168	180	192	204

Table 4. De-interleaver data sequence.

1.5. The Reed Solomon block.

In the Transmission system, the MPEG2 message packet is encoded using the Reed Solomon RS(204,188, T=8) shortened code. This converts the 188 byte data packet into a Reed Solomon encoded block containing 204 bytes. The 16 check bytes allow the decoding system to search the packet for errors and correct up to eight bytes containing errors. If there are more than eight bytes containing errors, the packet is flagged as containing uncorrectable errors by pulling the $\overline{\text{BKERR}}$ pin low and setting the TEI bit in the second byte of the packet header, see figure 21 on page 68. The number of blocks containing uncorrectable errors may be read from the RS UBC register which is reset to zero each time it is read. The 16 check bytes are discarded before the data packet is passed on to the Energy Dispersal block.

Reed Solomon encoded block.



MPEG2 transport packet.

1.6. The Energy Dispersal (descrambler) block.

Before Reed Solomon encoding in the transmission system, the MPEG2 data stream is randomised using the configuration shown in figure 11 below. This is a Pseudo Random Binary Sequence (PRBS) generator, with the polynomial:

$$1 + X^{14} + X^{15}$$

The PRBS registers are loaded with the initialisation sequence as shown, at the start of the first transport packet in a group of eight packets. This point is indicated by the inverted sync byte B8hex. The normal sync. byte is 47hex. The data starting with the first byte after the sync. byte is randomised. (The sync. bytes themselves are not randomised).

In the decoder, the process of de-randomising or de scrambling the data is exactly the same as described above.

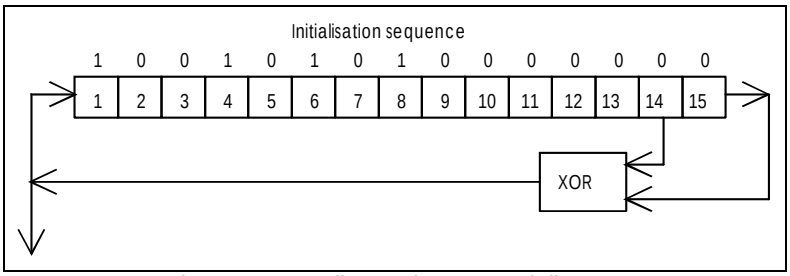


Fig. 11. Energy dispersal conceptual diagram.

1.6.1. Output stage.

A complete transport stream data packet of 188 bytes is output on the MDO7:0 bus, clocked by the MCLK signal. The MDO7:0 bus is enabled by pulling the $\overline{\text{MDOEN}}$ low. The start sync byte is flagged by the MOSTRT signal going high and the MOVAL signal will also go high to indicate a valid packet. If the packet contains uncorrectable bytes, a $\overline{\text{BKERR}}$ signal will go low on the first error byte and remain low until the end of the packet. The TEI bit in the packet header can optionally be set automatically to indicate a packet with uncorrectable bytes.

1.7. Microprocessor interface.

This interface can be either a serial I²C bus or a parallel interface port, see section 3 starting on page 58.

2. REGISTER DETAILS

2.1. Parallel interface register map.

The default state of almost all of the registers is zero, except the ID register and unused registers. Reserved or unused bits should be set to zero when writing to a register.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
BANK	0	Reserved		AD5	AD4	AD3	Reserved			W

Table 5a. BANK Register 0. (Address byte = 0, Data byte = NEXT BANK)

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
INT_QPSK	1	INT_QPSK[7:0] Interrupt QPSK								R
INT_FEC	2	INT_FEC[7:0] Interrupt FEC								R
STATUS	3	Reserved	STATUS[6:0]							R
AGC_LVL	4	AGC_LVL[7:0] AGC loop voltage meter								R
CR_VCOF U	5	Reserved		CR_VCOF[13:8] Measured VCO frequency (upper nibble)						R
CR_VCOF L	6	CR_VCOF[7:0] Measured VCO frequency (lower byte)								R
IE_QPSK	7	IE_QPSK[7:0] Interrupt enable QPSK								R/W

Table 5b. Register bank 0. BANK[5:3] = 0.

Note: In Bank 0, the registers 1 to 6 are READ only. Writing to these addresses will have no effect.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
SYM_CONFIG	1	Reserved		SYM_CONFIG[5:0] Symbol configuration						R/W
SYM_RP	2	Reserved				SYM_RP[3:0] Symbol AFC reference period				R/W
SYM_NF U	3	SYM_NF[15:8] Symbol input nominal frequency (upper byte)								R/W
SYM_NF L	4	SYM_NF[7:0] Symbol input nominal frequency (lower byte)								R/W
SYM_RATIO	5	Reserved					SYM_RATIO[2:0]			R/W
AGC_REF	6	AGC_REF[7:0] Reference AGC level								R/W
AGC_BW	7	Reserved				INT_DC	AGC_BW[2:0]			R/W

Table 5c. Register bank 1. BANK[5:3] = 8.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
SCALE	1	SCALE[7:0] Scale factor for IOUT and QOUT outputs								R/W
SNR_THS	2	SNR_THS[7:0] SNR estimator threshold								R/W
CR_OFFSET	3	CR_OFFSET[7:0] Carrier loop DC offset compensation value								R/W
CR_RP	4	Reserved				CR_RP[3:0] Carrier reference period				R/W
CR_KP	5	CR_KP[7:0] Carrier loop filter gain (P term)								R/W
CR_KD	6	CR_KD[7:0] Carrier loop filter gain (D term)								R/W
CR_THSL	7	CR_THSL[7:0] Carrier lock detector threshold								R/W

Table 5d Register bank 2. BANK[5:3] = 16.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
CR_SWR	1	CR_SWR[7:0] Carrier sweep rate								R/W
CR_USWL U	2	Reserved		CR_USWL[13:8] Carrier Upper sweep limit (upper nibble)						R/W
CR_USWL L	3	CR_USWL[7:0] Carrier Upper sweep limit (lower byte)								R/W
CR_LSWL U	4	Reserved		CR_LSWL[13:8] Carrier Lower sweep limit (upper nibble)						R/W
CR_LSWL L	5	CR_LSWL[7:0] Carrier Lower sweep limit (lower byte)								R/W
CR_CONFIG	6	CR_CONFIG[7:0] Carrier configuration								R/W
CONFIG	7	CONFIG[7:0] Configuration								R/W

Table 5e. Register bank 3. BANK[5:3] = 24.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
VIT_ERR_C H	1	VERRC[15:8] - Viterbi error count high byte								R
VIT_ERR_C L	2	VERRC[7:0] - Viterbi error count low byte								R
RS_UBC	3	RSUBC[7:0] - Reed Solomon uncorrected block count								R
Not used	4 - 7	Writing to these addresses will have no effect. Reading will return 255								R/W

Table 5f. Register bank 4. BANK[5:3] = 32.

Note: In Bank 4, the registers 1 to 3 are READ only and registers 4 to 7 are not used. Writing to these addresses will have no effect.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
VIT_MODE	1	IQSWAP	F_LOCK	Reserved			VITCR[2:0] - code rate			R/W
VIT_ERR H	2	VITEP[23:16] - Viterbi error period high byte								R/W
VIT_ERR M	3	VITEP[15:8] - Viterbi error period middle byte								R/W
VIT_ERR L	4	VITEP[7:0] - Viterbi error period low byte								R/W
VI_MAX_ERR	5	VMERR[7:0] - Viterbi max. bit error count								R/W
VI_BER_PER	6	VBPER[7:0] - Viterbi bit error rate based synchronisation period								R/W
VI_BER_LIM	7	VBLIM[7:0] - Viterbi bit error rate based synchronisation limit								R/W

Table 5g. Register bank 5. BANK[5:3] = 40.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
VIT_CTRL1	1	BS_MODE[1:0]		VS_UNLK[3:0]				VBIT_MV[1:0]		R/W
VIT_CTRL2	2	Reserved					VS_LK[2:0]			R/W
IE_FEC	3	IE_FEC[7:0] Interrupt enable FEC								R/W
STAT_EN	4	STAT_EN[7:0] Enable various outputs on STATUS pin.								R/W
GEN_CTRL	5	-	-	-	MCLKINV	BSO	ENTEI	NSYNC[1:0]		R/W
GPP_CTRL	6	Reserved			GPP_CTRL[4:0]					R/W
RESET	7	RES	-	-	-	PR_DS	PR_BS	FR_QP	PR_QP	R/W

Table 5h. Register bank 6. BANK[5:3] = 48.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	0	ID[7:0] Chip identification								R
TEST1	1	Reserved								R/W
TEST2	2	INTVIS	-	-	-	EN[3:0]				R/W
TEST3	3	Reserved								R/W
Not used	4 - 7	Writing to these addresses will have no effect. Reading will return 255								R/W

Table 5i. Register bank 7. BANK[5:3] = 56.

Note: In Bank 7, the registers 4 - 7 are not used. Writing to these addresses will have no effect.

Note: When writing to, or reading from registers which are part of a group, all registers in the group must be addressed for the data transfer to be sucessfully completed.

2.2. Serial interface register map.

Not available on VP305.
The default state of all registers is reset to 0.
Reserved or unused bits should be set to zero when writing to a register.
All values are shown as decimal numbers, unless otherwise defined.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
RADD		IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W
ID	00	ID[7:0] Chip identification. Writing to this address will have no effect.								R
INT_QPSK	01	INT_QPSK[7:0] Interrupt QPSK								R
INT_FEC	02	INT_FEC[7:0] Interrupt FEC								R
STATUS	03	Reserved	STATUS[6:0]							R
AGC_LVL	04	AGC_LVL[7:0] AGC loop voltage meter								R
CR_VCOF U	05	Reserved		CR_VCOF[13:8] Measured VCO frequency (upper nibble)						R
CR_VCOF L	06	CR_VCOF[7:0] Measured VCO frequency (lower byte)								R
Not used	01-06	Writing to these addresses will have no effect.								W
IE_QPSK	07	IE_QPSK[7:0] Interrupt enable QPSK								R/W
ID	08	ID[7:0] Chip identification. Writing to this address will have no effect.								R
SYM_CONFIG	09	Reserved		SYM_CONFIG[5:0] Symbol configuration						R/W
SYM_RP	10	Reserved				SYM_RP[3:0] Symbol AFC ref. period				R/W
SYM_NF U	11	SYM_NF[15:8] Symbol input nominal frequency (upper byte)								R/W
SYM_NF L	12	SYM_NF[7:0] Symbol input nominal frequency (lower byte)								R/W
SYM_RATIO	13	Reserved					SYM_RATIO[2:0]			R/W
AGC_REF	14	AGC_REF[7:0] Reference AGC level								R/W
AGC_BW	15	Reserved				INT_DC	AGC_BW[2:0]			R/W
ID	16	ID[7:0] Chip identification. Writing to this address will have no effect.								R
SCALE	17	SCALE[7:0] Scale factor for IOUT and QOUT outputs								R/W
SNR_THS	18	SNR_THS[7:0] SNR estimator threshold								R/W
CR_OFFSET	19	CR_OFFSET[7:0] Carrier loop DC offset compensation value								R/W
CR_RP	20	Reserved				CR_RP[3:0] Carrier reference period				R/W
CR_KP	21	CR_KP[7:0] Carrier loop filter gain (P term)								R/W
CR_KD	22	CR_KD[7:0] Carrier loop filter gain (D term)								R/W
CR_THSL	23	CR_THSL[7:0] Carrier lock detector threshold								R/W
ID	24	ID[7:0] Chip identification. Writing to this address will have no effect.								R
CR_SWR	25	CR_SWR[7:0] Carrier sweep rate								R/W
CR_USWL U	26	Reserved		CR_USWL[13:8] Carrier Upper sweep limit (upper nibble)						R/W
CR_USWL L	27	CR_USWL[7:0] Carrier Upper sweep limit (lower byte)								R/W
CR_LSWL U	28	Reserved		CR_LSWL[13:8] Carrier Lower sweep limit (upper nibble)						R/W
CR_LSWL L	29	CR_LSWL[7:0] Carrier Lower sweep limit (lower byte)								R/W
CR_CONFIG	30	CR_CONFIG[7:0] Carrier configuration								R/W
CONFIG	31	CONFIG[7:0] Configuration								R/W

Table 6a. QPSK Register details.

NAME	ADR	D7	D6	D5	D4	D3	D2	D1	D0	R/W
ID	32	ID[7:0] Chip identification. Writing to this address will have no effect.								R
VIT_ERR_C H	33	VERRC[15:8] - Viterbi error count high byte								R
VIT_ERR_C L	34	VERRC[7:0] - Viterbi error count low byte								R
RS_UBC	35	RSUBC[7:0] - Reed Solomon uncorrected block count								R
Not used	33-35	Writing to these addresses will have no effect.								W
Not used	36-39	Writing to these addresses will have no effect. Reading will return 255								R/W
ID	40	ID[7:0] Chip identification. Writing to this address will have no effect.								R
VIT_MODE	41	IQSWAP	F_LOCK	Reserved			VITCR[2:0] - code rate			R/W
VIT_ERR H	42	VITEP[23:16] - Viterbi error period high byte								R/W
VIT_ERR M	43	VITEP[15:8] - Viterbi error period middle byte								R/W
VIT_ERR L	44	VITEP[7:0] - Viterbi error period low byte								R/W
VI_MAX_ERR	45	VMERR[7:0] - Viterbi max. bit error count								R/W
VI_BER_PER	46	VBPER[7:0] - Viterbi bit error rate based synchronisation period								R/W
VI_BER_LIM	47	VBLIM[7:0] - Viterbi bit error rate based synchronisation limit								R/W
ID	48	ID[7:0] Chip identification. Writing to this address will have no effect.								R
VIT_CTRL1	49	BS_MODE[1:0]		VS_UNLK[3:0]				VBIT_MV[1:0]		R/W
VIT_CTRL2	50	Reserved					VS_LK[2:0]			R/W
IE_FEC	51	IE_FEC[7:0] Interrupt enable FEC								R/W
STAT_EN	52	STAT_EN[7:0] Enable various outputs on STATUS pin.								R/W
GEN_CTRL	53	-	-	-	MCLKINV	BSO	ENTEI	NSYNC[1:0]		R/W
GPP_CTRL	54	Reserved			GPP_CTRL[4:0]					R/W
RESET	55	RES	-	-	-	PR_DS	PR_BS	FR_QP	PR_QP	R/W
ID	56	ID[7:0] Chip identification. Writing to this address will have no effect.								R
TEST1	57	Reserved								R/W
TEST2	58	INTVIS	-	-	-	EN[3:0]				R/W
TEST3	59	Reserved								R/W
Not used	60-63	Writing to these addresses will have no effect. Reading will return 255								R/W

Table 6b. FEC Register details.

Note: When writing to, or reading from registers which are part of a group, all registers in the group must be addressed for the data transfer to be sucessfully completed.

2.3. BANK: Register bank address - Parallel mode only.

Registers are directly addressed via the address bus in banks of seven. In the BANK register 0, the bits AD5, AD4 and AD3 are used to select the active register bank to be used until changed by writing to the BANK register. For examples of use, see page 60.

Parallel mode - Bank 0. Address 0. Type Write.
Serial mode - see RADD / ID registers on pages 26 and 27.

7	6	5	4	3	2	1	0	R/W
Reserved		AD5	AD4	AD3	Reserved			W

AD[2:0] Reserved - not used. If these bits are written they are ignored by the VP305/6. This allows the microprocessor to write the BANK address with the serial mode register address.

AD[5:3] Bank address These are the active bits in the register. See table 7 below for details.

BANK[5:0] decimal	AD5	AD4	AD3	Bank	Function
0 - 7	0	0	0	0	Monitor interrupts and QPSK registers
8 - 15	0	0	1	1	Program QPSK registers
16 - 23	0	1	0	2	Program QPSK registers
24 - 31	0	1	1	3	Program QPSK registers
32 - 39	1	0	0	4	Monitor FEC registers
40 - 47	1	0	1	5	Program FEC registers
48 - 55	1	1	0	6	Program FEC and general registers
56 - 59	1	1	1	7	Program test registers

Table 7. BANK address decodes for parallel mode.

The register address in parallel mode may be calculated from the serial mode register address as follows:

Parallel address = serial address (mod 8) where mod = modulus

Example CR_CONFIG register: serial address =30, parallel = Bank 3 address 6

Bank address = 30 (serial address)

Alternatively, the bit value is:

BANK[5:3] = (30 - (30 mod 8))
= (30 - 6)
= 24 This equates to Bank 3, see table 7 above.)

Parallel Address = 30 mod 8
= 6.

2.4. RADD: I²C Register address - Serial mode only.

Not available on VP305.

RADD is the I²C register address. It is the first byte written after the VP306 I²C chip address when in write mode.

To write to the chip, the microprocessor should send a START condition and the chip address with the write bit set, followed by the register address where subsequent data bytes are to be written. Finally, when all the 'message' has been sent, a STOP condition is sent to free the bus.

To read from the chip from register address one, the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of SCL clocks to read the bytes out. Finally a STOP condition is sent to free the bus. RADD is not sent in this case.

To read from the chip from an address other than one, the microprocessor should send the chip address with the write bit set, followed by the register address where subsequent data bytes are to be read from. Then the microprocessor should send a START condition and the chip address with the read bit set, followed by the requisite number of SCL clocks to read the bytes out. Finally a STOP condition is sent to free the bus. This case should also be used to read the chip identification number in register zero.

A STOP condition shall reset the RADD value to 01. For examples of use, see page 59.

Serial mode - Address none. Type Write.

7	6	5	4	3	2	1	0	R/W
IAI	AD6	AD5	AD4	AD3	AD2	AD1	AD0	W

AD[6:0] I²C register address, numbers in the range 0 to 63 are allowed. AD6 should be set to zero.

IAI High = Inhibit auto increment.
Low = Increment addresses.
The IAI bit and function is only available via the I²C port. When the address is incremented to 63 it stops and the bus will continue to write to or read from 'register' 63 until a STOP condition is sent. Since 'register' 63 does not exist, data writen to it is lost or it will read back 255.

2.5. BANK 0: Monitor QPSK read registers.

2.5.1. ID: Identification register.

Parallel mode - Bank 0-7. Address 0.Type Read.
Serial mode - Addresses 00, 08, 16, 24, 32, 40, 48, 56.

7	6	5	4	3	2	1	0	R/W
ID[7:0] Chip identification								R

ID[7:0] Identification: 0 = VP305/6 version.

2.5.2. INT_QPSK: Interrupt for QPSK block, register.

These bits indicate the QPSK block event causing the interrupt signalled by the $\overline{IRQ}$ line going low. The $\overline{IRQ}$ line is reset high and the register is reset to zero when the INT_QPSK register is read. The events can be masked from activating both the INT_QPSK register bit and the $\overline{IRQ}$ line by setting the appropriate event masking bit LOW in the IE_QPSK (interrupt enable) register, see page 31. All bits in the IE_QPSK register should be set high.

Parallel mode - Bank 0. Address 1. Type Read.
Serial mode - Address 01.

7	6	5	4	3	2	1	0
INT_QPSK[7:0]							

INT_QPSK[0] High = Symbol AFC lock is detected. This means that the number of clock VCO cycles measured during the reference period set by SYM_RP register is in the range SYM_NF (register) ±2 range.

INT_QPSK[1] High = Symbol AFC lock is lost.

INT_QPSK[2] High = Carrier Phase lock is detected.

INT_QPSK[3] High = Carrier Phase lock is lost.

INT_QPSK[4] High = Carrier Frequency lock is detected.

INT_QPSK[5] High = Carrier Frequency lock is lost.

INT_QPSK[6] High = Frequency sweep has reached its lower limit.

INT_QPSK[7] High = Frequency sweep has reached its upper limit.

2.5.3. INT_FEC: Interrupt FEC register.

These bits indicate the FEC block event causing the interrupt signalled by the $\overline{IRQ}$ line going low. The $\overline{IRQ}$ line is reset high and the register is reset to zero when it is read. The events can be masked from activating the $\overline{IRQ}$ line by setting the appropriate event masking bit in the IE_FEC (interrupt enable) FEC register, see page 52. The masking of events does not affect the setting of the bits in the INT_FEC register.

Parallel mode - Bank 0. Address 2. Type Read.
Serial mode - Address 02.

7	6	5	4	3	2	1	0
INT_FEC[7:0]							

INT_FEC[0] High = Descrambler lock established.

INT_FEC[1] High = Descrambler lock is lost.

INT_FEC[2] High = Viterbi error monitor period has reached the value programmed in the VMERR[7:0] register.

INT_FEC[3] Reserved.

INT_FEC[4] High = Viterbi bit lock established.

INT_FEC[5] High = Viterbi bit lock is lost.

INT_FEC[6] High = Frame alignment lock established. (A Frame is 8 blocks, each block is 204 bytes).

INT_FEC[7] High = Frame alignment lock is lost.

2.5.4. STATUS: Status register.

Parallel mode - Bank 0. Addresses 3. Type Read.
Serial mode - Address 03.

7	6	5	4	3	2	1	0
Reserved	STATUS[6:0]						

The register is NOT reset to zero when it is read. Each of these indicators can be output on the STATUS pin by enabling the appropriate bit in the STAT_EN register, see page 53.

STATUS[0] High = SYM_LCF, Symbol AFC within pull-in range.
Low = SYM_LCF, Symbol AFC not within pull-in range.

STATUS[1] High = CR_LC, carrier loop in lock.
Low = CR_LC, carrier loop out of lock.

STATUS[2] High = CR_LCF, carrier frequency detector in lock.
Low = CR_LCF, carrier frequency detector out of lock.

STATUS[3] High = good SNR.
Low = bad SNR.

STATUS[4] High = Descrambler lock detector in lock.
Low = Descrambler lock detector out of lock.

STATUS[5] High = Viterbi bit lock detector in lock.
Low = Viterbi bit lock detector out of lock.

STATUS[6] High = Frame align detector in lock.
Low = Frame align detector out of lock.

2.5.5. AGC_LVL: AGC loop voltage meter register.

Parallel mode - Bank 0. Address 4. Type Read.
Serial mode - Address 04.

7	6	5	4	3	2	1	0
AGC_LVL[7:0] AGC loop voltage meter							

AGC_LVL[7:0] AGC loop voltage meter. The register is NOT reset to zero when it is read.

The relationship between the loop voltage Vagc and the AGC_LVL register is:

Vagc = AGC_LVL * Vref / 256

The AGC_OUT pin has an open drain buffer allowing an external Vref of up to 5 volts to be used.

2.5.6. CR_VCOF U & L: Measured VCO frequency registers.

Parallel mode - Bank 0. Addresses 5, 6. Type Read.
Serial mode - Addresses 05, 06.

7	6	5	4	3	2	1	0
Reserved		CR_VCOF[13:8] Measured VCO frequency (upper nibble)					
CR_VCOF[7:0] Measured VCO frequency (lower byte)							

These two bytes together form the 14 bit number: CR_VCOF[13:0] Measured carrier VCO frequency. The register is NOT reset to zero when it is read.

The actual carrier frequency is found from the following formula:

$$Fvco = \frac{32 * Fcrystal}{CR\_RP * 1024} * CR\_VCOF$$

The incremental carrier step frequency is found by putting the value of CR_VCOF = 1 in the equation:

$$\delta Fvco = \frac{32 * Fcrystal}{CR\_RP * 1024} * 1$$

See page 12 for further discussion.

2.5.7. IE_QPSK: Interrupt enable QPSK register.

When the bits of this register are set high, they enable an event to be signalled in the INT_QPSK register to generate an interrupt on the $\overline{IRQ}$ pin. All bits should be set high, see page 27.

Parallel mode - Bank 0. Address 7. Type Read / Write.
Serial mode - Address 07.

7	6	5	4	3	2	1	0
IE_QPSK[7:0] Interrupt enable QPSK							

IE_QPSK[7:0] Interrupt enable QPSK.

When : IE_QPSK[i] =1 : enable INT_QPSK[i]
IE_QPSK[i] =0 : disable INT_QPSK[i] (default state)

where i = 0 to 7.

IE_QPSK[0] High = Enable Symbol AFC lock detected indication in INT_QPSK register.

IE_QPSK[1] High = Enable Symbol AFC lock lost indication in INT_QPSK register.

IE_QPSK[2] High = Enable Carrier Phase lock detected indication in INT_QPSK register.

IE_QPSK[3] High = Enable Carrier Phase lock lost indication in INT_QPSK register.

IE_QPSK[4] High = Enable Carrier Frequency lock detected indication in INT_QPSK register.

IE_QPSK[5] High = Enable Carrier Frequency lock lost indication in INT_QPSK register

IE_QPSK[6] High = Enable Frequency sweep has reached its lower limit indication in INT_QPSK register.

IE_QPSK[7] High = Enable Frequency sweep has reached its upper limit indication in INT_QPSK register.

2.6. BANK 1: Program QPSK registers.

2.6.1. SYM_CONFIG: Symbol configuration register.

Parallel mode - Bank 1. Address 1. Type Read / Write.
Serial mode - Address 09.

7	6	5	4	3	2	1	0
Reserved		SYM_CONFIG[5:0] Symbol configuration					

SYM_CONFIG[1:0] SYM_DR[1:0] Filtered decimation ratio select.
00 = no decimation (over sampling ratio = 2)
01 = decimation by 1/2 (over sampling ratio = 4)
10 = decimation by 2/3 (over sampling ratio = 3)
See also SYM_RATIO: Input decimation factor register, page 34.

SYM_CONFIG[2] SYM_VCO _SWAP
High = swap U and D output polarity, pins 96 and 97.
Low = normal

SYM_CONFIG[3] SYM_LCF _SUPP
High = suppress timing error detector.
Low = normal

SYM_CONFIG[4] SYM_VCO U/D
High = tri-state D and U outputs.
Low = active outputs.

SYM_CONFIG[5] Reserved set low.

SYM_CONFIG[6] Reserved set low.

SYM_CONFIG[7] Reserved set low.

2.6.2. SYM_RP: Symbol AFC reference period register.

Parallel mode - Bank 1. Address 2. Type Read / Write.
Serial mode - Address 10.

7	6	5	4	3	2	1	0
Reserved				SYM_RP[3:0] Symbol AFC reference period			

SYM_RP[3:0] Symbol frequency reference period for the count of the crystal clock cycles ($\overline{\text{XTI}}$ pin). This sets the reference for the measurement of the ADC VCO frequency (SYS_CLK pin). The register value sets the 4 most significant bits of a 14 bit counter. The actual count is SYM_RP[3:0] * 1024.

2.6.3. SYM_NF U & L: Symbol input nominal frequency registers.

Parallel mode - Bank 1. Addresses 3, 4. Type Read / Write.
Serial mode - Addresses 11, 12.

7	6	5	4	3	2	1	0
SYM_NF[15:8] Symbol input nominal frequency (upper byte)							
SYM_NF[7:0] Symbol input nominal frequency (lower byte)							

These two bytes together form the 16 bit number: SYM_NF[15:0] Symbol input nominal frequency. This is the division ratio for the Symbol clock input from the ADC VCO.

2.6.4. SYM_RATIO: Symbol input decimation factor register.

Parallel mode - Bank 1. Address 5. Type Read / Write.
Serial mode - Address 13.

7	6	5	4	3	2	1	0
Reserved					SYM_RATIO[2:0]		

SYM_RATIO[2:0] Input decimation factor for IIN and QIN inputs, no filtering.

SYM_RATIO[2:0]	Decimation factor
0	no decimation
1	input every second sample
2	input every fourth sample
3	input every eighth sample
4	input every sixteenth sample
5 to 7	reserved

2.6.5. AGC_REF: Reference AGC level registers.

Parallel mode - Bank 1. Address 6. Type Read / Write.
Serial mode - Address 14.

7	6	5	4	3	2	1	0
AGC_REF[7:0] Reference AGC level							

AGC_REF[7:0] Reference AGC level sets the ratio of the input signal range (S) to the ADC range (R). The objective is to maintain this a constant ratio (S : R = 1 : 1.7).

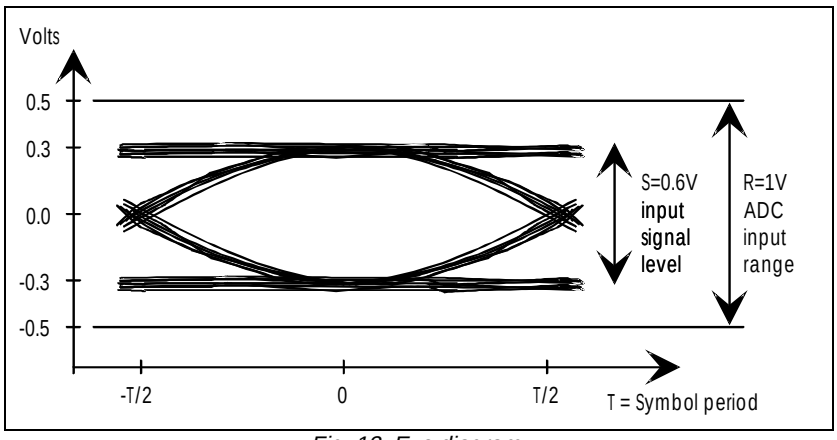


Fig. 12. Eye diagram.

The AGC_REF value is found from the following formula:

$$AGC\_REF = 233.3 * L * \frac{S^2}{R^2}$$

Where: S = Signal peak-to-peak level at the ADC input
R = Input range of the ADC.
L = 1 for no filtered decimation, SYM_CONFIG[1:0] = 0
or L = 4 for some filtered decimation, SYM_CONFIG[1:0] = 1 or 2, (this adds 6dB gain)

Therefore:

for L = 1 $AGC\_REF = 233.3 * 1 * \frac{0.6^2}{1^2} = 84.$

for L = 4 $AGC\_REF = 233.3 * 4 * \frac{0.3^2}{1^2} = 84.$

2.6.6. AGC_BW: AGC estimation bandwidth register.

Parallel mode - Bank 1. Address 7. Type Read / Write.
Serial mode - Address 15.

7	6	5	4	3	2	1	0
Reserved					INT_DC	AGC_BW[1:0]	

AGC_BW[1:0] AGC estimation bandwidth.

AGC_BW[1:0]	Symbol rate Rs MSym/s
0	>20
1	10 - 20
2	5 - 10
3	Reserved

The AGC control signal drives the Sigma Delta modulated output AGC_OUT pin. This output can drive an external passive RC filter feeding the AGC stage. The RC time constant should be <63.6µs.

INT_DC Internal DC offset.
High = Enable internal DC offset compensation on I and Q channels.
Low = Disable internal DC offset compensation on I and Q channels.

2.7. BANK 2: Program QPSK registers.

2.7.1. SCALE: IOUT and QOUT outputs, scale factor register.

Parallel mode - Bank 2. Address 1. Type Read / Write.
Serial mode - Address 17.

7	6	5	4	3	2	1	0
SCALE[7:0] Scale factor for IOUT and QOUT outputs							

SCALE[7:0] Scale factor for IOUT and QOUT outputs. The value in the SCALE register adjusts the matched filter outputs before the signal is truncated to 3 bits. These signals are output from the QPSK block and fed direct to the Viterbi block.

For an AGC_REF setting of 84, the SCALE value is recommended to be set to 158.

2.7.2. SNR_THS: Signal to noise ratio estimator threshold register.

Parallel mode - Bank 2. Address 2. Type Read / Write.
Serial mode - Address 18.

7	6	5	4	3	2	1	0
SNR_THS[7:0] SNR estimator threshold							

SNR_THS[7:0] SNR estimator threshold.

The SNR is compared internally to the value set in the SNR_THS register. Fig 14 on page 38 shows the relationship between the parameter and the Symbol energy to Noise power ratio (Es / No). A value for SNR_THS of 100 which corresponds to an Es / No of 11dBs is recommended during tracking mode. After acquisition is complete, set the SNR_THS value to zero.

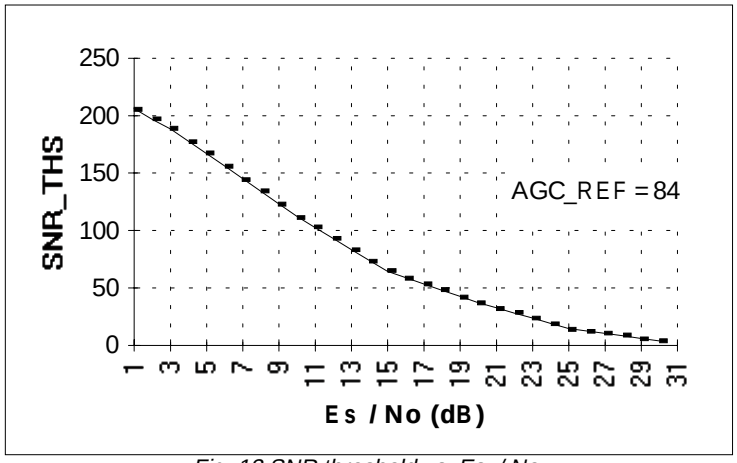


Fig. 13 SNR threshold vs. Es / No.

2.7.3. CR_OFFSET: Carrier loop DC offset register.

Parallel mode - Bank 2. Address 3. Type Read / Write.
Serial mode - Address 19.

7	6	5	4	3	2	1	0
CR_OFFSET[7:0] Carrier loop DC offset compensation value							

CR_OFFSET[7:0] Carrier loop DC offset compensation value. This is used to suppress internal DC offsets on the I and Q channels. This feature is only enabled when the carrier loop is closed, CR_OPEN bit must be set low in the CR_CONFIG register, see page 44.

The CR_OFFSET[7:0] value is a signed integer in the range -128 to +127.

Because of imperfections in the analog components in the loop filter, it is possible that the loop voltage shows a DC offset. This can have the following consequences:

- During the acquisition phase, the frequency sweeping becomes asymmetric. The DC offset causes the sweep to slow down in one direction and speed up in the other direction. If sweeping is too slow, false locks can occur in high signal to noise ratio conditions. If sweeping is too fast, true locks can be missed in low signal to noise ratio conditions.

- During the tracking phase, the static error of the loop is not a minimum, since the DC offset generates a frequency ramp that the loop has to compensate for.

The following figure shows the effect the CR_OFFSET value can have on the carrier sweep. The graph indicates a cross-over point at about -18 when Trise = Tfall. Moving CR_OFFSET more negative lengthenes the Trise and shortens the Tfall and visa versa.

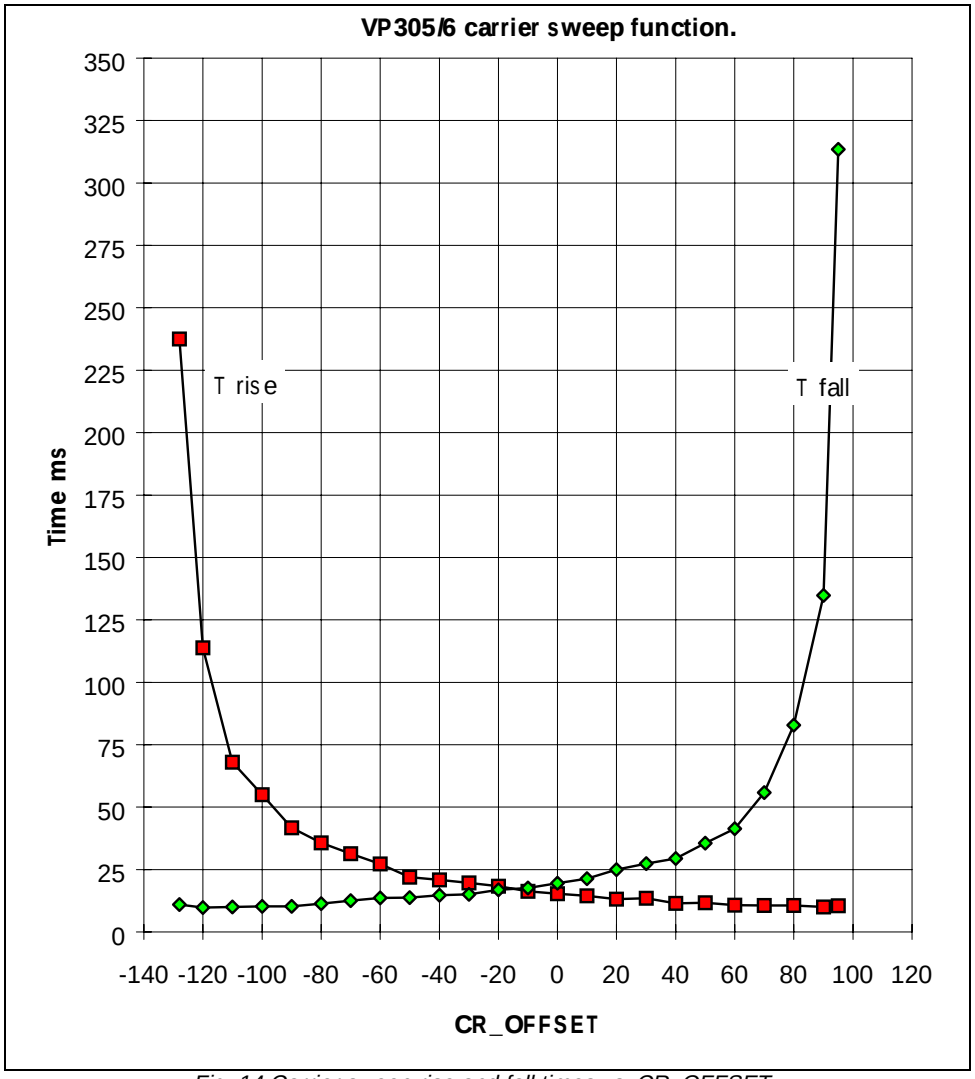


Fig. 14 Carrier sweep rise and fall times vs. CR_OFFSET..

2.7.3.1. Acquisition Phase.

To calculate the DC offset value required, the period of each ramp should be measured and used in the following formula:

$$CR\_OFFSET = \pm \frac{CR\_SWR}{2} * \frac{Tdwn - Tup}{Tdwn + Tup}$$

Where: Tup = the ramp up time
Tdown = the ramp down time

The ± choice depends on the polarity of the VCO U/D signals. Select + if polarity is normal or - if polarity is swapped (inverted). This is set by the CR_CONFIG[6] bit, see page 44.

The ramp times can be measured by observing the time intervals between the setting of interrupts INT_QPSK[6] and INT_QPSK[7]. These interrupts are generated when the lower and upper frequency limits are reached respectively, see page 27.

The relationship between the offset voltage and the CR_OFFSET parameter is as follows:

$$Voffset = \pm \frac{CR\_OFFSET}{32 * CR\_KP} * VDD$$

See above for choice of ±.

2.7.3.2. Tracking Phase.

During the tracking phase, the mean value of the phase error should be zero. The mean value is internally computed and subtracted from the phase error before the Sigma-Delta conversion. This system is only operational in the tracking mode, set by CR_CONFIG[1] = 0, see page 44.

The maximum DC offset voltage which can be compensated by this method is:

$$Voffset\_max = + \frac{CR\_OFFSET}{32 * CR\_KP} * VDD$$

e.g. for VDD = 3.3v, CR_OFFSET = 127

For CR_KP = 255, Voffset_max = 51mV (resolution 0.4mV)
For CR_KP = 30, Voffset_max = 437mV (resolution 3.4mV)

2.7.4. CR_RP: Carrier reference period register.

Parallel mode - Bank 2. Address 4. Type Read / Write.
Serial mode - Address 20.

7	6	5	4	3	2	1	0
Reserved				CR_RP[3:0] Carrier reference period			

CR_RP[3:0] Carrier frequency reference period for the count of the crystal clock cycles ($\overline{XTI}$ pin). This sets the reference for the measurement of the I/Q down converter VCO frequency (PSCAL pins). The register value sets the 4 most significant bits of a 14 bit counter. The actual count is CR_RP[3:0] * 1024. See page 12 for further discussion.

2.7.5. CR_KP: Carrier loop filter gain (P term) register.

Parallel mode - Bank 2. Address 5. Type Read / Write.
Serial mode - Address 21.

7	6	5	4	3	2	1	0
CR_KP[7:0] Carrier loop filter gain (P term)							

CR_KP[7:0] Carrier loop filter gain (P term)

This term, CR_KP * 2 determines the resolution of the Sigma Delta conversion. It should be >30 for six bits of resolution.

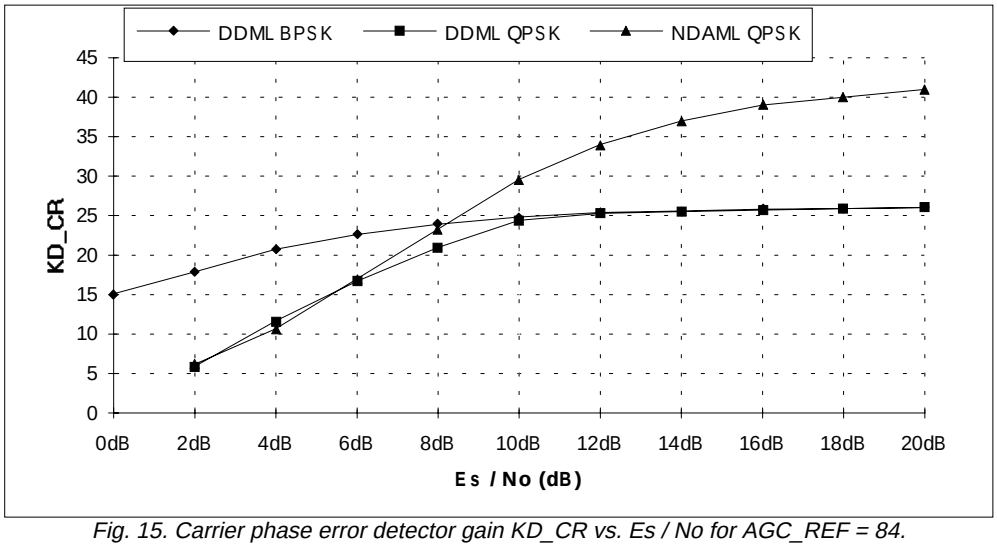


Fig. 15. Carrier phase error detector gain KD_CR vs. Es / No for AGC_REF = 84.

2.7.6. CR_KD: Carrier loop filter gain (D term) register.

Parallel mode - Bank 2. Address 6. Type Read / Write.
Serial mode - Address 22.

7	6	5	4	3	2	1	0
CR_KD[7:0] Carrier loop filter gain (D term)							

CR_KD[7:0] Carrier loop filter gain (D term)

The loop damping factor is given by the following equation:

$$\zeta = \frac{2 * CR\_KD * \omega_n}{Rs}$$

where ω_n = natural frequency in radians / second
Rs = QPSK symbol rate.

therefore $CR\_KD = \frac{\zeta * Rs}{2 * \omega_n}$

2.7.7. CR_THSL: Carrier lock detector threshold register.

Parallel mode - Bank 2. Address 7. Type Read / Write.
Serial mode - Address 23.

7	6	5	4	3	2	1	0
CR_THSL[7:0] Carrier lock detector threshold							

CR_THSL[7:0] Carrier lock detector threshold. This should be set to correspond to the phase lock detector length set by bit 4 of the CONFIG register, see page 45.

CONFIG[4]	CR_THSL
0	31
1	72

2.8. BANK 3: Program QPSK registers.

2.8.1. CR_SWR: Carrier sweep rate register.

Parallel mode - Bank 3. Address 1. Type Read / Write.
Serial mode - Address 25.

7	6	5	4	3	2	1	0
CR_SWR[7:0] Carrier sweep rate							

CR_SWR[7:0] Carrier sweep rate.

$$CR\_SWP = 64 * K_{DCR} * \theta$$

Where: K_{DCR} is the carrier phase detector gain, typically 10 for low Eb / No of 4 dB.
θ is the phase lock loop steady state error during acquisition. θ should be lower than 5° expressed in radians. During the tracking phase, the loop drives the residual steady state error to 0.

Therefore, if $K_{DCR} = 10$ and $\theta = 3° = 0.052$rad.

$$CR\_SWP = 64 * 10 * 0.052 = 33 \text{ (rounded down).}$$

The frequency sweep rate is given by the following formula:

$$f = \frac{5 * CR\_SWP}{128 * \pi * CR\_KP} * \frac{K_{VCOCR}}{R_{CR} * C_{CR}} * \frac{VDD}{5V} \text{ Hz/s}$$

For the SL1710 $K_{VCOCR} = 11.56$Mrad/s/V.

For VDD = 3.3V

Therefore $$f = \frac{5 * 33 * 11.56 * 10^6 * 3.3}{128 * \pi * CR\_KP * R_{CR} * C_{CR} * 5} = \frac{3.13 * 10^6}{CR\_KP * R_{CR} * C_{CR}}$$

The sweep rate varies as a function of the value of CR_SWR register and the delta frequency, effectively selected by the CR_USWL and CR_LSWL registers. If the delta frequency is halved, the sweep rate doubles. If the receiver fails to lock, a higher value of CR_SWR should be tried. If the value of CR_SWR is too low, the frequency sweep may be stopped. The rise and fall times of the sweep can be adjusted to be equal by setting the value of CR_OFFSET, see page 37. This becomes more critical at very low values of CR_SWR where the sweep will stop unless the rise and fall times are equal.

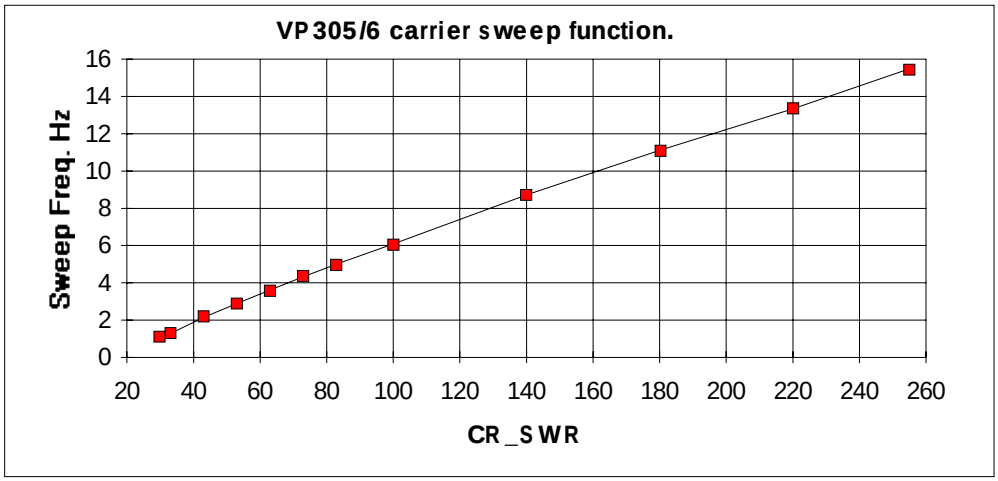


Fig. 16. Carrier sweep rate for a delta frequency of ±10MHz.

2.8.2. CR_USWL U & L: Carrier Upper sweep limit registers.

Parallel mode - Bank 3. Addresses 2, 3. Type Read / Write.
Serial mode - Addresses 26, 27.

7	6	5	4	3	2	1	0
Reserved		CR_USWL[13:8] Carrier Upper sweep limit (upper nibble)					
CR_USWL[7:0] Carrier Upper sweep limit (lower byte)							

These two bytes together form the 14 bit number: CR_USWL[13:0] Carrier Upper sweep limit. This is the division ratio (upper) for the prescaler input (PSCAL) from the SL1710. See page 12 for further discussion.

2.8.3. CR_LSWL U & L: Carrier Lower sweep limit registers.

Parallel mode - Bank 3. Addresses 4, 5. Type Read / Write.
Serial mode - Addresses 28, 28.

7	6	5	4	3	2	1	0
Reserved		CR_LSWL[13:8] Carrier Lower sweep limit (upper nibble)					
CR_LSWL[7:0] Carrier Lower sweep limit (lower byte)							

These two bytes together form the 14 bit number: CR_LSWL[13:0] Carrier Lower sweep limit. This is the division ratio (lower) for the prescaler input (PSCAL) from the SL1710.

2.8.4. CR_CONFIG: Carrier configuration register.

Parallel mode - Bank 3. Address 6. Type Read / Write.
Serial mode - Address 30.

7	6	5	4	3	2	1	0
CR_CONFIG[7:0] Carrier configuration							

CR_CONFIG[0] CR_SW
High = carrier loop sweep on.
Low = carrier loop sweep off.

CR_CONFIG[1] CR_OPEN
High = carrier loop open. This is only used to get out of a false lock.
Low = carrier loop closed.

CR_CONFIG[2] CR_PED_SEL Carrier phase error detector select.
High = NDAML Non-data aided maximum likelihood estimator (only available in QPSK mode).
Low = DDML Decision directed maximum likelihood estimator.

CR_CONFIG[3] Reserved set low.

CR_CONFIG[4] CR_VCO1 D/U
High = tri-state D and U outputs.
Low = active outputs.

CR_CONFIG[5] CR_VCO2 D/U
High = tri-state D and U outputs.
Low = active outputs.

CR_CONFIG[6] CR_VCO_SWAP exchange polarity for both CR_VCO1 and CR_VCO2 D and U outputs.
High = swapped (i.e. D and U inverted).
Low = normal.

CR_CONFIG[7] CR_SWEEP_SWAP change carrier sweep direction.
High = swapped.
Low = normal.

2.8.5. CONFIG: Configuration register.

Parallel mode - Bank 3. Address 7. Type Read / Write.
Serial mode - Address 31.

7	6	5	4	3	2	1	0
CONFIG[7:0]							

CONFIG[0] IIN and QIN input format selector.
High = 2's complement format.
Low = Offset binary format. This is the normal format used with the VP216/7.

Code for six bit input	Offset binary CONFIG[0] = 0	Offset 2's Complement CONFIG[0] = 1
00	000000	100000
01	000001	100001
•	•	•
31	011111	111111
32	100000	000000
33	100001	000001
•	•	•
62	111110	011110
63	111111	011111

CONFIG[1] Reserved set low.

CONFIG[2] Reserved set high.

CONFIG[3] AGC out.
High = inverted.
Low = normal.

CONFIG[4] FP_LOCK_LEN : Frequency / Phase lock detector length.
High = short.
Low = normal - long.

See also CR_THSL register on page 41.

CONFIG[5] Reserved set low.

CONFIG[6] Constellation selector.
High = BPSK.
Low = QPSK..

CONFIG[7] SNR Estimator on/off.
High = used.
Low = off.

2.9. BANK 4: Monitor FEC read registers.

2.9.1. VIT_ERR_C H & L: Viterbi error count registers.

Parallel mode - Bank 4. Addresses 1, 2. Type Read.
Serial mode - Addresses 33, 34.

7	6	5	4	3	2	1	0
VERRC[15:8] - Viterbi error count high byte							
VERRC[7:0] - Viterbi error count low byte							

These two bytes together form the 16 bit number: VERRC[15:0] Viterbi error count related to the period defined in the VIT_ERR H-M-L registers, see page 48. When the count increments to the maximum value, it freezes at 65535. The actual count = 4 x VERRC[15:0] data bits. The register is NOT reset to zero when it is read. See also figure 8 on page 15.

2.9.2. RS_UBC: Reed Solomon uncorrected block count register.

Parallel mode - Bank 4. Address 3. Type Read.
Serial mode - Address 35.

7	6	5	4	3	2	1	0
RSUBC[7:0] - Reed Solomon uncorrected block count							

RSUBC[7:0] Reed Solomon uncorrected block count. When the count increments to the maximum value, it freezes at 255. The register is reset to zero when it is read.

2.10. BANK 5: Program FEC registers.

2.10.1. VIT_MODE: Viterbi mode register.

Parallel mode - Bank 5. Address 1 Type Read / Write.
Serial mode - Address 41.

7	6	5	4	3	2	1	0
IQSWAP	F_LOCK	Reserved			VITCR[2:0] - code rate		

VITCR[2:0] Viterbi code rate

VITCR[2:0]	code rate
0	1/2
1	2/3
2	3/4
3	5/6
4	7/8
5	1/2
6	1/2
7	1/2

F_LOCK False lock
High = Exit false lock state. This is automatically set low after use.
Low = normal.
See section 2.10.5 on page 49 for an explanation on how to use this bit.

IQSWAP I / Q Swap
High = I lags Q.
Low = I leads Q.

2.10.2. VIT_ERR H, M & L: Viterbi error period registers.

Parallel mode - Bank 5. Addresses 2, 3, 4. Type Read / Write.
Serial mode - Addresses 42, 43, 44.

7	6	5	4	3	2	1	0
VITEP[23:16] - Viterbi error period high byte							
VITEP[15:8] - Viterbi error period middle byte							
VITEP[7:0] - Viterbi error period low byte							

These three bytes together form the 24 bit number: VITEP[23:0] Viterbi error period, effectively the number of valid data bits, during which an error count is accumulated. At the end of the defined period, the error count is frozen and that value stored in the VIT_ERR_C H-L registers, see page 46. Also at the end of the defined period, an interrupt is generated on the $\overline{\text{IRQ}}$ line to advise the microprocessor that a new error count is available to be read. The interrupt is enabled by setting the IE_FEC[2] bit in the IE_FEC register, see page 52. The actual period = 4 x VITEP[23:0] data bits. See also figure 8 on page 15.

2.10.3. VI_MAX_ERR: Viterbi maximum bit error count register.

Parallel mode - Bank 5. Address 5. Type Read / Write.
Serial mode - Address 45.

7	6	5	4	3	2	1	0
VMERR[7:0] - Viterbi max. bit error count							

VMERR[7:0] Viterbi maximum bit error count. When the coarse count reaches the number programmed in VMERR[7:0], the count is reset to zero and an interrupt is generated on the VERR line (provided the INTVIS bit is enabled in the TEST2 register, see page 56). This technique provides a visible indication of the frequency of bit errors in the signal. It may be used, via a suitable monitor device, to assist in receiver dish alignment. The actual count = 4 x VMERR[7:0] data bits. See also figure 9 on page 16.

2.10.4. VI_BER_PER: Viterbi bit error rate based synchronisation period register.

Parallel mode - Bank 5. Address 6. Type Read / Write.
Serial mode - Address 46.

7	6	5	4	3	2	1	0
VBPER[7:0] - Viterbi bit error rate based synchronisation period							

VBPER[7:0] Viterbi bit error rate based synchronisation period.
The actual period = 256 x VBPER[7:0] data bits.

2.10.5. VI_BER_LIM: Viterbi bit error rate based synchronisation limit register.

Parallel mode - Bank 5. Address 7. Type Read / Write.
Serial mode - Address 47.

7	6	5	4	3	2	1	0
VBLIM[7:0] - Viterbi bit error rate based synchronisation limit							

VBLIM[7:0] Viterbi bit error rate based synchronisation limit.
The actual limit = 128 x VBLIM[7:0] + 32 data bits.

The Viterbi bit error rate threshold is the ratio of the register values:

Threshold = VI_BER_LIM / VI_BER_PER

The following table shows recommended threshold values for the various Viterbi code rates. If the Viterbi bit error rate threshold is set too low, the Viterbi circuit will lock up on incorrect data. But conversely, if the threshold is set too high, the Viterbi circuit will have difficulty in llocking up. A false lock may be exited by toggling F_LOCK (bit 6 of VIT_MODE register, see page 47).

Coding rate	min.	max.
1/2	0.090	0.120
2/3	0.055	0.070
3/4	0.035	0.050
5/6	0.020	0.035
7/8	0.010	0.025

Table 9. Viterbi bit error rate threshold. .

2.11. BANK 6: Program FEC and general control registers.

2.11.1. VIT_CTRL1: Viterbi control synchronisation byte register 1

Parallel mode - Bank 6. Address 1. Type Read / Write.
Serial mode - Address 49.

7	6	5	4	3	2	1	0
BS_MODE[1:0]		VS_UNLK[3:0]				VBIT_MV[1:0]	

VBIT_MV[1:0] Viterbi synchronisation majority voting selection for the number of correct bits in a byte to have the byte labelled as a synchronisation byte.

VBIT_MV[1:0]	No. correct bits in sync	
0	5	
1	6	← Recommended
2	7	
3	8	

Table 10. Number of correct bits in the sync byte.

VS_UNLK[3:0] Viterbi sync majority voting selection for retaining sync lock.

VIT_CTRL1 (weighted)	VS_UNLK[3:0]	No. syncs to keep lock	
0	0	3	
4	1	4	
8	2	5	
12	3	6	
16	4	7	← Recommended
20	5	8	
24	6	9	
28	7	10	
32	8	11	
36	9	12	
40	10	13	
44	11	14	
48	12	15	
52	13	16	
56	14	17	
60	15	18	

Table 11. Number of correct sync bytes to retain lock.

BS_MODE[0] Byte sync mode bit 0
High = seeking lock
Low = normal

BS_MODE[1] Byte sync mode bit 1
High = remaining in lock
Low = normal

2.11.2. VIT_CTRL2: Viterbi control synchronisation byte register 2

Parallel mode - Bank 6. Address 2. Type Read / Write.
Serial mode - Address 50.

7	6	5	4	3	2	1	0
VIT_CTRL2[7:3] - Reserved					VS_LK[2:0]		

VS_LK[2:0] Viterbi synchronisation acquire. This defines the number of consecutive synchronisation bytes that need to be detected before block lock is established.

VS_LK[2:0]	No. syncs for lock	
0	2	
1	3	
2	4	
3	5	← Recommended
4	6	
5	7	
6	Not valid	
7	Not valid	

Table 12. Number of consecutive sync bytes to establish block lock.

VIT_CTRL2[7:3] These bits are reserved for test applications. For normal operation, they must be set to zero.

2.11.3. IE_FEC: Interrupt FEC register.

When the bits of this register are set high, they enable an event signalled in the INT_FEC register to generate an interrupt on the $\overline{IRQ}$ pin. They do not affect the setting of bits in the INT_FEC register, see page 28.

Parallel mode - Bank 6. Address 3. Type Read / Write.
Serial mode - Address 51.

7	6	5	4	3	2	1	0
IE_FEC[7:0] Interrupt enable FEC							

IE_FEC[7:0] Interrupt enable FEC

When : IE_FEC[i] =1 : enable INT_FEC[i]
IE_FEC[i] =0 : disable INT_FEC[i] (default state)

where i = 0 to 7.

IE_FEC[0] High = Enable Descrambler lock established indication in INT_FEC register.

IE_FEC[1] High = Enable Descrambler lock lost indication in INT_FEC register.

IE_FEC[2] High = Enable Viterbi error period indication in INT_FEC register.

IE_FEC[3] Reserved set low.

IE_FEC[4] High = Enable Viterbi bit lock established indication in INT_FEC register.

IE_FEC[5] High = Enable Viterbi bit lock lost indication in INT_FEC register.

IE_FEC[6] High = Enable Frame alignment lock established indication in INT_FEC register. (A Frame is 8 blocks, each block is 204 bytes).

IE_FEC[7] High = Enable Frame alignment lock lost indication in INT_FEC register.

2.11.4. STAT_EN: Status enable register.

Parallel mode - Bank 6. Address 4. Type Read / Write.
Serial mode - Address 52.

7	6	5	4	3	2	1	0
STAT_EN[7:0] Enable various outputs on STATUS pin.							

This register allows various indicator signals to be output on the STATUS pin. The signals are equivalent to the corresponding bits in the STATUS register, see page 29, or to events signalled in the INT_FEC register, see page 28.

Note: only one bit should be programmed high at any one time, otherwise a meaningless output on the STATUS pin will result!

STAT_EN[0] High = Enable Symbol AFC lock detect signal on the STATUS pin.

STAT_EN[1] High = Enable Carrier Phase lock detect signal on the STATUS pin.

STAT_EN[2] High = Enable Carrier Frequency lock detect signal on the STATUS pin.

STAT_EN[3] High = Enable SNR quality signal on the STATUS pin.

STAT_EN[4] High = Enable descrambler lock detect signal on the STATUS pin.

STAT_EN[5] High = Enable Viterbi bit lock detect signal on the STATUS pin.

STAT_EN[6] High = Enable Frame alignment lock detect signal on the STATUS pin.

STAT_EN[7] High = Enable symbol clock signal on the STATUS pin.

2.11.5. GEN_CTRL: General control register.

Parallel mode - Bank 6. Address 5. Type Read / Write.
Serial mode - Address 53.

7	6	5	4	3	2	1	0
-	-	-	MCLKINV	BSO	ENTEI	NSYNC[1:0]	

NSYNC[1:0] The number of successive incorrect synchronising bytes in N successive blocks before byte lock in the descrambler is lost. The value programmed is related to N as shown in the following truth table.

NSYNC[1:0]	No. incorrect sync bytes	
0	2	
1	3	← Recommended
2	4	
3	5	

Table 13. Number of incorrect sync bytes for descrambler to lose lock.

ENTEI High = Enable automatic setting of transport_error_indicator (TEI) bit in the MPEG packet header byte 2 when the block contains an uncorrectable byte error.

BSO High = Bit serial output of the MPEG data on MDO0 pin.

MCLKINV High = MCLK clock output inverted.
Low = MCLK clock output normal.

2.11.6. GPP_CTRL: General Purpose Port control register.

Parallel mode - Bank 6. Address 6. Type Read / Write.
Serial mode - Address 54.

7	6	5	4	3	2	1	0
Reserved			GPP_CTRL[4:1] External outputs control.				GPP_CTRL[0]

GPP_CTRL[i] bit drives the OUTPUT pin GPP[i]

where i = 1, 2, 3 or 4.

Note: GPP_CTRL[0] reads the logic level of the input pin GPP0. Writing to this bit has no effect.

2.11.7. RESET: Reset register.

Parallel mode - Bank 6. Address 7. Type Read / Write.
Serial mode - Address 55.

7	6	5	4	3	2	1	0
RES	-	-	-	PR_DS	PR_BS	FR_QP	PR_QP

PR_QP High = Partial reset of the QPSK block, except for the registers.
Low = No reset.

FR_QP High = Full reset of the QPSK block, including the registers.
Low = No reset.

PR_BS High = Partial reset of the byte synchronising mechanism.
Low = No reset.

PR_DS High = Partial reset of the De scramble block with its synchronising function.
Low = No reset.

RES High = Reset the complete chip, except for the microprocessor interface, to its default state.
Low = No reset.

2.12. BANK 7: Program test registers.

2.12.1. TEST1: Test 1 register - for diagnostic / qualification purposes only.

Parallel mode - Bank 7. Address 1. Type Read / Write.
Serial mode - Address 57.

7	6	5	4	3	2	1	0
Reserved							

TEST1[7:0] Set all bits low for normal operation.

2.12.2. TEST2: Test 2 register - for diagnostic / qualification purposes only.

Parallel mode - Bank 7. Address 2. Type Read / Write.
Serial mode - Address 58.

7	6	5	4	3	2	1	0
INTVIS	-	-	-	EN[3:0]			

EN[3:0] Enable / disable functions

EN3,2,1,0	QPSK	VITERBI	DEINT	RS	DESCR	
0	EN	EN	EN	EN	EN	← Default state
3	EN	EN	DIS	DIS	DIS	← Test viterbi output
All other states reserved.						

Table 14. Enable / disable circuit blocks.

In the mode 3, digitised I and Q data is input in the normal way to the QPSK decoder block. The output from the viterbi block is then connected directly to the MDO7:0 pins, bypassing the remaining blocks.

INTVIS High = Enable the toggled VERR output when VMERR (viterbi max. error count) is reset. See also figure 9 on page 16. This is the mode to assist in aligning the satellite dish.

Low = VERR pin held low.

2.12.3. TEST3: Test 3 register - for diagnostic / qualification purposes only.

Parallel mode - Bank 7. Address 3. Type Read / Write.
Serial mode - Address 59.

7	6	5	4	3	2	1	0
Reserved							

TEST3[7:0] Set all bits low for normal operation.

3. MICROPROCESSOR CONTROL.

Selection of the microprocessor interface type is controlled by the $\overline{SER}$ pin.

$\overline{SER}$	interface type
0	I²C bus interface
1	Parallel interface

3.1. I²C bus Interface.

Not available on VP305.

The I²C bus serial interface (ref. 2.) uses pins:

SDA Serial data, the most significant bit is sent first.
SCL Serial clock (D0).

The I²C bus Address is 0001 110 R/$\overline{W}$.

The circuit works as a slave transmitter with the eighth bit set high or as a slave receiver with the eighth bit set low. In receive mode, the first data byte is written to RADD register, which forms the register sub-address.

Bit 7 of the RADD register, IAI is an Increment Auto Inhibit function. When the IAI bit is set high, the automatic incrementing of register addresses is inhibited. IAI set low is the normal situation so that data bytes sent on the I²C bus after the RADD register data are loaded into successive registers. This automatic incrementing feature avoids the need to individually address each register.

Following a valid chip address, the I²C bus STOP command resets the RADD register to 01. If the chip address is not recognised, the VP306 will ignore all activity until a valid chip address is received. The I²C bus START command does NOT reset the RADD register to 01. This allows a combined I²C bus message, to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. RADD would not be sent in this case. Finally a STOP command should be sent to free the bus.

When the I²C bus is addressed (after a recognised STOP command) with the read bit set, the first byte read out shall be the content of register 01. To access the chip identification in register 00, the microprocessor should send the chip address with the write bit set, followed by the register address 00, then a restart with the read bit set, followed by a data read.

3.1.1. Examples of I²C bus messages:

KEY:	S	Start condition	W	Write (= 0)
	P	Stop condition	R	Read (= 1)
	A	Acknowledge	NA	NOT Acknowledge
	ITALICS	VP305/6 output		

Write operation - as a slave receiver.

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	DATA (reg n)	***A***	DATA (reg n+1)	***A***	P

Read operation - VP305/6 as a slave transmitter.

S	DEVICE ADDRESS	R	***A***	***DATA (reg 1)***	A	***DATA (reg 2)***	A	***DATA (reg 3)***	NA	P

Write/read operation with repeated start - VP305/6 as a slave transmitter.

S	DEVICE ADDRESS	W	***A***	RADD (n)	***A***	S	DEVICE ADDRESS	R	***A***	***DATA (reg n)***	A	***DATA (reg n+1)***	NA	P

Write/read/write operation with repeated start and auto increment off with IAI set high - VP305/6 as a slave transmitter. This example uses the GPP_CTRL register which has a read bit 0 and write bits 1 to 4. Register address is 54 + 128 (IAI).

S	DEVICE ADDRESS	W	***A***	RADD (182)	***A***	S	DEVICE ADDRESS	R	***A***	***DATA (reg 54)***	NA	S	DEVICE ADDRESS	W	***A***	DATA (reg 54)	***A***	P

Note: The serial register map is NOT continuous. The increment function will address the non-used addresses, so when writing a sequence of data, dummy data will need to be inserted at the appropriate points for the non-used addresses. Similarly, when reading a sequence of data, the value 255 will be read out from the non-used addresses.

3.2. Parallel interface.

The Parallel interface is selected by a logic '1' on the $\overline{SER}$ pin.

This uses pins:

D7-0	data input/output bus
A2-0	address input bus
$\overline{CS}$	chip select
$\overline{AS}$	address select
$\overline{DTAK}$	data acknowledge
R/$\overline{W}$	read / write control

Registers are directly addressed via the address bus. There is no register incrementing feature as on the I²C bus interface.

3.2.1. Examples of writing to and reading from the parallel interface.

To write the value 64 to the CONFIG register 7 in Bank 3, send the following sequence:

Set R/$\overline{W}$ to write	
Addr[0],Data[24]	this writes 24 (Bank 3) to the BANK register
Addr[7],Data[64]	this writes 64 to register 7 (of Bank 3) (CONFIG)

To read the value of the RS_UBC register 3 in Bank 4, send the following sequence:

Set R/$\overline{W}$ to write	
Addr[0],Data[32]	this writes 32 (Bank 4) to the BANK register
Set R/$\overline{W}$ to read	
Addr[3],Data[?].	this reads register 3 (of Bank 4) (RS_UBC)

It is not necessary to write the value of the BANK register if writing to / or reading from a group of registers in the same bank. For example, to read the registers 1 to 6 of Bank 0:

Set R/$\overline{W}$ to write	
Addr[0],Data[0]	this writes 0 to the BANK register
Set R/$\overline{W}$ to read	
Addr[1],Data[?].	this reads register 1 (of Bank 0) (INT_QPSK)
Addr[2],Data[?].	this reads register 2 (of Bank 0) (INT_FEC)
Addr[3],Data[?].	this reads register 3 (of Bank 0) (STATUS)
Addr[4],Data[?].	this reads register 4 (of Bank 0) (AGC_LVL)
Addr[5],Data[?].	this reads register 5 (of Bank 0) (CR_VCOF U)
Addr[6],Data[?].	this reads register 6 (of Bank 0) (CR_VCOF L)

3.2.2. Parallel interface Write cycle description.

A write cycle starts with the master indicating its intent by setting R/$\overline{W}$ to write and placing a valid address on A2:0 and asserting $\overline{AS}$. The VP305/6 takes the assertion of $\overline{AS}$ as the start of a cycle and latches the address on A2:0 by the falling edge $\overline{AS}$. This event also causes VP305/6 to respond to the request by the master to send data, WHEN IT CAN, by asserting $\overline{DTACK}$. The

master requests to send data by asserting $\overline{CS}$, data may be placed on the data bus before or after asserting $\overline{CS}$.

Notice that there is no maximum time specified from the assertion of $\overline{AS}$ to the assertion of $\overline{DTACK}$. It is assumed that the master will insert wait states/cycles until $\overline{DTACK}$ is recognised.

When the master negates $\overline{CS}$ the VP305/6 will latch the data on D7:0 on the rising edge of $\overline{CS}$. When the master negates $\overline{CS}$ the VP305/6 will then negate $\overline{DTACK}$.

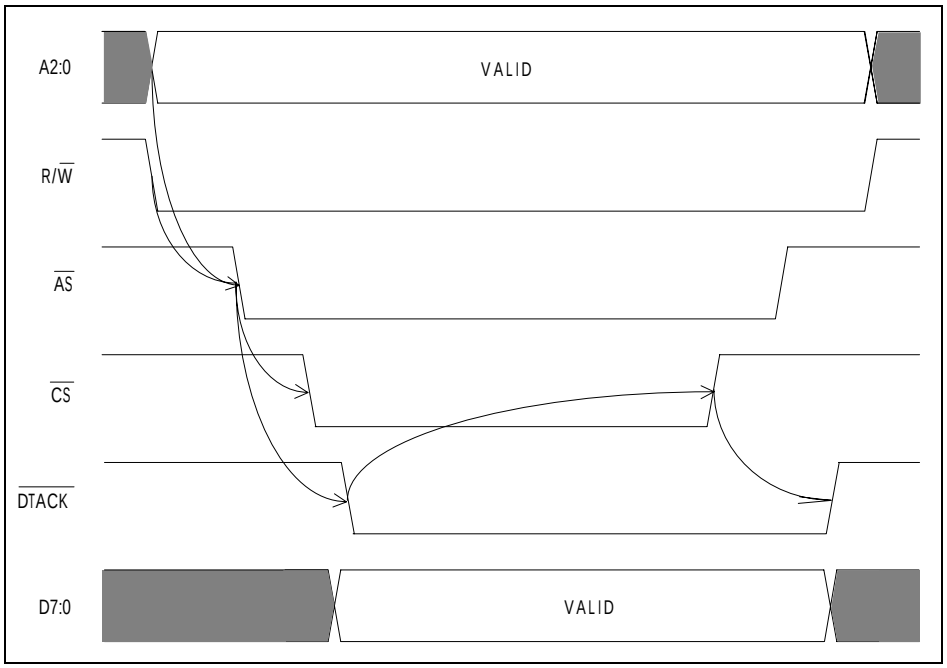
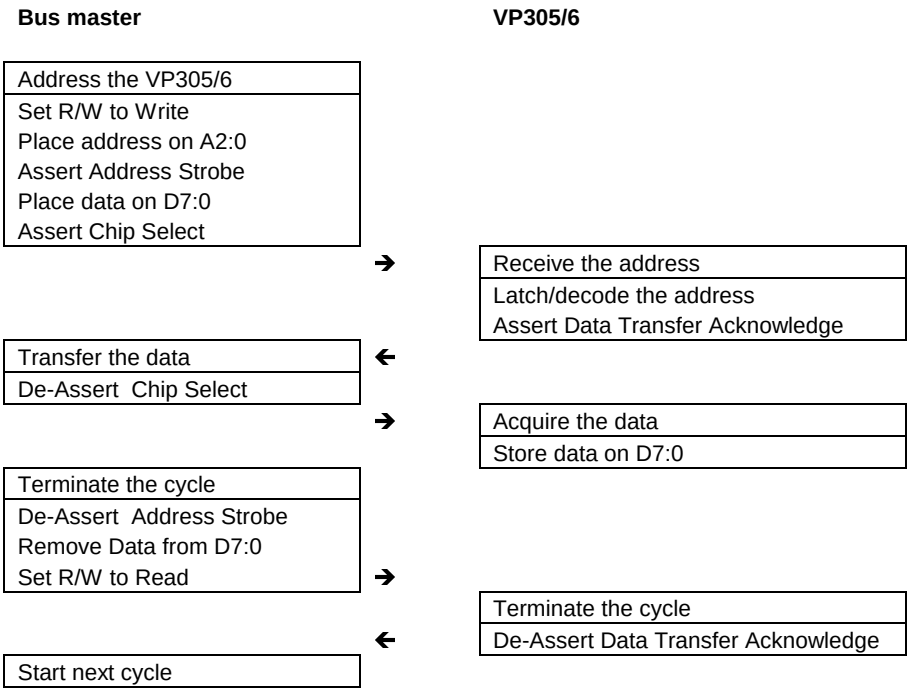


Fig. 17. Parallel interface write cycle action diagram.

Write cycle flowchart.



3.2.3. Parallel interface Read cycle description.

A read cycle starts with the master indicating its intent by setting R/$\overline{W}$ to read and placing a valid address on A2:0 and asserting $\overline{AS}$. The VP305/6 takes the assertion of $\overline{AS}$ as the start of a cycle and latches the address on A2:0 by the falling edge $\overline{AS}$. This event also causes VP305/6 to respond to the data request, WHEN IT CAN, by placing valid data on the data bus and asserting $\overline{DTACK}$, informing the master that it may proceed. The master then requests data by asserting $\overline{CS}$.

Notice that there is no maximum time specified from the assertion of $\overline{AS}$ to the assertion of $\overline{DTACK}$. It is assumed that the master will insert wait states/cycles until $\overline{DTACK}$ is recognised.

The master will then read the data on D7:0 and negate $\overline{CS}$ and $\overline{AS}$. The negation of $\overline{CS}$ causes the VP305/6 to remove the data from D7:0 and then negate $\overline{DTACK}$.

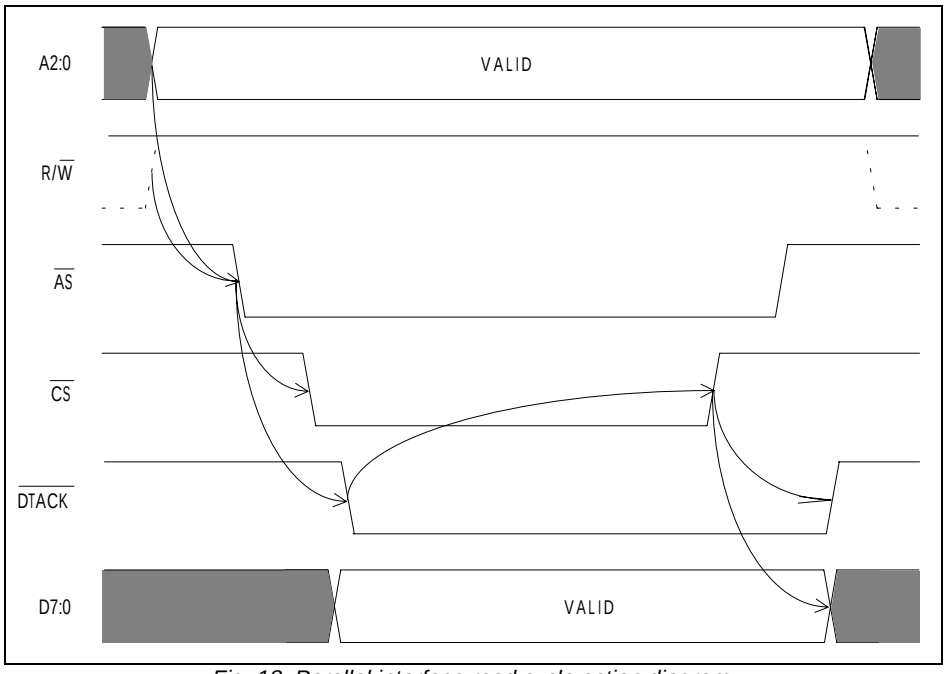
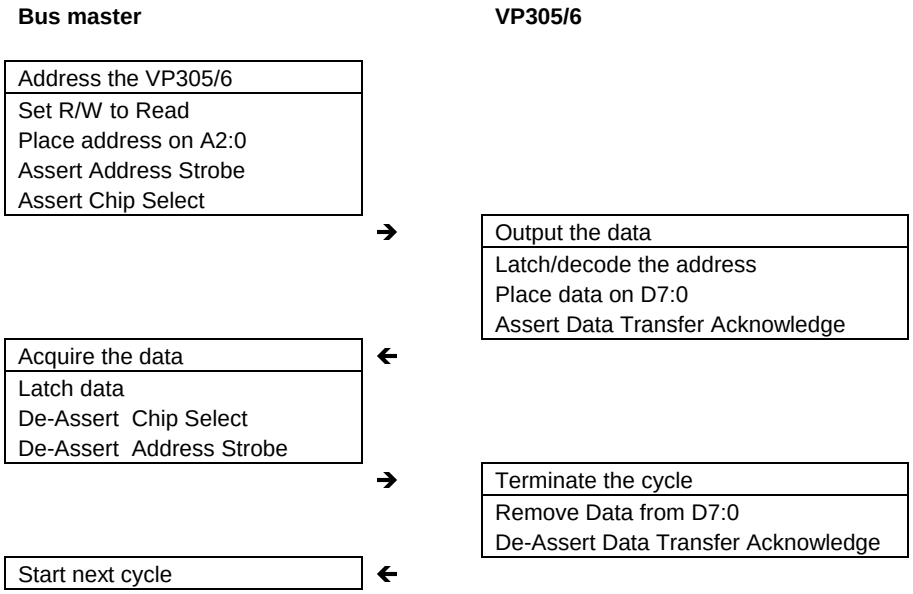


Fig. 18. Parallel interface read cycle action diagram.

Read cycle flowchart.



4. TIMING INFORMATION.

4.1. I²C bus timing.

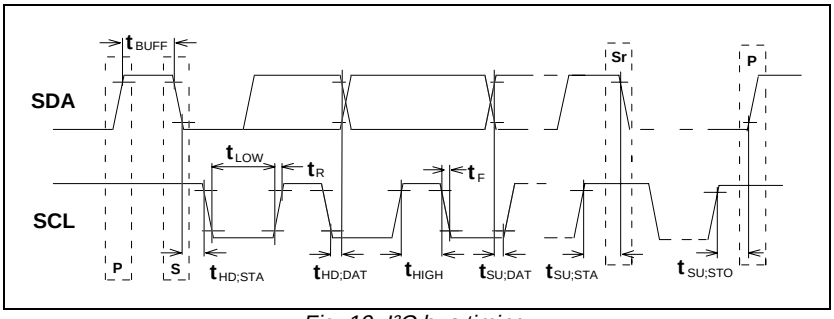


Fig. 19. I²C bus timing.

Where: S = Start
Sr = Restart, i.e. Start without stopping first.
P = Stop.

Parameter	Symbol	Value		Unit
		Min	Max.	
SCL clock frequency	f_{SCL}	0	450	kHz
Bus free time between a STOP and START condition.	t_{BUFF}	200		ns
Hold time (repeated) START condition.	$t_{HD;STA}$	200		ns
LOW period of SCL clock.	t_{LOW}	450		ns
HIGH period of SCL clock.	t_{HIGH}	600		ns
Set-up time for a repeated START condition.	$t_{SU;STA}$	200		ns
Data hold time (when input).	$t_{HD;DAT}$	100		ns
Data set-up time	$t_{SU;DAT}$	100		ns
Rise time of both SCL and SDA signals.	t_R		note 1	ns
Rise time of both SCL and SDA signals, (100pF to ground).	t_F		20	ns
Set-up time for a STOP condition.	$t_{SU;STO}$	200		ns

Table 15. I²C bus timing.

Note 1. The rise time depends on the external bus pull up resistor.

4.2. Parallel interface Write cycle timing.

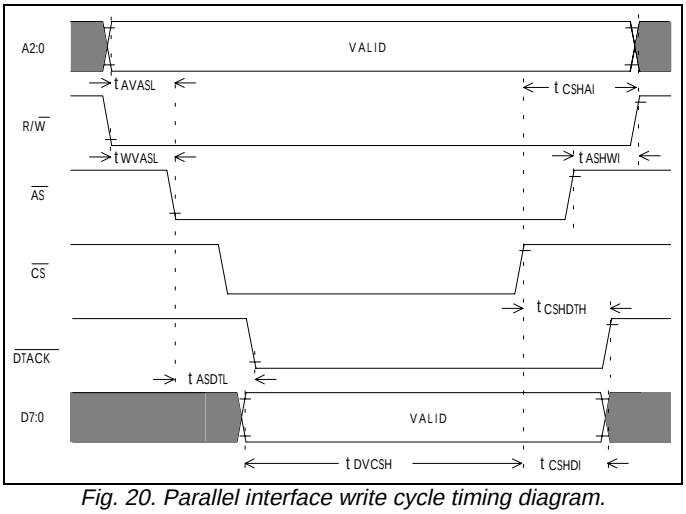


Fig. 20. Parallel interface write cycle timing diagram.

4.3. Parallel interface Read cycle timing.

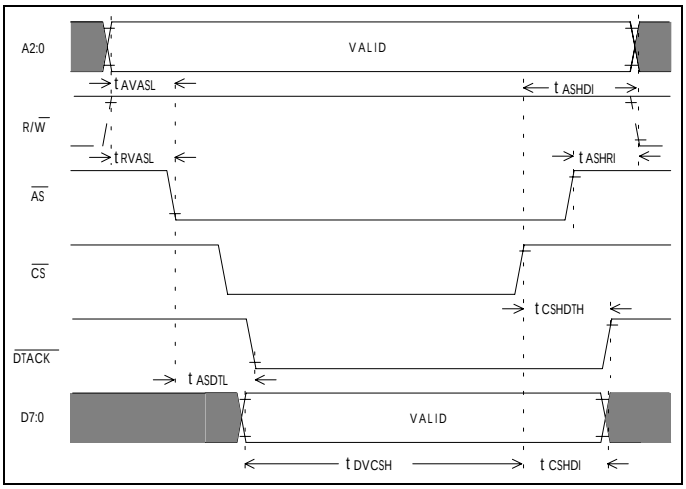


Fig. 21. Parallel interface read cycle timing diagram.

Symbol	Characteristic	Min.	Max.	Units
t_{AVASL}	Address Valid to Address Strobe Low			ns
t_{RVASL}	Read Valid to Address Strobe Low			ns
t_{WVASL}	Write Valid to Address Strobe Low			ns
t_{ASHDTH}	Address Strobe High to $\overline{\text{DTACK}}$ High			ns
t_{ASLDTL}	Address Strobe Low to $\overline{\text{DTACK}}$ Low			ns
t_{DVCSH}	Data Valid to Chip Select High			ns
t_{CSHAI}	Chip Select High to Address Invalid			ns
t_{ASHRI}	Address Strobe High to Read Invalid			ns
t_{ASHWI}	Address Strobe High to Write Invalid			ns
t_{CSHTDH}	Chip Select High to $\overline{\text{DTACK}}$ High			ns
t_{CSHDI}	Chip Select High to Data Invalid			ns

Table 16. Parallel bus timing.

4.4. Data input timing.

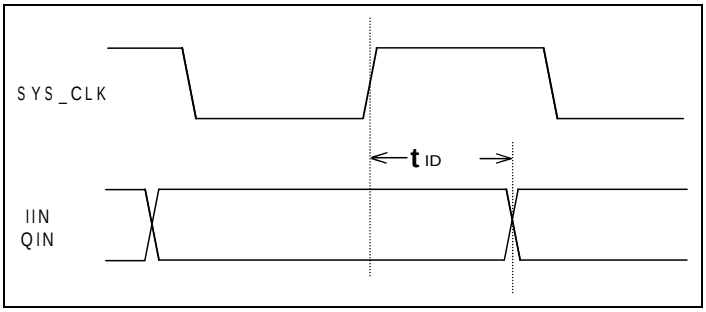


Fig. 22. VP305/6 data input timing diagram.

Parameter	Symbol	Min.	Typ.	Max.	Units
Data intput delay	tID	2.0		6.0	ns

5. MPEG PACKET DATA OUTPUT.

5.1. Data output format.

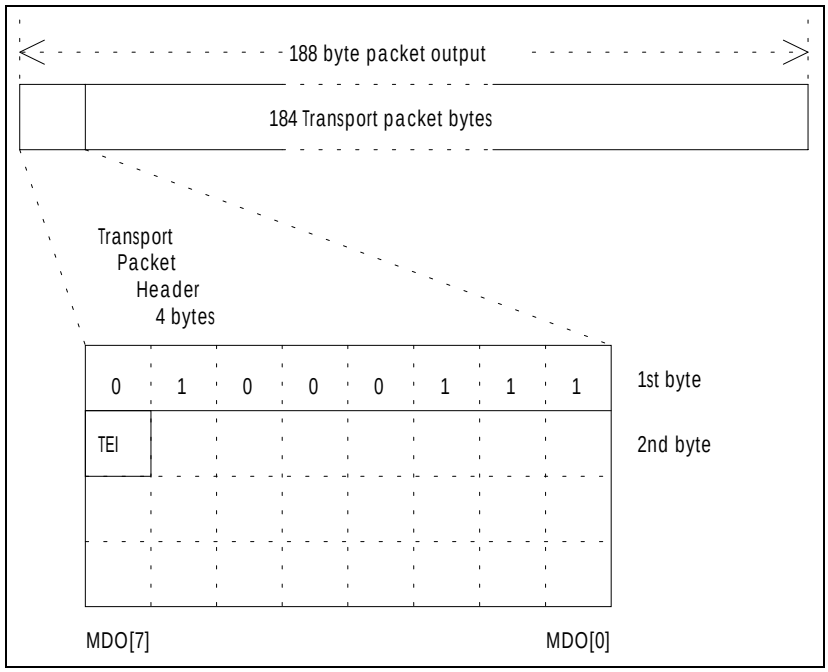


Fig. 23. VP305/6 Transport Packet Header bytes.

After decoding, the 188 byte MPEG packet is output on the MDO pins in 188 consecutive clock cycles.

Additionally, when the ENTEI bit in the GEN_CTRL register is set high, any decoded packets with uncorrectable bytes will automatically set the TEI bit in the MPEG header, see page 54.

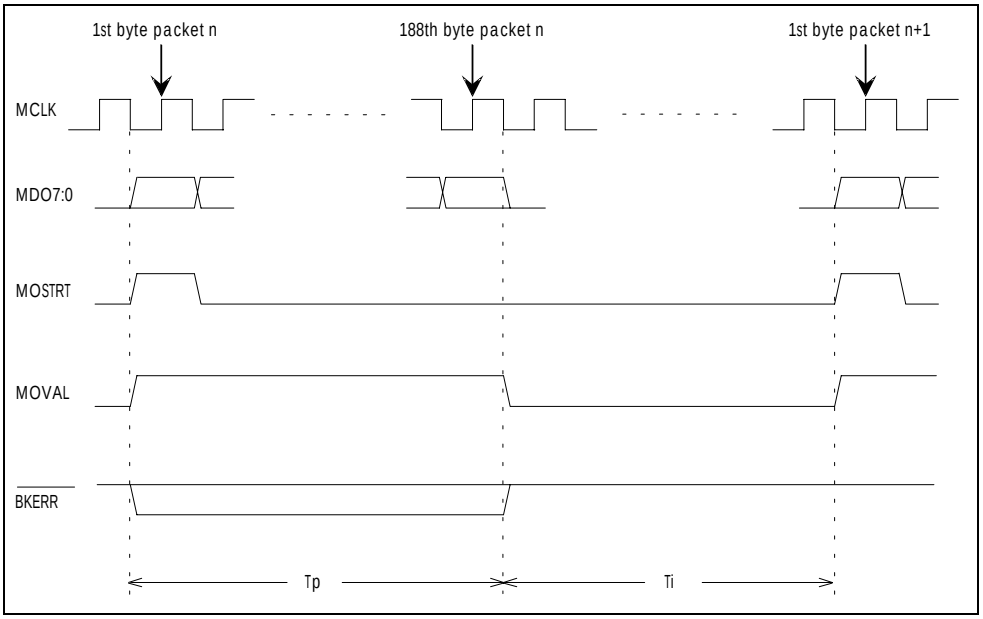


Fig. 24. VP305/6 output data wave form diagram.

MCLK will be a continuously running clock once symbol lock has been achieved in the QPSK block and is derived from the symbol clock.

MCLK is the output interface byte rate clock, running at a rate given by the table on page 70. The maximum jitter in the packet synchronisation byte is limited to one output clock period.

All output data and signals (MDO7:0, MOSTRT, MOVAL, $\overline{\text{BKERR}}$) change on the negative edge of MCLK to present stable data and signals on the positive edge of the clock.

A complete packet of data is output on MDO7:0 on 188 consecutive clocks and the MDO7:0 pins will remain low during the inter packet gaps.

MOSTRT goes high for the first byte clock of a packet.

MOVAL will go high on the first byte of a packet and remain high until the 188th byte has been clocked out.

$\overline{\text{BKERR}}$ will go low on the first byte of a packet where uncorrectable bytes are detected and remain low until the 188th byte has been clocked out.

Tp is equivalent to 188 clock cycles irrespective of the code rate.
Ti depends on the inner code rate (1/2, 2/3, 3/4, 5/6 or 7/8).

The following table shows data output timing and an example of the data rate on MDO7:0 for a maximum input symbol rate (Rs) of 30Msym/sec.

Viterbi Code rate	t_{CLKP} µs	t_{CLKH} µs	t_{CLKL} µs	e.g. MDO7:0 MByte/sec
1/2	16/2Rs	8/2Rs	8/2Rs	3.7500
2/3	12/2Rs	6/2Rs	6/2Rs	5.0000
3/4	11/2Rs	6.2Rs	5/2Rs	5.4545
5/6	10/2Rs	5/2Rs	5/2Rs	6.0000
7/8	9/2Rs	5/2Rs	4/2Rs	6.6667

Table 17. MPEG data output rates.

The Viterbi code rate is programmed in the VIT_MODE register, see page 47.

5.2. Data output timing.

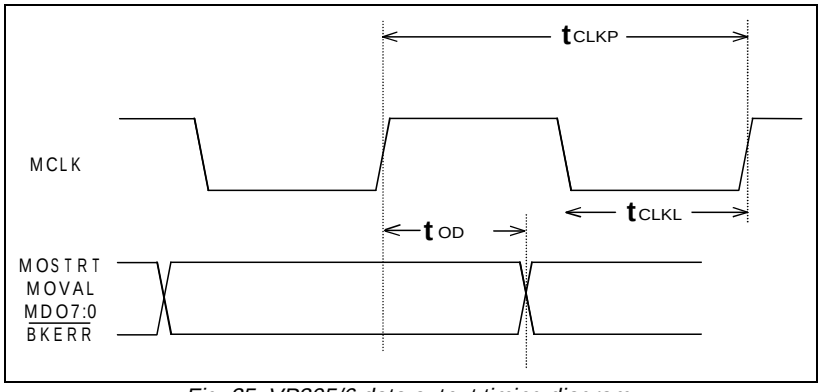


Fig. 25. VP305/6 data output timing diagram.

Parameter	Symbol	Min.	Typ.	Max.	Units
Data output delay	tOD			±20	ns

6. VP305/6 OPERATING CONDITIONS.

6.1. Recommended operating conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	V_{DD}	2.97	3.30	3.63	V
Power supply current	I_{DD}		410		mA
Input clock frequency [1]	$\overline{XTI}$	9.99		16.00	MHz
PSCAL input frequency	PSCAL		15.00	25.00	MHz
Sytem clock input frequency	SYS_CLK			60.00	MHz
SCL clock frequency	f_{SCL}			450	kHz
Ambient operating temperature		0		70	°C

Table 18. Recommended operating conditions.

Note 1. When not using a crystal, $\overline{XTI}$ may be driven from an external source over the frequency range shown.

6.2. Electrical characteristics.

Test conditions (unless otherwise stated): As specified in Recommended Operating Conditions.

DC CHARACTERISTICS

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Units
Digital Inputs CMOS compatible						
Input high voltage		V_{IH}	0.8V_{DD}		5.5	V
Input low voltage		V_{IL}			0.2V_{DD}	V
Digital Inputs TTL compatible						
Input high voltage		V_{IH}	2.0		5.5	V
Input low voltage		V_{IL}			0.8	V
Leakage current - All inputs except TEST1,2,3, XTI						
Input high	V_{IN} = 5.5V	I_{IH}		1	10	µA
Input low	V_{IN} = V_{SS}	I_{IL}		1	-10	µA
Leakage current - TEST1,2,3, XTI						
Input high	V_{IN} = 3.63V	I_{IH}		1	10	µA
Input low	V_{IN} = V_{SS}	I_{IL}		1	-10	µA
Digital Outputs CMOS compatible						
Output high voltage	I_{OH} = -1mA	VOH	0.8V_{DD}			V
Output low voltage	I_{OL} = +1mA	VOL			0.4	V
Digital Outputs Open drain						
Output high voltage		VOH			5.5	V
Output low voltage	I_{OL} = +6mA	VOL			0.4	V
PECL Inputs Common mode						
Input range	@ V_{DD}	V_{IR}	V_{DD}-1.9		V_{DD}-0.4	V
Input voltage swing		V_{IS}	250			mV

Table 19. DC Characteristics.

6.3. Crystal specification.

Parallel resonant fundamental frequency (preferred)	9.99 to 16.00MHz.
Tolerance over operating temperature range	± 25ppm.
Tolerance overall	± 50ppm.
Nominal load capacitance	30pF.
Equivalent series resistance	<35Ω

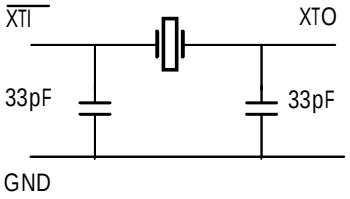


Fig. 26. Crystal oscillator circuit.

6.4. Absolute maximum ratings.

Supply voltage	-0·3V to +3.63V
All 5V compatible inputs	-0·3V to 5V+0·3VV_{DD}
All 3.3V compatible inputs	-0·3V to V_{DD}+0·3V
Operating temperature	0°C to +70°C
Storage temperature	-65°C to 150°C

Note: Stresses exceeding these listed under Absolute Maximum Ratings may induce failure. Exposure to Absolute Maximum Ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

6.5. Pinout description.

Pin No	Name	Pin Description	I/O	Note	V	mA
1	$\overline{\text{SER}}$	A logic 1 selects the 8 bit interface, a logic 0 selects I²C interface. Not connected on VP305.	I	CMOS	5	
4	PSCAL	Input from SL1710 (differential prescaler true output).	I	PECL	δ1	
5	$\overline{\text{PSCAL}}$	Input from SL1710 (differential prescaler inverted output).	I	PECL	δ1	
6-11	IIN5:0	In phase data input from the ADC digitiser.	I	TTL	5	
14-19	QIN5:0	Quadrature phase data input from the ADC digitiser. Input format is selected by bit CONFIG[0].	I	TTL	5	
22	SYS_CLK	System clock input.	I	TTL	5	
23	$\overline{\text{AS}}$	Address select strobe. The address on pins A2:0 is latched on the negative going edge.	I	CMOS	5	
24	$\overline{\text{CS}}$	Chip select for the microprocessor interface, a logic 0 makes the interface active. Data on pins D7:0 is latched on the positive going edge.	I	CMOS	5	
25-27	A2:0	Address pins for the internal registers used with the 8 bit interface.	I	CMOS	5	
30	$\overline{\text{DTACK}}$	Data acknowledge. A logic 0 indicates data has been transferred.	O	Open drain	5	6
31	R/$\overline{\text{W}}$	A logic 1 indicates a read operation, a logic 0 a write operation.	I	CMOS	5	
32	$\overline{\text{IRQ}}$	A low output on this pin indicates an event has occurred and the microprocessor should read the interrupt registers. A read of both interrupt registers resets this pin.	O	Open drain	5	6
33,35-39, 42-43	D7:0	Data port for read or write data. D0 = SCL Clock input for I²C when $\overline{\text{SER}}$ = logic 0.	I/O	Open drain	5	6
44	SDA	Data I/O pin for I²C. Not available on VP305 version.	I/O	Open drain	5	6
45	RESET	Active HIGH reset input, with 100k pull down resistor.	I	CMOS	5	
48	XTO	Crystal output. An internal feedback resistor to $\overline{\text{XTI}}$ is included.	O	CMOS	3.3	
49	$\overline{\text{XTI}}$	Crystal clock input or external reference clock input for QPSK block.	I	CMOS	3.3	
50	STATUS	Output pin for various functions selected by register bits.	O	CMOS	3.3	1
51	MCLK	MPEG clock output at the data byte rate.	O	Tri-state	3.3	1
63-60, 57-54	MDO7:0	MPEG transport packet data output bus.	O	Tri-state	3.3	1
64	$\overline{\text{MDOEN}}$	Logic 1 = MPEG data and clock outputs disable - tristate. Logic 0 = MPEG data and clock outputs enable.	I	CMOS	5	

Pin No	Name	Pin Description	I/O	Note	V	mA

67	MOVAL	MPEG data output valid. This pin is high during the MCLK clock cycles when valid data bytes are being output.	O	Tri-state	3.3	1
68	$\overline{\text{BKERR}}$	Flag for packets which have uncorrectable byte errors. The pin goes low for the whole of the packet containing uncorrectable errors.	O	Tri-state	3.3	1
69	MOSTRT	MPEG output start signal, high on the first byte of a packet.	O	Tri-state	3.3	1
75	TEST1	For factory test only. This pin must be connected to VSS in normal operation.	I	CMOS	3.3	
76	VERR	Viterbi error indication.	O	Tri-state	3.3	1
77	TEST2	For factory test only. This pin must be connected to VSS in normal operation.	I	CMOS	3.3	
80	GPP0	General purpose port input. Controlled by the GPP register.	I	CMOS	5	
84-81	GPP4:1	General purpose port outputs. Controlled by the GPP register.	O	Open drain	5	6
87	AGC_OUT	Sigma Delta modulated AGC true output. A logic 0 = minimum gain.	O	Open drain	5	6
88	CR_VCO2D	Carrier VCO positive feedback output 2 down. A logic 1 decreases and a logic 0 increases the carrier VCO frequency.	O	Tri-state	3.3	1
89	CR_VCO1D	Carrier VCO positive feedback output 1 down. A logic 1 decreases and a logic 0 increases the carrier VCO frequency.	O	Tri-state	3.3	1
90	CR_VCO2U	Carrier VCO positive feedback output 2 up. A logic 1 increases and a logic 0 decreases the carrier VCO frequency.	O	Tri-state	3.3	1
91	CR_VCO1U	Carrier VCO positive feedback output 1 up. A logic 1 increases and a logic 0 decreases the carrier VCO frequency.	O	Tri-state	3.3	1
96	SYM_VCOU	Symbol pulse width modulated true output. A logic 1 increases and a logic 0 decreases the symbol VCO frequency.	O	Tri-state	3.3	1
97	SYM_VCOD	Symbol pulse width modulated inverted output. A logic 1 decreases and a logic 0 increases the symbol VCO frequency.	O	Tri-state	3.3	1
100	TEST3	For factory test only. This pin must be connected to VSS in normal operation.	I	CMOS	3.3	

Pin No	Name	Pin Description	I/O	Note	V	mA
2,12,20, 28,34,41, 47,53,59, 65,70,74, 78,86,93, 98	VDD	+3.3V power supply. All pins must be connected.				
3,13,21, 29,40,46, 52,58,66, 72,79,85, 92,99	VSS	0V power ground. All pins must be connected.				

Table 20. Pinout details.

The remaining pins 71, 73, 94 and 95 are N/C - not connected internal to the VP305/6. They may be connected external to the VP305/6.

6.6. Alphabetical listing of the pinout.

FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN
A0	27	IIN0	11	QIN0	19	VDD	47
A1	26	IIN1	10	QIN1	18	VDD	53
A2	25	IIN2	9	QIN2	17	VDD	59
AGC_OUT	87	IIN3	8	QIN3	16	VDD	65
$\overline{AS}$	23	IIN4	7	QIN4	15	VDD	70
$\overline{BKERR}$	68	IIN5	6	QIN5	14	VDD	74
CR_VCO1D	89	$\overline{IRQ}$	32	R/ $\overline{W}$	31	VDD	78
CR_VCO2D	88	MCLK	51	RESET	45	VDD	86
CR_VCO1U	91	MDO0	54	SDA	44	VDD	93
CR_VCO2U	90	MDO1	55	$\overline{SER}$	1	VDD	98
$\overline{CS}$	24	MDO2	56	STATUS	50	VERR	76
D0 (SCL)	43	MDO3	57	SYM_VCOD	97	VSS	3
D1	42	MDO4	60	SYM_VCOU	96	VSS	13
D2	39	MDO5	61	SYS_CLK	22	VSS	21
D3	38	MDO6	62	TEST1	75	VSS	29
D4	37	MDO7	63	TEST2	77	VSS	40
D5	36	$\overline{MDOEN}$	64	TEST3	100	VSS	46
D6	35	MOSTRT	69	$\overline{XTI}$	48	VSS	52
D7	33	MOVAL	67	XTO	49	VSS	58
$\overline{DTACK}$	30	N/C	71	VDD	2	VSS	66
GPP0	80	N/C	73	VDD	12	VSS	72
GPP1	81	N/C	94	VDD	20	VSS	79
GPP2	82	N/C	95	VDD	28	VSS	85
GPP3	83	PSCAL	4	VDD	34	VSS	92
GPP4	84	$\overline{PSCAL}$	5	VDD	41	VSS	99

Table 21. Alphabetical listing of the pinout.

6.7. Numerical listing of the pinout.

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{SER}}$	26	A1	51	MCLK	76	VERR
2	VDD	27	A0	52	VSS	77	TEST2
3	VSS	28	VDD	53	VDD	78	VDD
4	PSCAL	29	VSS	54	MDO0	79	VSS
5	$\overline{\text{PSCAL}}$	30	$\overline{\text{DTACK}}$	55	MDO1	80	GPP0
6	IIN5	31	R/ $\overline{\text{W}}$	56	MDO2	81	GPP1
7	IIN4	32	$\overline{\text{IRQ}}$	57	MDO3	82	GPP2
8	IIN3	33	D7	58	VSS	83	GPP3
9	IIN2	34	VDD	59	VDD	84	GPP4
10	IIN1	35	D6	60	MDO4	85	VSS
11	IIN0	36	D5	61	MDO5	86	VDD
12	VDD	37	D4	62	MDO6	87	AGC_OUT
13	VSS	38	D3	63	MDO7	88	CR_VCO2D
14	QIN5	39	D2	64	$\overline{\text{MDOEN}}$	89	CR_VCO1D
15	QIN4	40	VSS	65	VDD	90	CR_VCO2U
16	QIN3	41	VDD	66	VSS	91	CR_VCO1U
17	QIN2	42	D1	67	MOVAL	92	VSS
18	QIN1	43	D0 (SCL)	68	$\overline{\text{BKERR}}$	93	VDD
19	QIN0	44	SDA	69	MOSTRT	94	N/C
20	VDD	45	RESET	70	VDD	95	N/C
21	VSS	46	VSS	71	N/C	96	SYM_VCOU
22	SYS_CLK	47	VDD	72	VSS	97	SYM_VCOD
23	$\overline{\text{AS}}$	48	$\overline{\text{XTI}}$	73	N/C	98	VDD
24	$\overline{\text{CS}}$	49	XTO	74	VDD	99	VSS
25	A2	50	STATUS	75	TEST1	100	TEST3

Table 22. Numerical listing of the pinout.

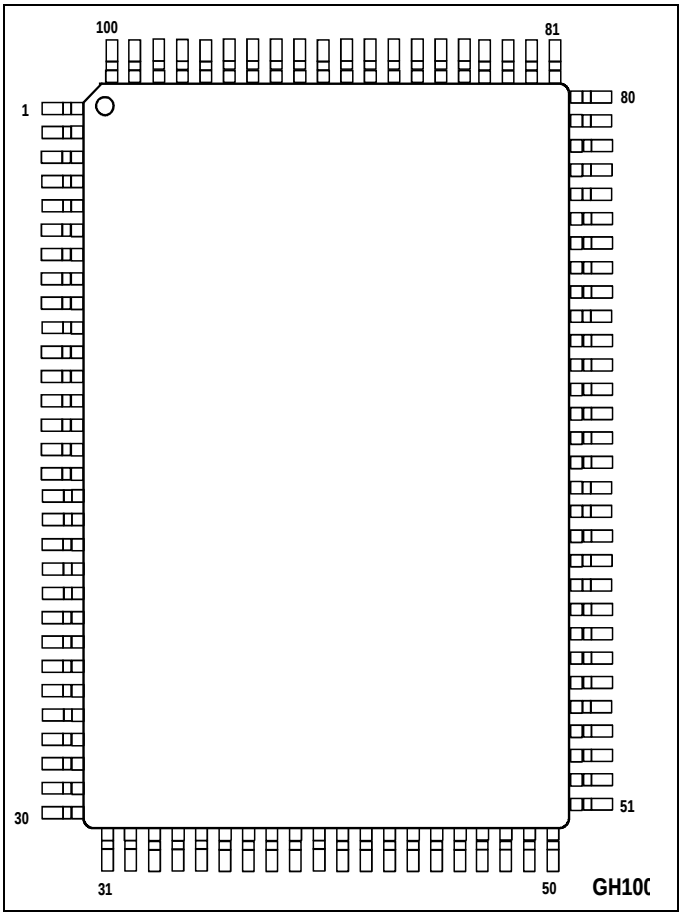


Fig. 27. Pin connections - top view.

7. REFERENCES.

1. European Digital Video Broadcast Standard, ETS 300 421 December 1994.
ETS Secretariat
06921 Sophia Antipolis Cedex
France.

2. Purchase of Mitel I²C components conveys a licence under the Philips I²C Patent Rights to use these components in I²C systems, provided that the systems conform to the I²C Standard Specification as defined by Philips.

8. APPENDIX 1: FEATURES

GENERAL
- Conforms to EBU specification for DVB-S.
- Parallel 8 bit or I²C bus microprocessor interface.

DEMODULATOR
- BPSK or QPSK selectable.
- Variable Symbol data rate from 5 to 30MSym/sec.
- Decimation filter with over sampling ratios of 2, 3, 4.
- ADC Decimation ratios of 1, 2, 4, 8, 16.

VITERBI
- Selectable decoder rates 1/2, 2/3, 3/4, 5/6, 7/8.
- 3 bit soft decision decoder input from QPSK.
- Constraint length k=7.
- Trace back depth 128.
- On chip error rate monitor.

SYNCHRONISATION CONTROL
- Automatic synchronisation.

DE-INTERLEAVER
- Forney with depth 12.

REED SOLOMON
- Conforms to EBU specification.

DESCRAMBLER
- EBU specification Descrambler.

Ordering information.
VP306 S / CG / GP1N.

9. APPENDIX 2: LOCK ACQUISITION ALGORITHM.

9.1. Pre conditions.

Set the frequency sweep limits in CR_USWL and CR_LSWL registers, also the reference period CR_RP, see page 12. Set the carrier threshold CR_THSL = 72 and the carrier sweep rate CR_SWR = 150.

9.2. Lock acquisition algorithm.

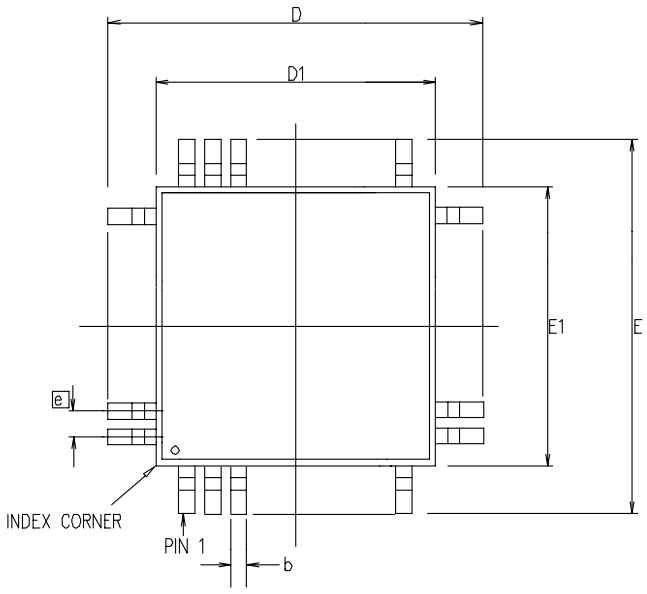
The Symbol loop phase lock acquisition is automatically handled in the VP305/6. It is initiated by turning on the carrier sweep function with the carrier loop open. The NDAML carrier phase detector is enabled. These three items are selected in CR_CONFIG[2:0] register 30. Next the carrier loop is closed and a program loop started to detect when lock occurs.

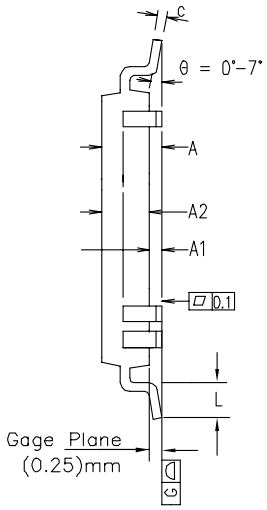
The carrier phase lock acquisition is indicated in the STATUS register (3) by CR_LC (bit 1) going high. When this event occurs, the carrier sweep is turned off. The lock condition is checked five times to ensure it is stable then the program loop is exited.

Example of pseudo code fragment (using decimal number representation):

```
Write CR_CONFIG = 39 to register address 30. (Sweep on, Loop open, NDAML)
Write CR_CONFIG = 37 to register address 30. (Sweep on, Loop closed, NDAML)
Initialise variables:          TREND = 0, A_FLAG = 0,
Loop:  For A_LOOP = 0 to 200 Do
            LOOP_STAT = read CR_LC from STATUS[1] register address 3.
            If LOOP_STAT = 1 Then
                  TREND = TREND + 1
                  Write CR_CONFIG = 36 to register address 30.
                                                (Sweep off, Loop closed, NDAML)
                  If TREND > 5 Then
                        A_FLAG = 1
                        GOTO EX_ACQ
                  End If
            End If
            If LOOP_STAT = 0 Then
                  TREND = 0
            End If
      Next A_LOOP
EX_ACQ: sucess
```

If sucessful, the loop exits with A_FLAG = 1, otherwise, A_FLAG = 0.





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	3.40		–	0.134
A1	0.25	0.50		0.010	0.020
A2	2.50	2.90		0.098	0.114
D	23.20 BSC			0.913 BSC	
D1	20.00 BSC			0.787 BSC	
E	17.20 BSC			0.677 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.73	1.03		0.029	0.041
e	0.65 BSC.			0.026 BSC.	
b	0.22	0.40		0.009	0.016
c	0.11	0.23		0.004	0.009
	Pin features				
N	100				
ND	30				
NE	20				
NOTE	RECTANGULAR				

Conforms to JEDEC MS–022 GC–1 Iss. B

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.010 mm max.

ORIGINATING SITE: SWINDON

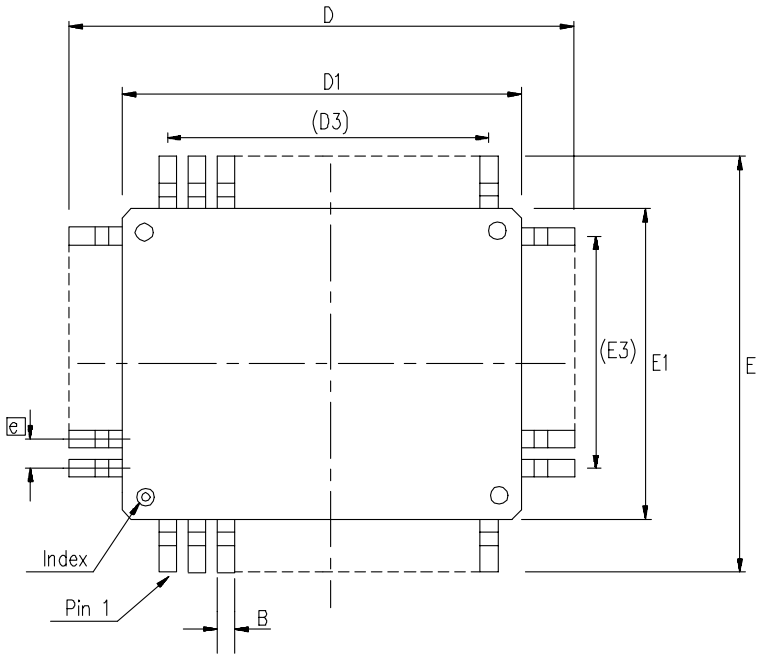
ISSUE	1	2	3		
ACN	202054	207072	207319		
DATE	20FEB97	5JUL99	24AUG99		
APPRD.					

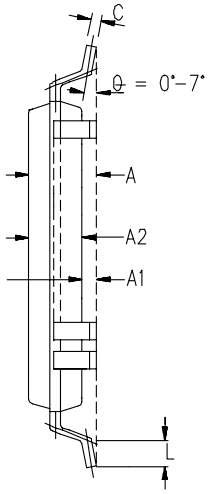
MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 100L MQFP (GP) (14x20x2.8) mm, Body+3.2 mm

Drawing Number

GPD00305





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	3.10		---	0.122
A1	0.10	0.36		0.004	0.014
A2	2.57	2.87		0.101	0.113
D	23.65	24.15		0.931	0.951
D1	19.90	20.10		0.783	0.791
D3	18.85 REF			0.742 REF	
E	17.65	18.15		0.695	0.715
E1	13.90	14.10		0.547	0.555
E3	12.35 REF			0.486 REF	
L	0.65	0.95		0.026	0.037
e	0.65 BSC			0.026 BSC	
B	0.22	0.38		0.009	0.015
C	0.13	0.23		0.005	0.009
	Pin features				
N	100				
ND	30				
NE	20				
NOTE	RECTANGULAR				

NOTES: –
1. Controlling dimensions are in MM.
2. Maximum allowable die thickness to be assembled in this pkg. family is 0.51(0.020") millimeters.
3. This document supersedes 418/ED/51699/003 issue 1

ORIGINATING SITE: Swindon

ISSUE	1					MITEL SEMICONDUCTOR
ACN	207464					
DATE	10SEP99					
APPRD.						

Title: Outline Drawing for 100 Lead PQUAD2 (GH) (14 x 20)mm Body+3.9mm

Drawing Number
GPD00600

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