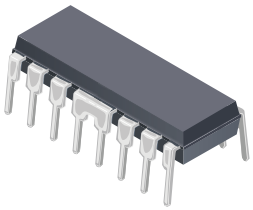
Full-Bridge PWM Microstepping Motor Driver

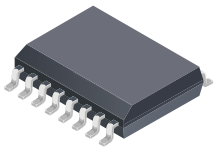
Features and Benefits

- ±1.5 A continuous output current
- 50 V output voltage rating
- Internal PWM current control
- 3-bit nonlinear DAC
- Fast, mixed fast/slow, and slow current-decay modes
- Internal thermal shutdown circuitry
- Crossover-current and UVLO protection

Packages:



Package B, 16-pin DIP
with exposed tabs



Package LB, 16-pin SOIC
with internally fused pins

Not to scale

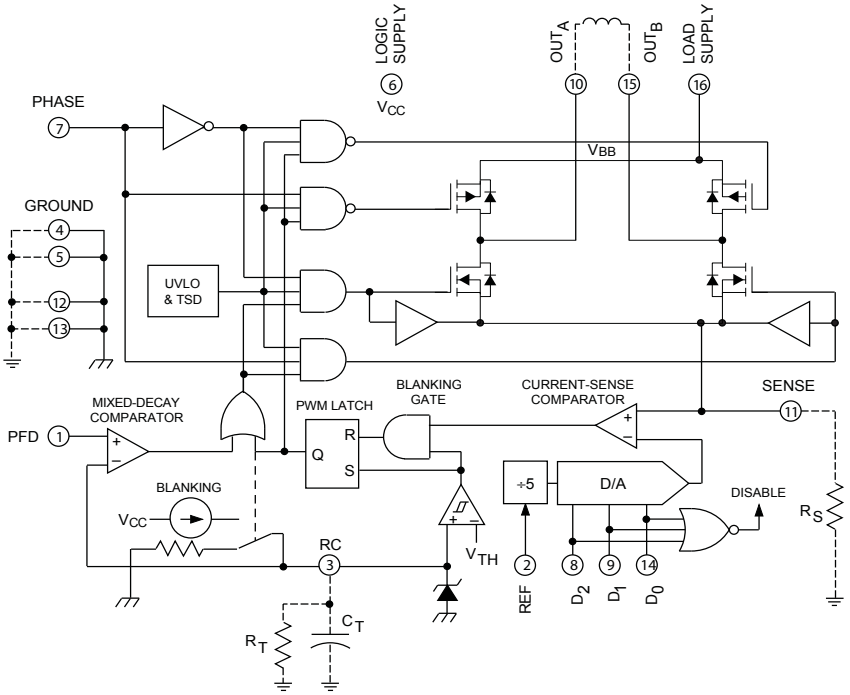
Description

The A4975 is designed to drive one winding of a bipolar stepper motor in a microstepping mode. The outputs are rated for continuous output currents to ±1.5 A and operating voltages to 50 V. Internal pulse width modulated (PWM) current control combined with an internal three-bit nonlinear digital-to-analog converter allows the motor current to be controlled in full-, half-, quarter-, or eighth-step (microstepping) modes. Nonlinear increments minimize the number of control lines necessary for microstepping. Microstepping provides increased step resolution, and reduces torque variations and resonance problems at low speed.

Internal circuitry determines whether the PWM current-control circuitry operates in a slow (recirculating) current-decay mode, fast (regenerative) current-decay mode, or in a mixed current-decay mode in which the off-time is divided into a period of fast current decay and with the remainder of the fixed off-time spent in slow current decay. The combination of user-selectable current-sensing resistor and reference voltage, digitally selected output current ratio; and slow, fast, or mixed current-decay modes provides users with a broad, variable range of motor control.

Continued on the next page…

Functional Block Diagram



Description (continued)

Internal circuit protection includes thermal shutdown with hysteresis, an undervoltage monitor, and crossover-current protection. Special power-up sequencing is not required.

The A4975 is supplied in a choice of two power packages; a 16-pin dual-in-line plastic package with copper heat-sink tabs (suffix 'B'), and a 16-lead plastic SOIC with internally fused pins (suffix 'LB'). For both package styles, the thermally enhanced pins are at ground potential and need no electrical isolation. Both packages are lead (Pb) free, with leadframe plating 100% matte tin.

Selection Guide

Part Number	Packing	Package
A4975SB-T	16-pin DIP with exposed thermal tabs	25 per tube
A4975SLBTR-T	16-pin SOICW with internally fused pins	1000 per reel

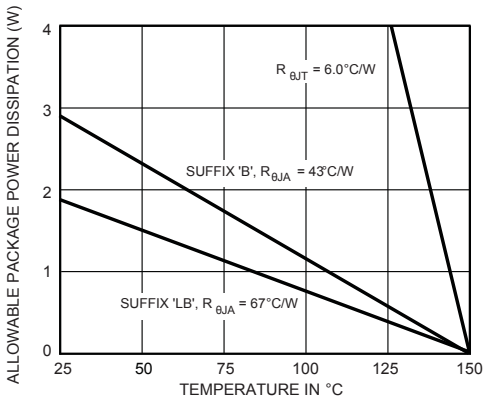
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}		50	V
Logic Supply Voltage	V_{CC}		6	V
Logic/Reference Input Voltage Range	V_{IN}		–0.3 to 6	V
Sense Voltage	V_S		0.5	V
Output Current, Continuous	I_{OUT}	Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.	±1.5	A
Package Power Dissipation	P_D		See graph	W
Operating Ambient Temperature	T_A	Range S	–20 to 85	°C
Maximum Junction Temperature	T_J(max)	Fault conditions that produce excessive junction temperature will activate the device's thermal shutdown circuitry. These conditions can be tolerated but should be avoided.	150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	B Package, single-layer PCB, 1 in² 2-oz. exposed copper	43	°C/W
		LB Package, 2-layer PCB, 0.3 in² 2-oz. exposed copper each side	67	°C/W
Package Thermal Resistance, Junction to Tab	$R_{\theta JT}$		6	°C/W

*Additional thermal information available on Allegro website.



Allegro MicroSystems, Inc.
115 Northeast Cutoff
Worcester, Massachusetts 01615-0036 U.S.A.
1.508.853.5000; www.allegromicro.com

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = 4.5 to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Outputs						
Load Supply Voltage Range	V_{BB}	Operating	5	—	50	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	—	<1.0	50	µA
		V_{OUT} = 0 V	—	<-1.0	-50	µA
Output Resistance	R_{DS}	Total Sink + Source, I_{OUT} = 1.5 A, V_{BB} > 8 V, T_J = 25°C	—	1	1.4	Ω
Motor Supply Current (No Load)	$I_{BB(ON)}$	$D_0 = D_1 = D_2 = V_{IN(1)}$	—	500	700	µA
	$I_{BB(OFF)}$	$D_0 = D_1 = D_2 = V_{IN(0)}$	—	250	500	µA
Control Circuitry						
Logic Supply Voltage Range	V_{CC}	Operating	4.5	5.0	5.5	V
Reference Voltage Range	V_{REF}	Operating	0.5	—	2.5	V
UVLO Enable Threshold		V_{CC} = 0 → 5 V	3.35	3.7	4.05	V
UVLO Hysteresis			0.3	0.45	0.6	V
Logic Supply Current	$I_{CC(ON)}$	$D_0 = D_1 = D_2 = V_{IN(1)}$	—	2.7	—	mA
	$I_{CC(OFF)}$	$D_0 = D_1 = D_2 = V_{IN(0)}$	—	2.7	—	mA
Logic Input Voltage	$V_{IN(1)}$		V_{CC} × 0.55	—	—	V
	$V_{IN(0)}$		—	—	V_{CC} × 0.27	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{CC}$ = 5 V	—	0	–10	µA
	$I_{IN(0)}$	V_{IN} = 0 V, V_{CC} = 5 V	—	–106	–200	µA
Mixed-Decay Comparator Trip Points	V_{PFD}	Slow Current-Decay Mode	3.5	—	—	V
		Mixed Current-Decay Mode	1.1	—	3.1	V
		Fast Current-Decay Mode	—	—	0.8	V
Mixed-Decay Comparator Input Offset Voltage	$V_{IO(PFD)}$		—	0	±50	mV
Mixed-Decay Comparator Hysteresis	$\Delta V_{IO(PFD)}$		5	25	55	mV
Reference Input Current	I_{REF}	V_{REF} = 0.5 to 2.5 V	—	—	±5.0	µA
Reference Divider Ratio	V_{REF}/V_S	At trip, $D_0 = D_1 = D_2 = V_{IN(1)}$	—	5	—	—
Digital-to-Analog Converter Accuracy*	—	1.0 V < V_{REF} ≤ 2.5 V	—	—	±3.0	%
		0.5 V ≤ V_{REF} ≤ 1.0 V	—	—	±4.0	%

Continued next page…

ELECTRICAL CHARACTERISTICS (continued) at T_A = 25°C, V_{CC} = 4.5 to 5.5 V (unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Control Circuitry (cont'd)						
Current-Sense Comparator Input Offset Voltage*	$V_{IO(S)}$	V_{REF} = 0 V	—	—	±5.0	mV
Step Reference Current Ratio	SRCR	$D_0 = D_1 = D_2 = V_{IN(0)}$	—	0	—	%
		$D_0 = V_{IN(1)}$, $D_1 = D_2 = V_{IN(0)}$	—	19.5	—	%
		$D_0 = V_{IN(0)}$, $D_1 = V_{IN(1)}$, $D_2 = V_{IN(0)}$	—	38.2	—	%
		$D_0 = D_1 = V_{IN(1)}$, $D_2 = V_{IN(0)}$	—	55.5	—	%
		$D_0 = D_1 = V_{IN(0)}$, $D_2 = V_{IN(1)}$	—	70.7	—	%
		$D_0 = V_{IN(1)}$, $D_1 = V_{IN(0)}$, $D_2 = V_{IN(1)}$	—	83.1	—	%
		$D_0 = V_{IN(0)}$, $D_1 = D_2 = V_{IN(1)}$	—	92.4	—	%
		$D_0 = D_1 = D_2 = V_{IN(1)}$	—	100	—	%
Thermal Shutdown Temp.	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	15	—	°C
AC Timing						
PWM RC Fixed Off-time	t_{OFFRC}	C_T = 470 pF, R_T= 43 kΩ	18.2	20.2	22.3	µs
PWM Minimum On Time	$t_{ON(min)}$	V_{CC} = 5.0 V, $R_T \geq$ 43 kΩ, C_T = 470 pF, I_{OUT} = 100 mA	0.8	1.6	2.2	µs

* The total error for the V_{REF}/V_S function is the sum of the D/A error and the current-sense comparator input offset voltage.

Table 1 — PHASE Truth Table

PHASE	OUT_A	OUT_B
H	H	L
L	L	H

Table 2 — PFD Truth Table

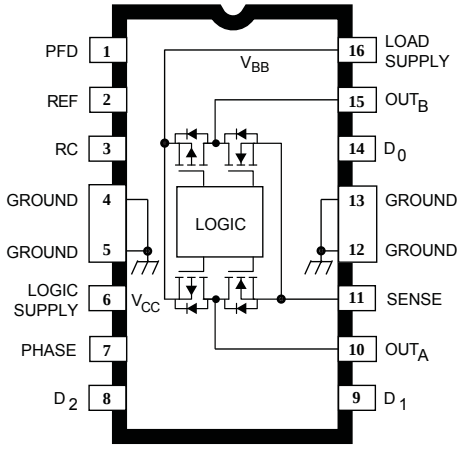
V_{PFD}	Description
≥3.5 V	Slow Current-Decay Mode
1.1 V to 3.1 V	Mixed Current-Decay Mode
≤0.8 V	Fast Current-Decay Mode

Table 3 — DAC Truth Table

DAC DATA D_2	D_1	D_0	Current Ratio, %	V_{REF}/V_S
H	H	H	100	5.00
H	H	L	92.4	5.41
H	L	H	83.1	6.02
H	L	L	70.7	7.07
L	H	H	55.5	9.01
L	H	L	38.2	13.09
L	L	H	19.5	25.64
L	L	L	All Outputs Disabled	

where $V_S = I_{TRIP} \times R_S$. See Applications section.

Note the A4975SB (DIP) and the A4975SLB (SOIC) are electrically identical and share a common terminal number assignment.



Terminal Functions

Terminal	Name	Description
1	PFD	(Percent Fast Decay) The analog input used to set the current-decay mode.
2	REF	(V_{REF}) The voltage at this input (along with the value of R_S and the states of DAC inputs D_0, D_1, and D_2) set the peak output current.
3	RC	The parallel combination of external resistor R_T and capacitor C_T set the off time for the PWM current regulator. C_T also sets the blanking time.
4-5	GROUND	Return for the logic supply (V_{CC}) and load supply (V_{BB}); the reference for all voltage measurements.
6	LOGIC SUPPLY	(V_{CC}) Supply voltage for the logic circuitry. Typically = 5 V.
7	PHASE	The PHASE input determines the direction of current in the load.
8	D_2	($DATA_2$) One-of-three (MSB) control bits for the internal digital-to-analog converter.
9	D_1	($DATA_1$) One-of-three control bits for the internal digital-to-analog converter.
10	OUT_A	One-of-two output load connections.
11	SENSE	Connection to the sink-transistor emitters. Sense resistor R_S is connected between this point and ground.
12-13	GROUND	Return for the logic supply (V_{CC}) and load supply (V_{BB}); the reference for all voltage measurements.
14	D_0	($DATA_0$) One-of-three (LSB) control bits for the internal digital-to-analog converter.
15	OUT_B	One-of-two output load connections.
16	LOAD SUPPLY	(V_{BB}) Supply voltage for the load.

Functional Description

Two A4975 full-bridge PWM microstepping motor drivers are needed to drive the windings of a bipolar stepper motor. Internal pulse width modulated (PWM) control circuitry regulates each motor winding current. The peak motor current is set by the value of an external current-sense resistor (R_S), a reference voltage (V_{REF}), and the digital-to-analog converter (DAC) data inputs (D_0, D_1, and D_2).

To improve motor performance, especially when using sinusoidal current profiles necessary for microstepping, the A4975 has three distinct current-decay modes: slow decay, fast decay, and mixed decay.

PHASE Input. The PHASE input controls the direction of current flow in the load (table 1). An internally generated dead time of approximately 500 ns prevents crossover currents that could occur when switching the PHASE input.

DAC Data Inputs (D_0, D_1, D_2). A non-linear DAC is used to digitally control the output current. The output of the DAC is used to set the trip point of the current-sense comparator. Table 3 shows DAC output voltages for each input condition. When D_0, D_1, and D_2 are all logic low, all of the power output transistors are turned off.

Internal PWM Current Control. Each motor driver contains an internal fixed off-time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink transistors are enabled and current flows through the motor winding and R_S (figure 1). When the voltage across the sense resistor equals the DAC output voltage the current-sense comparator resets the PWM latch, which turns off the source drivers (slow-decay mode) or the sink and source drivers (fast- or mixed-decay mode).

With the DAC data input lines at $V_{IN(1)}$ voltage, the maximum value of current limiting is set by the selection of R_S and V_{REF} with a transconductance function approximated by:

$$I_{TRIP} \approx V_{REF} / 5R_S.$$

The actual peak load current (I_{PEAK}) will be slightly higher than I_{TRIP} due to internal logic and switching delays. The driver(s) remain off for a time period determined by a user-selected external resistor-capacitor combination (R_TC_T). At the end of the fixed off-time, the driver(s) are re-enabled, allowing the load current to increase to I_{TRIP} again, maintaining an average load current.

The DAC data input lines are used to provide up to eight levels of output current. The internal 3-bit digital-to-analog converter reduces the reference input to the current-sense comparator in precise steps (the step reference current ratio or SRCR) to provide half-step, quarter-step, or "microstepping" load-current levels.

$$I_{TRIP} \approx SRCR \times V_{REF} / 5R_S$$

Slow Current-Decay Mode. When $V_{PFD} \geq 3.5$ V, the device is in slow current-decay mode (the source drivers are disabled when the load current reaches I_{TRIP}). During the fixed off-time, the load inductance causes the current to recirculate through the motor winding and sink drivers (see figure 1). Slow-decay mode produces low ripple current for a given fixed off-time (see figure 2). Low ripple current is desirable because the average current in the motor winding is more nearly equal to the desired reference value, resulting in increased motor

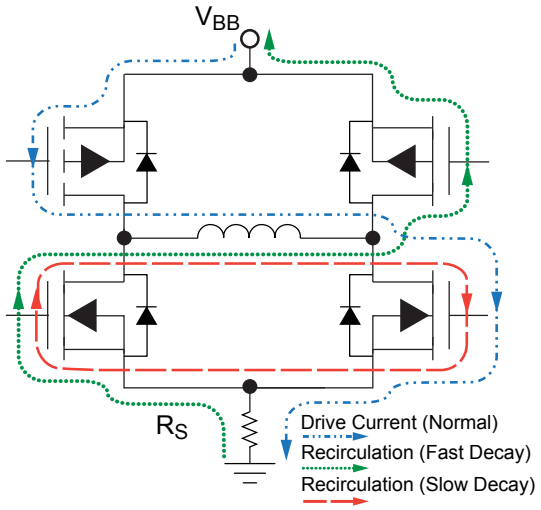


Figure 1 — Load-Current Paths

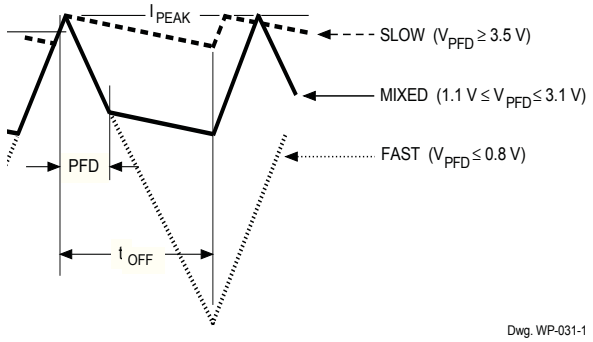


Figure 2 — Current-Decay Waveforms

performance in microstepping applications.

For a given level of ripple current, slow decay affords the lowest PWM frequency, which reduces heating in the motor and driver IC due to a corresponding decrease in hysteretic core losses and switching losses respectively. Slow decay also has the advantage that the PWM load current regulation can follow a more rapidly increasing reference before the PWM frequency drops into the audible range. For these reasons slow-decay mode is typically used as long as good current regulation can be maintained.

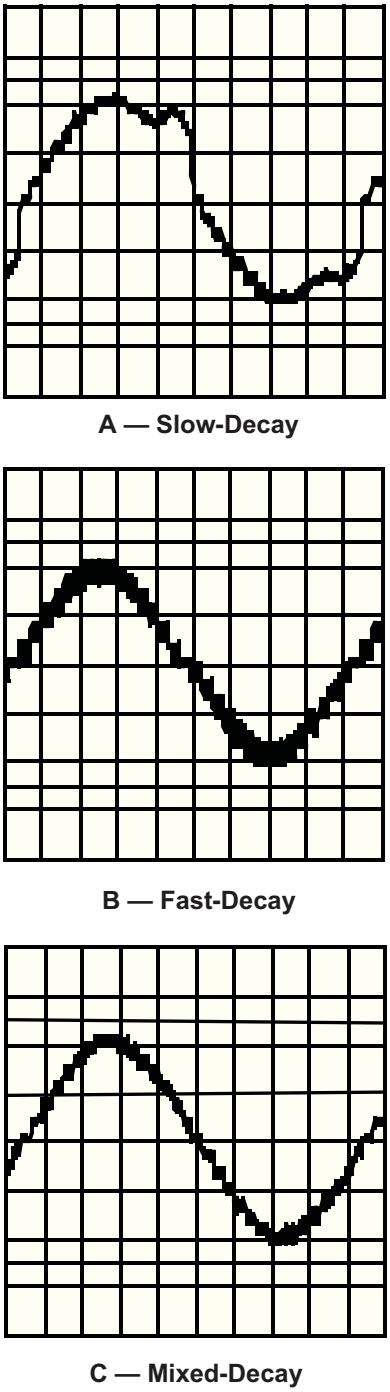
Under some circumstances slow-decay mode PWM can fail to maintain good current regulation:

1) The load current will fail to regulate in slow-decay mode due to a sufficiently negative back-EMF voltage in conjunction with the low voltage drop across the load during slow decay recirculation. The negative back-EMF voltage can cause the load current to actually increase during the slow decay off time. A negative back-EMF voltage condition commonly occurs when driving stepping motors because the phase lead of the rotor typically causes the back-EMF voltage to be negative towards the end of each step (see figure 3A).

2) When the desired load current is decreased rapidly, the slow rate of load current decay can prevent the current from following the desired reference value.

3) When the desired load current is set to a very low value, the current-control loop can fail to regulate due to its minimum duty cycle, which is a function of the user-selected value of t_{OFF} and the minimum on-time pulse width $t_{on(min)}$ that occurs each time the PWM latch is reset.

Fast Current-Decay Mode. When $V_{PFD} < 0.8$ V, the device is in fast current-decay mode (both the sink and source drivers are disabled when the load current reaches I_{TRIP}, and the opposite pair is turned on). During the fixed off-time, the load inductance causes the current to flow from ground to the load supply via the motor winding and the opposite pair of transistors (see figure 1). Because the full motor supply voltage is across the load during fast-decay recirculation, the rate of load current decay is rapid, producing a high ripple current for a given fixed off-time (see figure 2). This rapid rate of decay allows good current regulation to be maintained at the cost of decreased average current accuracy or increased driver and motor losses.



A — Slow-Decay

B — Fast-Decay

C — Mixed-Decay

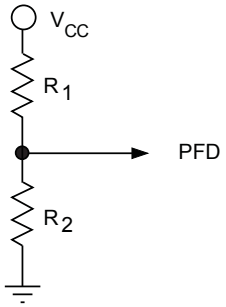
Figure 3 — Sinusoidal Drive Currents

Mixed Current-Decay Mode. If V_{PFD} is between 1.1 V and 3.1 V, the device will be in a mixed current-decay mode. Mixed-decay mode allows the user to achieve good current regulation with a minimum amount of ripple current and motor/driver losses by selecting the minimum percentage of fast decay required for their application (see also the Stepper Motor Applications section).

As in fast current-decay mode, mixed-decay starts with the sink and source drivers disabled and the opposite pair turned on after the load current reaches I_{TRIP}. When the voltage at the RC terminal decays to a value below V_{PFD}, the sink drivers are re-enabled, placing the device in slow current-decay mode for the remainder of the fixed off-time (figure 2). The percentage of fast decay (PFD) is user determined by V_{PFD} or two external resistors.

$$PFD = 100 \ln (0.6[R_1+R_2]/R_2)$$

where:



Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one-shot off-time, t_{OFF}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminal to ground. The off-time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ, is approximated by:

$$t_{OFF} \approx R_T C_T.$$

When the load current is increasing, but has not yet reached the sense-current comparator threshold (I_{TRIP}), the voltage on the RC terminal is approximately $0.6V_{CC}$. When I_{TRIP} is reached, the PWM latch is reset by the current-sense comparator and the voltage on the RC terminal will decay until it reaches approximately $0.22V_{CC}$. The PWM latch is then set, thereby re-enabling the driver(s) and allowing load current to increase again. The PWM cycle repeats, maintaining the peak load current at the desired value.

With increasing values of $t_{OFF,}$ switching losses will decrease, low-level load-current regulation will improve, EMI will be reduced, the PWM frequency will decrease, and ripple current will increase. A value of t_{OFF} can be chosen for optimization of these parameters. For applications where audible noise is a concern, typical values of t_{OFF} are chosen to be in the range of 15 to 35 µs.

RC Blanking. In addition to determining the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry (or by the PHASE input, or when the device is enabled with the DAC data inputs). The comparator output is blanked to prevent false over-current detections due to reverse recovery currents of the clamp diodes, and/or switching transients related to distributed capacitance in the load.

During internal PWM operation, at the end of the t_{OFF} time, the comparator's output is blanked and C_T begins to be charged from approximately $0.22V_{CC}$ by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$. The blanking time, t_{BLANK}, can be calculated as:

$$t_{BLANK} = R_T C_T \ln (R_T/[R_T – 3\ k\Omega]).$$

When a transition of the PHASE input occurs, C_T is discharged to near ground during the crossover delay time (the crossover delay time is present to prevent simultaneous conduction of the source and sink drivers). After the crossover delay, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$.

Similarly, when the device is disabled, via the DAC data inputs, C_T is discharged to near ground. When the device is re-enabled, C_T is charged by an internal current source of approximately 1 mA. The comparator output remains blanked until the voltage on C_T reaches approximately $0.6V_{CC}$. The blanking time, t_{BLANK}, can be calculated as:

$$t_{BLANK} = R_T C_T \ln ([R_T - 1.1\ k\Omega]/R_T - 3\ k\Omega).$$

The minimum recommended value for C_T is 470 pF ± 5 %. This value ensures that the blanking time is sufficient to avoid

false trips of the comparator under normal operating conditions. For optimal regulation of the load current, this value for C_T is recommended and the value of R_T can be sized to determine t_{OFF}.

Thermal Considerations. Thermal-protection circuitry turns off all output transistors when the junction temperature reaches approximately +165°C. This is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. The output transistors are re-enabled when the junction temperature cools to approximately +150°C.

Stepper Motor Applications. The A4975 is used to optimize performance in microstepping/sinusoidal stepper-motor drive applications (see figures 4 and 5). When the load current is increasing, the slow current-decay mode is used to limit the switching losses in the driver and iron losses in the motor. This also improves the maximum rate at which the load current can increase (as compared to fast decay) due to the slow rate of decay during t_{OFF}. When the load current is decreasing, the mixed current-decay mode is used to regulate the load current to the desired level. This prevents tailing of the current profile caused by the back-EMF voltage of the stepper motor (see figure 3A).

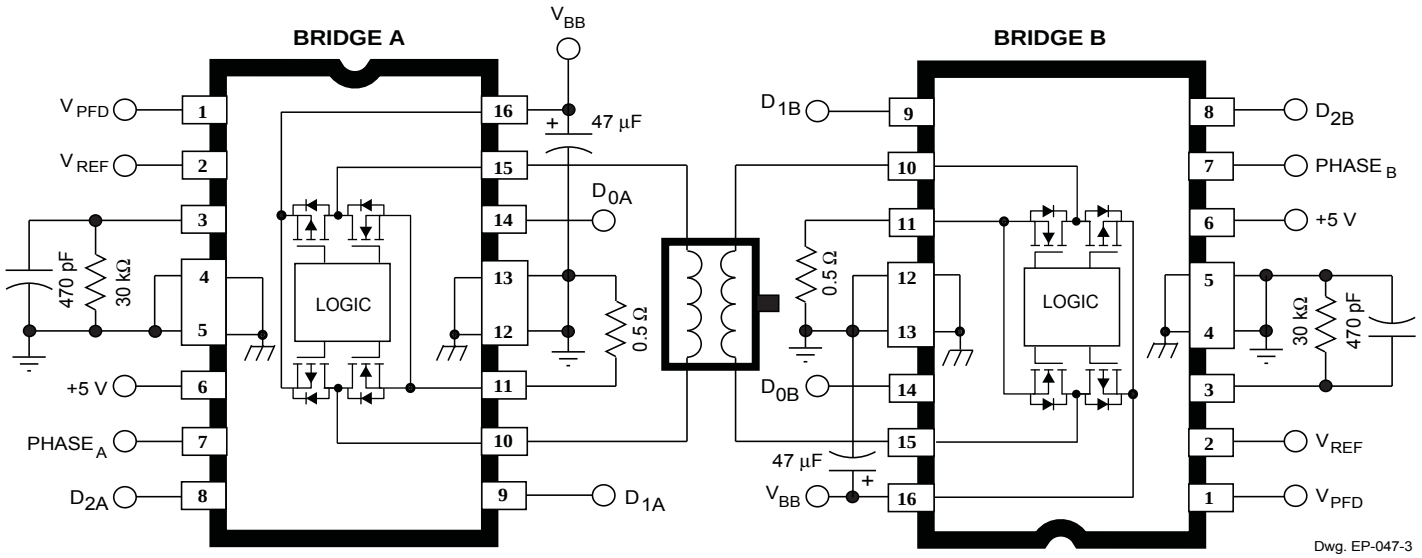


Figure 4 — Typical Application

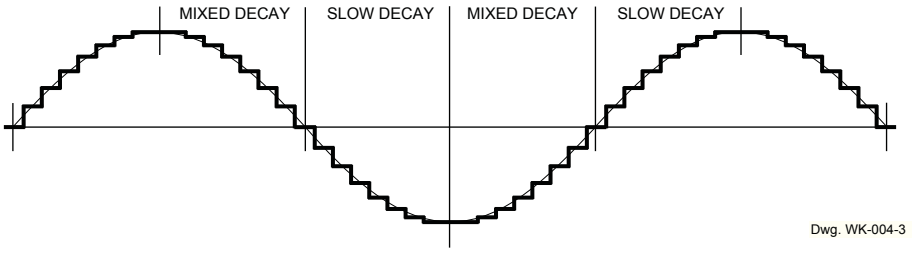


Figure 5 — Microstepping/Sinusoidal Drive Current

Table 4 — Step Sequencing

Full Step	Half Step	Quarter Step	Eighth Step	Bridge A					Bridge B				
				$PHASE_A$	D_{2A}	D_{1A}	D_{0A}	I_{LOADA}	$PHASE_B$	D_{2B}	D_{1B}	D_{0B}	I_{LOADB}
1	1	1	1	**H**	**H**	**L**	**L**	**70.7%**	**H**	**H**	**L**	**L**	**70.7%**
			2	**H**	**L**	**H**	**H**	**55.5%**	**H**	**H**	**L**	**H**	**83.1%**
		2	3	**H**	**L**	**H**	**L**	**38.2%**	**H**	**H**	**H**	**L**	**92.4%**
			4	**H**	**L**	**L**	**H**	**19.5%**	**H**	**H**	**H**	**H**	**100%**
	2	3	5	X	L	L	L	0%	**H**	**H**	**H**	**H**	**100%**
			6	L	L	L	H	-19.5%	**H**	**H**	**H**	**H**	**100%**
		4	7	L	L	H	L	-38.2%	**H**	**H**	**H**	**L**	**92.4%**
			8	L	L	H	H	-55.5%	**H**	**H**	**L**	**H**	**83.1%**
2	3	5	9	L	H	L	L	-70.7%	**H**	**H**	**L**	**L**	**70.7%**
			10	L	H	L	H	-83.1%	**H**	**L**	**H**	**H**	**55.5%**
		6	11	L	H	H	L	-92.4%	**H**	**L**	**H**	**L**	**38.2%**
			12	L	H	H	H	-100%	**H**	**L**	**L**	**H**	**19.5%**
	4	7	13	L	H	H	H	-100%	X	L	L	L	0%
			14	L	H	H	H	-100%	L	L	L	H	-19.5%
		8	15	L	H	H	L	-92.4%	L	L	H	L	-38.2%
			16	L	H	L	H	-83.1%	L	L	H	H	-55.5%
3	5	9	17	L	H	L	L	-70.7%	L	H	L	L	-70.7%
			18	L	L	H	H	-55.5%	L	H	L	H	-83.1%
		10	19	L	L	H	L	-38.2%	L	H	H	L	-92.4%
			20	L	L	L	H	-19.5%	L	H	H	H	-100%
	6	11	21	X	L	L	L	0%	L	H	H	H	-100%
			22	**H**	**L**	**L**	**H**	**19.5%**	L	H	H	H	-100%
		12	23	**H**	**L**	**H**	**L**	**38.2%**	L	H	H	L	-92.4%
			24	**H**	**L**	**H**	**H**	**55.5%**	L	H	L	H	-83.1%
4	7	13	25	**H**	**H**	**L**	**L**	**70.7%**	L	H	L	L	-70.7%
			26	**H**	**H**	**L**	**H**	**83.1%**	L	L	H	H	-55.5%
		14	27	**H**	**H**	**H**	**L**	**92.4%**	L	L	H	L	-38.2%
			28	**H**	**H**	**H**	**H**	**100%**	L	L	L	H	-19.5%
	8	15	29	**H**	**H**	**H**	**H**	**100%**	X	L	L	L	0%
			30	**H**	**H**	**H**	**H**	**100%**	**H**	**L**	**L**	**H**	**19.5%**
		16	31	**H**	**H**	**H**	**L**	**92.4%**	**H**	**L**	**H**	**L**	**38.2%**
			32	**H**	**H**	**L**	**H**	**83.1%**	**H**	**L**	**H**	**H**	**55.5%**

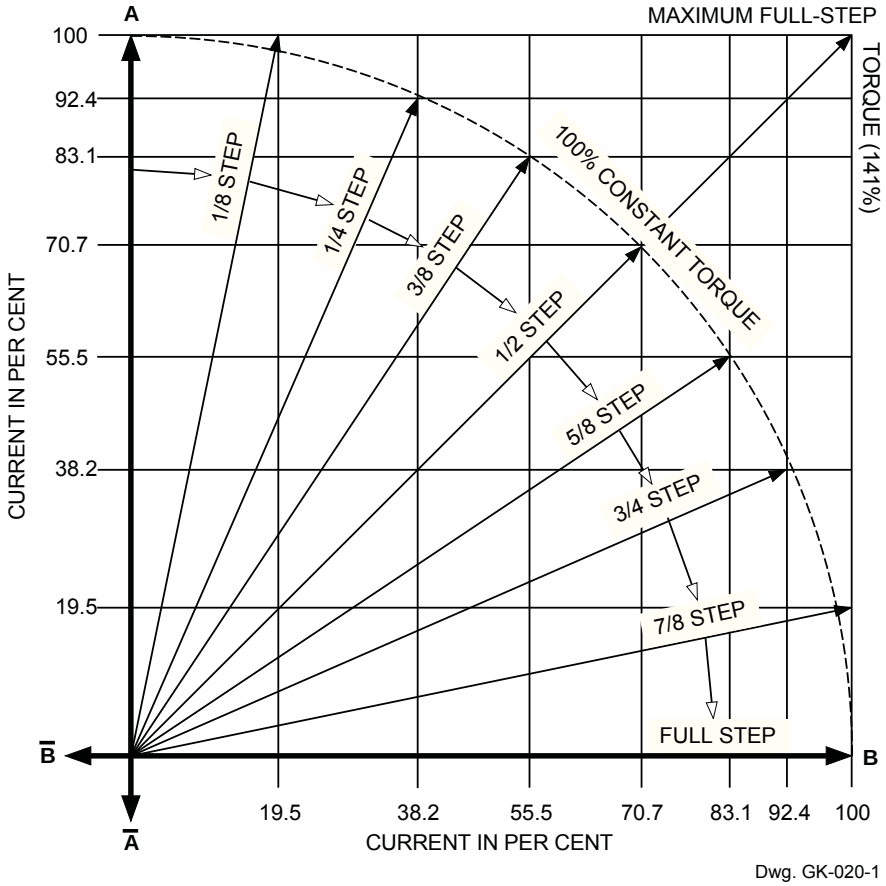
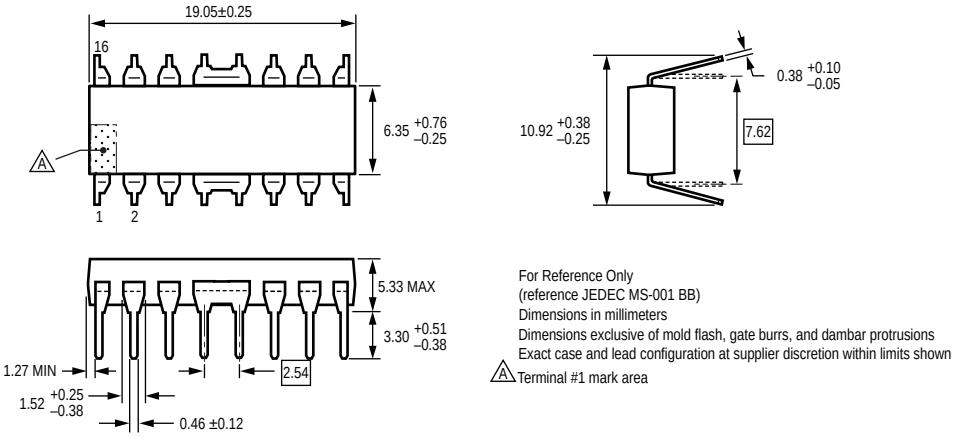


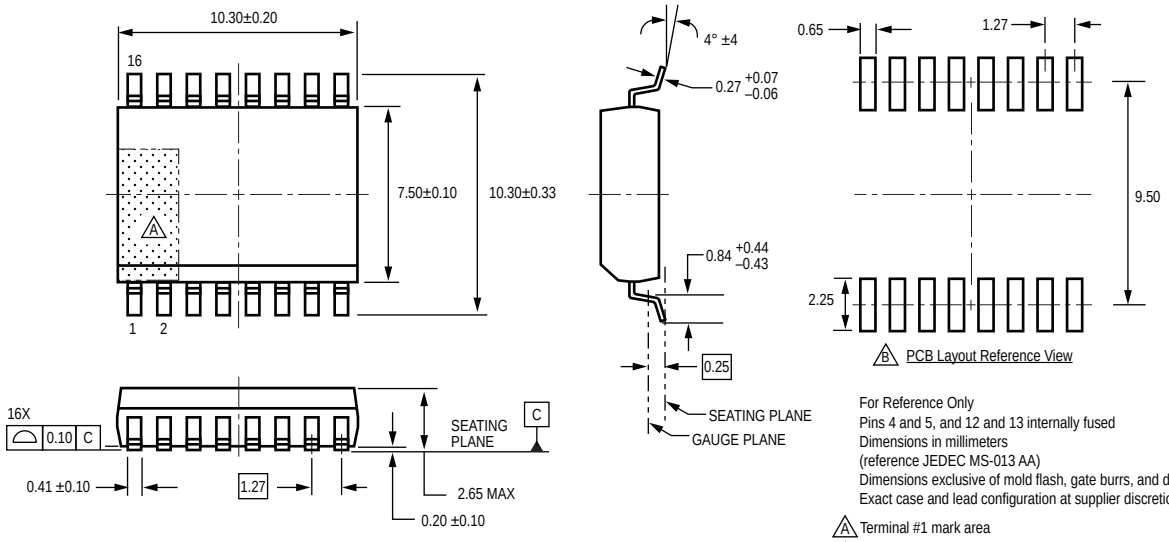
Figure 5 —
Current and Displacement Vectors

B package 16-pin DIP



For Reference Only
(reference JEDEC MS-001 BB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LB package 16-pin SOICW



For Reference Only
Pins 4 and 5, and 12 and 13 internally fused
Dimensions in millimeters
(reference JEDEC MS-013 AA)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-16M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Revision History

Revision	Revision Date	Description of Revision
Final	December 19, 2011	Update production availability

For the latest version of this document, visit our website:
www.allegromicro.com