◇Structure Silicon Monolithic integrated circuit
◇Product name Audio interface + Video driver LSI
◇Type BU7636MWV
◇Applications DVC, DSC, etc.
◇Functions ＜Audio part＞

- ・Stereo 16 bit ΔΣCODEC
- ・3-input stereo selector
- ・Stereo microphone amplifier with ALC function
- ・Stereo line amplifier
- ・BTL output speaker amplifier （300mW@8Ω）
- ・64-step electronic volume with ALC function
- ・Master clock：256fs/384fs/512fs/1024fs
- ・Sampling rate：8kHz～48kHz
- ・Three-line serial interface （power on reset function）
- ・Audio IF format MSB First, 2's compliment
  ＜ADC＞ 16bit word lengths Left justified, I^2S
  ＜DAC＞ 16bit word lengths Left, Right justified, I^2S

＜Video part＞

- ・Sync-tip-clamp, 6th LPF, Y/C/V output video driver
- ・Output coupling condenser unnecessary
- ・Aspect ratio identification signal output

◇Absolute maximum ratings （Ta=25℃）

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	LVDD1	−0.3～4.5	V	AVDD、DVDD、SPVDD、VVDD
	LVDD2	−0.3～4.5	V	CPVDD
	HVDD	−0.3～6.0	V	VVDD_SDC
Input voltage	VIN	−0.3 ～ supply voltage + 0.3	V	keep each limits upon
Storage temperature range	TSTG	−50～125	℃	
Operating temperature range	TOPE	−20～85	℃	
Power dissipation ＊1	PD	800	mW	

＊1：In the case of use at Ta=25℃ or more, 8.0mW should be reduced per 1℃.
(t=1.6mm, 74.2mm x 74.2mm, 1-layer board, Cu surface radiate foil 0mm^2)
Radiation resistance design is not arranged.

◇Operating conditions （Ta=25℃）

Parameter	Symbol	Limits	Unit	Comment
Supply voltage	LVDD1	2.7～3.6	V	AVDD、DVDD、SPVDD、VVDD
	LVDD2	2.7～3.4	V	CPVDD
	HVDD	4.5～5.5	V	VVDD_SDC

(note) AVDD、DVDD、SPVDD、VVDD are not needed to be same voltage.
(note) Please do not set SPVDD lower than AVDD-0.3V.

◇Electrical characteristics

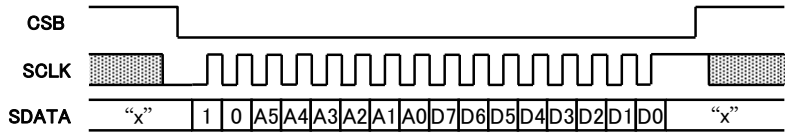
(Unless specified, Ta=25℃、AVDD=SPVDD=DVDD=VVDD=CPVDD= 3.3V、VVDD_SDC=5.0V、AVSS=SPVSS=DVSS=VVSS= 0V、B.W.=22Hz～22kHz、fs=48kHz、fin=1kHz)

Parameter		Symbol	Limits			Unit	Condition
			MIN.	TYP.	MAX.		
< Current consumption > #MCLK=24MHz							
Power-down mode		IDDS	−	0.03	0.1	mA	#PWAP=0
Rec mode		IDDR	−	8.5	16	mA	#MDREC=1
Play mode		IDDP	−	7.5	16	mA	#MDPB=MDSP= 1
Video mode		IDDV	−	33	80	mA	#PWVD=PWCP=1
<MREG>							
output voltage		VOREG	0.75AVDD−0.2	0.75AVDD	0.75AVDD+0.2	V	2.2kΩ load
<Logic interface>							
L input voltage		VIL	DVSS	—	0.3DVDD	V	
H input voltage		VIH	0.7DVDD	—	DVDD	V	
Input current		IIL	−10	—	10	μA	
L output voltage		VOL	0	—	0.5	V	IOL=−1mA
H output voltage		VOH	DVDD−0.5	—	DVDD	V	IOL=1mA
<REC path (MICIN→ADOUT)> #ALC1=OFF, MIC GAIN 22dB (MGAIN=42dB, MLIM=−20dB)							
Input impedance		ZIN	70	100	130	kΩ	
Input level		VIN	−26	−24	−22	dBV	DOUT=0dBFS
L/R gain mismatch		△GV	−1.0	0	+1.0	dB	DOUT=0dBFS
Distortion		THD+N	62	70	−	dB	DOUT=−6dBFS@1kHz
SNR		SNR	79	84	−	dB	B.W.=JIS-A
L/R separation		SEPR	79	100	−	dB	DOUT=−6dBFS@1kHz
ALC1 output level		DOALC	−	−6	−	dBFS	ALC1=ON
<PB path1 (DAIN→LINEOUT)> #LGAIN=+5dB							
Output level		VO	−5.5	−4.0	−2.5	dBV	DIN=−6dBFS
L/R gain mismatch		△GV	−1.0	0	+1.0	dB	DIN=−6dBFS
Distortion		THD+N	70	80	−	dB	DIN=−6dBFS@1kHz
SNR		SNR	82	90	−	dB	B.W.=JIS-A
L/R separation		SEPR	80	100	−	dB	DIN=−6dBFS@1kHz
<PB path2 (DAIN→EVROUT→SPIN→SPOUT BTL 出力)> #ALC2=OFF, EVR=−6dB, RL=8Ω							
Output level		VO	1.0	3.0	5.0	dBV	DIN=0dBFS
Distortion		THD+N	50	60	−	dB	DIN=0dBFS@1kHz
SNR		SNR	76	83	−	dB	B.W.=JIS-A
ALC2 output level		VOALC	1.0	3.0	5.0	dBV	ALC2=ON, EVR=8dB
< Video path (YIN→YOUT, VOUT)(CIN→COUT, VOUT)>							
Voltage gain		GV	+5.5	+6.0	+6.5	dB	VIN=100KHz, 1.0Vpp
Maximum output level		VOM	2.2	2.6	−	Vpp	f=10KHz, THD=1%
Frequency characteristic 1		GF1	−3.0	0	−	dB	f=6MHz/100KHz
Frequency characteristic 1		GF2	−	−27	−18	dB	f=18MHz/100KHz
Differential gain		DG	−	1.0	3.0	%	VIN=1.0Vpp Standard stair step signal
Differential phase		DP	−	1.0	3.0	deg	VIN=1.0Vpp Standard stair step signal
Y signal output S/N		SNY	+50	+65	−	dB	Band 100k～6MHz Terminal impedance 150Ω 100% white video signal
S-DC output voltage	L	V_{SDCL}	−	0.1	0.5	V	RL=10kΩ+100kΩ
	M	V_{SDCM}	1.8	2.1	2.4	V	RL=10kΩ+100kΩ
	H	V_{SDCH}	4.0	4.6	−	V	RL=10kΩ+100kΩ

(note) Input level of REC and Output level of PB are relative to AVDD. (note) V_{SDCM}, V_{SDCH} is relative to VVDD_SDC.

◇Serial interface

Control commands are entered on the CSB, SCLK, and SDATA pins, using 3 line 16 bit serial input (MSB first).
The input cycle is started on the CSB falling edge, and each bit of data is read in on the SCLK rising edge.
The data is loaded to register on the CSB rising edge.



Register Address : A5 – A0
Control Data : D7 – D0

◇Register map

Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power control	0	PWSV	PWAP	PWMRG	PWVD	PWCP	0	PWDRG
01H	Power control	0	COMENB	0	0	MDSP	MDPB	MDREC	0
03H	Gain control	1	0	ADA	0	0	LGAIN	MGAIN1	MGAIN0
04H	Gain control	SLMIN1	SLMIN0	0	0	MUSP	MUBSP	MULO	MUDVL
05H	Clock control	FMCK1	FMCK0	0	1	0	DIF2	DIF1	DIF0
06H	Clock control	0	0	0	0	SFS1	SFS0	DIV1	DIV0
07H	Clock control	0	BFPD	0	DLEN	0	0	0	0
08H	ALC control	0	MDALC1	MDEVR1	MDEVR0	0	0	0	MDDVL
09H	ALC control	ATMC1	ATMC0	RCMC1	RCMC0	ATSP1	ATSP0	RCSP1	RCSP0
0AH	ALC control	RC2MC1	RC2MC0	0	0	RCLM	0	0	0
0BH	Time control	RINI2	RINI1	RINI0	PINI1	PINI0	0	0	EVRT
0CH	Volume control	0	MLIM6	MLIM5	MLIM4	MLIM3	MLIM2	MLIM1	MLIM0
0DH	Filter control	0	0	DEM1	DEM0	HPFR3	HPFR2	HPFR1	HPFR0
0EH	Volume control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
0FH	Volume control	0	0	EVR5	EVR4	EVR3	EVR2	EVR1	EVR0
10H	Volume control	0	0	SPVOL1	SPVOL0	0	BVOL2	BVOL1	BVOL0
12H	Fade control	0	0	0	0	DVLSK	DVLT2	DVLT1	DVLT0
13H	Video control	1	1	1	SDC1	SDC2	0	0	0

(note) Do not write to the address except for the above.

◇Pin Functional Descriptions

No	Pin name	Function
1	CPVDD	Charge pump power supply
2	C4	Flying condenser terminal 4
3	C3	Flying condenser terminal 3
4	C2	Flying condenser terminal 2
5	VVEE	Video negative power supply
6	CIN	Chroma signal input
7	VVSS	Video ground
8	YIN	Luminance signal input
9	VVDD	Video power supply
10	YOUT	Luminance signal output
11	VOUT	Composite signal outut
12	COUT	Chroma signal output
13	SDCOUT	SDC signal output
14	VVDD_SDC	SDC power supply
15	DVDD	Digital power supply
16	DAIN	CODEC DA serial data input
17	ADOUT	CODEC AD serial data output
18	BCLK	CODEC bit clock in/output
19	LRCLK	CODEC LR clock in/output
20	MCLK	CODEC master clock input
21	DVSS	Digital ground
22	SDATA	3-wire serial data input

No	Pin name	Function
23	SCLK	3-wire serial clock input
24	CSB	3-wire chip select input
25	MICINR3	MICRch input 3
26	MICINR2	MICRch input 2
27	MICINR1	MICRch input 1
28	MREG	MIC power supply
29	MICINL1	MICLch input 1
30	MICINL2	MICLch input 2
31	MICINL3	MICLch input 3
32	BIAS	Bias (1/2AVDD)
33	AVSS	Analog ground
34	AVDD	Analog power supply
35	LINEOUTR	LINE output
36	LINEOUTL	LINE output
37	EVROUT	EVR output
38	SPIN	SP input
39	SPNEG	SP negative output
40	SPVSS	SP ground
41	SPVDD	SP power supply
42	SPPOS	SP positive output
43	BEEPIN	BEEP input
44	C1	Flying condenser terminal 1

◇Block diagram・External dimensions

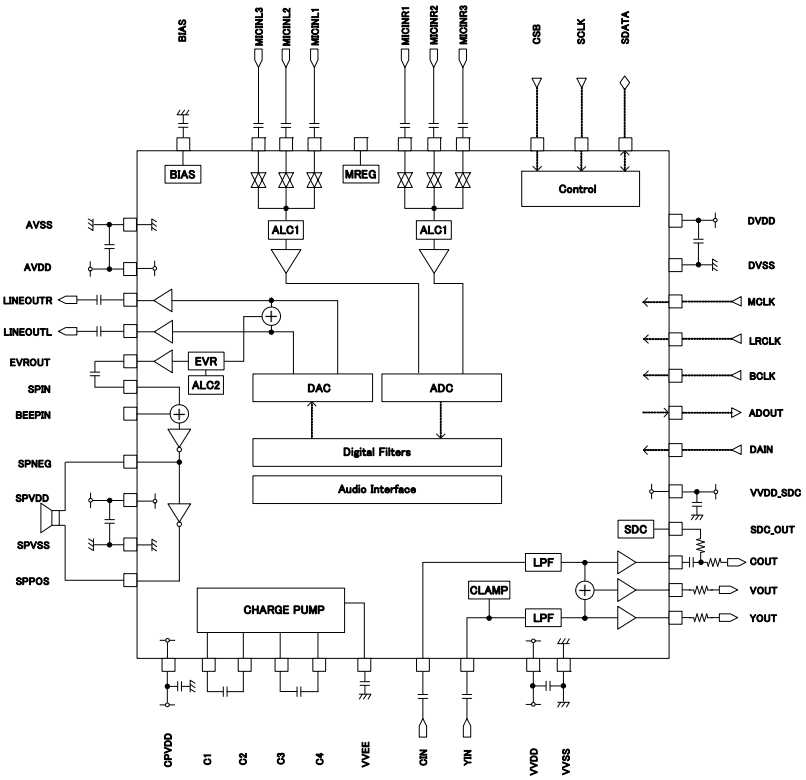


Figure 1　Block diagram

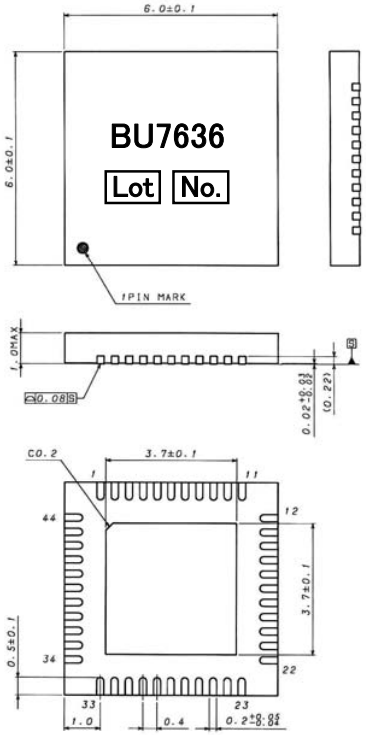


Figure 2　External dimension (Unit : mm)

PKG : UQFN044V6060
Drawing No. : EX475-6002

◇Caution

（1） About absolute maximum rating
When the absolute maximum rating such as the applied voltage and the ranges of the operating temperature is exceeded, LSI might be destroyed. Please apply neither voltage nor the temperature that exceeds the absolute maximum rating. Please execute physical measures for safety such as fuse when it is thought to exceed the absolute maximum rating, and examine it so that the condition to exceed the absolute maximum rating is not applied to LSI.

（2） About GND Voltage
In any state of operation must be the lowest voltage about the voltage of the terminal GND. Please actually confirm the voltage of each terminal is not a voltage that is lower than the terminal GND including excessive phenomenon.

（3） About design of overheating malfunction preventive circuit
Please design overheating malfunction preventive circuit with an enough margin in consideration of a permissible loss in the state of using actually.

（4） About the short between terminals and the mounting by mistake
Please note the direction and the gap of position of LSI enough about LSI when you mount on the substrate. LSI might be destroyed when mounting by mistake and energizing. Moreover, LSI might be destroyed when short-circuited by entering of the foreign substances between the terminal and GND, between terminals, between the terminal and the power supply of LSI.

（5） About operation in strong electromagnetic field
Use in strong electromagnetic field has the possibility of malfunctioning and evaluate it enough, please.

（6） Please note not to be beyond the package permissible range, When SPVDD is set.

（7） About charge pump
For prevent the undetermined state of charge pump, recommend to put together CPVDD and DVDD pins.
And to avoid the IC's broken or smoke, you must not supply the external voltage or current to C1, C2, C3, C4, and VEE pins.

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