HMC552LP4 / 552LP4E

v00.0306

GaAs MMIC MIXER w/ INTEGRATED LO AMPLIFIER, 1.6 - 3.0 GHz

Typical Applications

The HMC552LP4 / HMC552LP4E is ideal for Wireless Infrastructure Applications:

- PCS / 3G Infrastructure
- Base Stations & Repeaters
- WiMAX & WiBro
- ISM & Fixed Wireless

Features

Input IP3: +25 dBm

Low Input LO Drive: -4 to +4 dBm

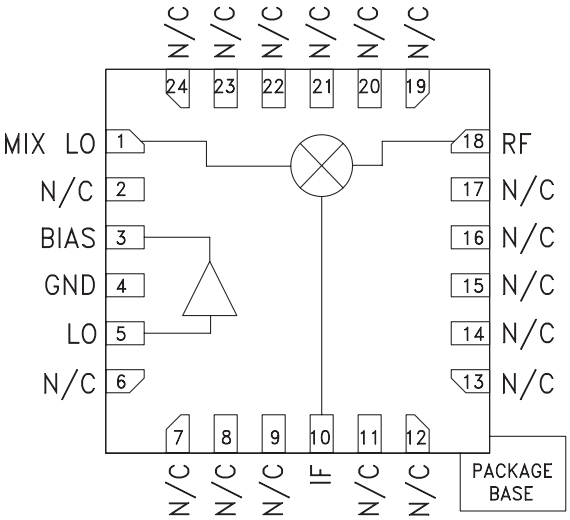
LO to RF Isolation: 30 dB

Low Conversion Loss: 8 dB

Single Positive Supply: +5V @ 62 mA

RoHS Compliant 4x4 mm QFN Package

Functional Diagram



General Description

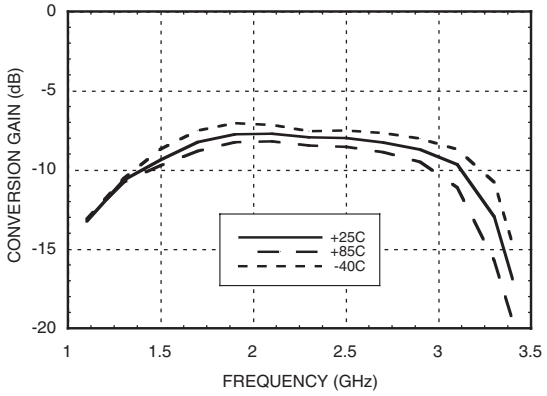
The HMC552LP4 & HMC552LP4E are high linearity, double-balanced converter ICs that operate from 1.6 to 3.0 GHz and deliver a +25 dBm input third order intercept point. The LO amplifier output and high dynamic range mixer input are positioned so that an external LO filter can be placed in series between them. The converter provides 30 dB of LO to RF isolation and is ideal for upconverter and downconverter applications. The IC operates from a single +5V supply consuming 62 mA of current and accepts a LO drive level of -4 to +4 dBm. The design requires no external baluns and supports IF frequencies between DC and 1 GHz. The HMC552LP4 & HMC552LP4E are pin for pin compatible with the HMC551LP4 & HMC551LP4E, which operate from 0.8 to 1.2 GHz.

Electrical Specifications, T_A = +25° C, LO = 0 dBm, Vcc = +5V, IF = 100 MHz*

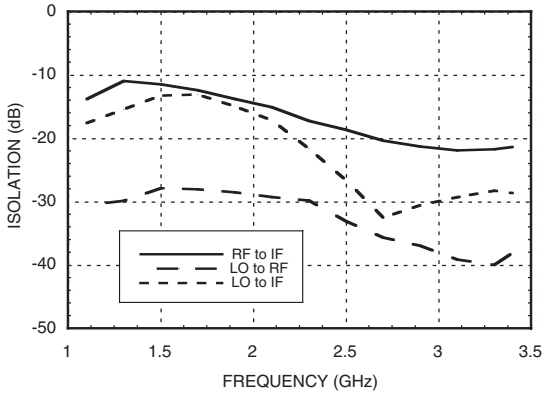
Parameter	Min.	Typ.	Max.	Units
Frequency Range, RF, LO		1.6 - 3.0		GHz
Frequency Range, IF		DC - 1.0		GHz
Conversion Loss		8	10	dB
Noise Figure (SSB)		8		dB
LO to RF Isolation	25	30		dB
LO to IF Isolation	10	20		dB
IP3 (Input)		25		dBm
1 dB Compression (Input)		16		dBm
LO Drive Input Level (Typical)		-4 to +4		dBm
Supply Current (Icc)		62		mA

Unless otherwise noted, all measurements performed as a downconverter configured as shown in application circuit.

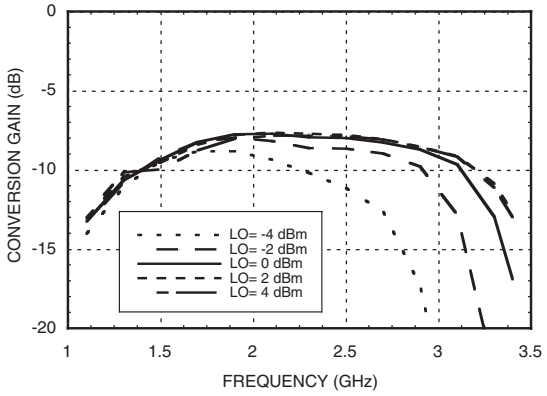
Conversion Gain vs. Temperature @ LO = 0 dBm



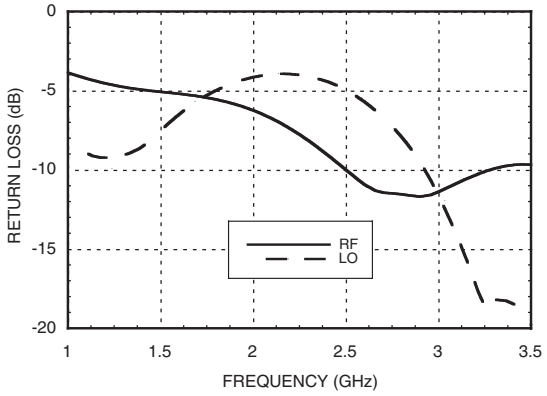
Isolation @ LO = 0 dBm



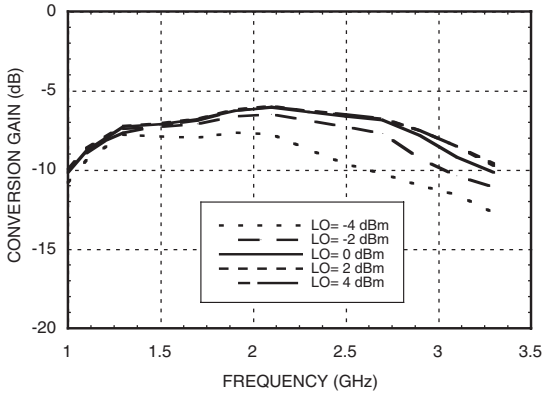
Conversion Gain vs. LO Drive



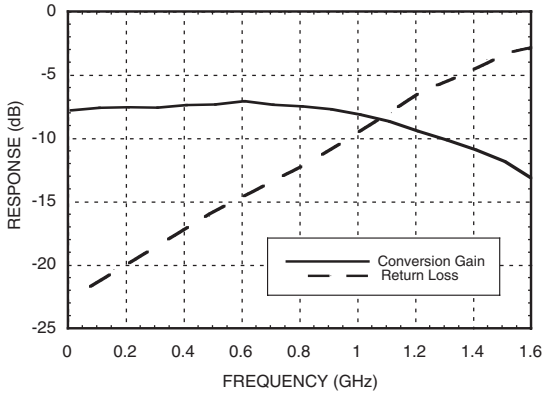
Return Loss @ LO = 0 dBm



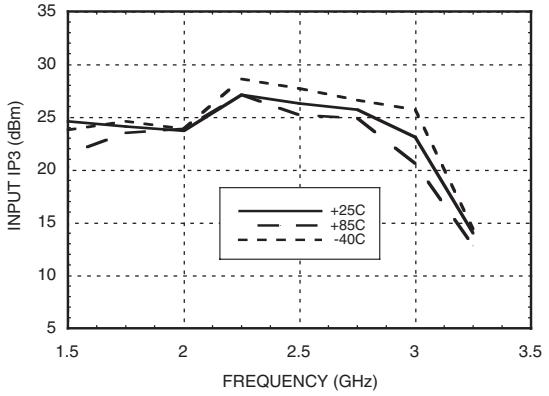
Upconverter Performance Conversion Gain vs. LO Drive



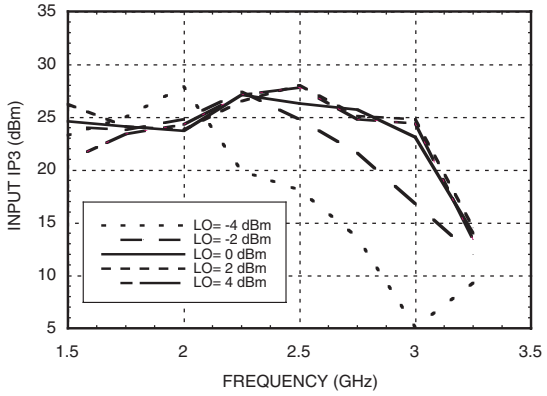
IF Bandwidth @ LO = 0 dBm



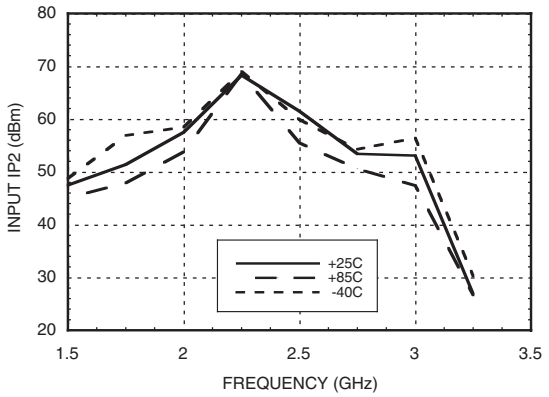
Input IP3 vs. Temperature @ LO = 0 dBm



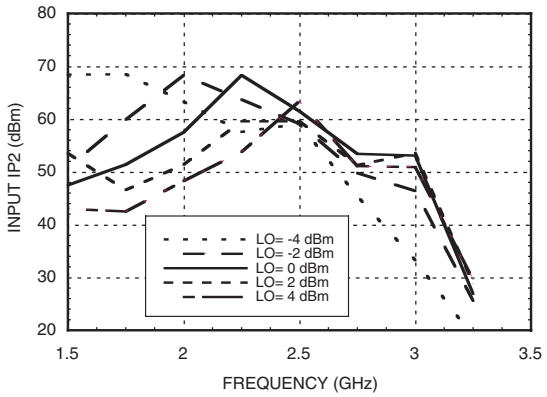
Input IP3 vs. LO Drive



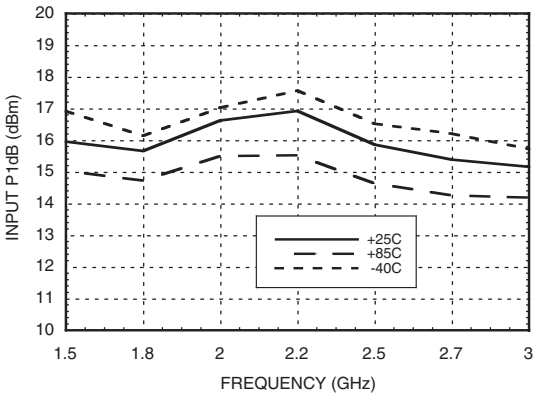
Input IP2 vs. Temperature @ LO = 0 dBm



Input IP2 vs. LO Drive



Input P1dB vs. Temperature @ LO = 0 dBm



MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	-3	16	16	25
1	7	0	23	44	53
2	79	66	61	61	98
3	102	105	93	94	84
4	103	107	107	102	103

RF Freq. = 1.9 GHz @ -10 dBm
LO Freq. = 1.8 GHz @ 0 dBm
All values in dBc relative to the IF power level.

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
1.5	27	17	31	32
1.8	28	16	40	44
2.1	28	18	31	47
2.4	34	21	33	41
2.7	36	28	42	46
3.0	41	27	48	54

LO = 0 dBm
All values in dBc below input LO level measured at RF port.

Typical Supply Current

Vcc	Icc (mA)
+5.0	62 mA

HMC552LP4 / 552LP4E

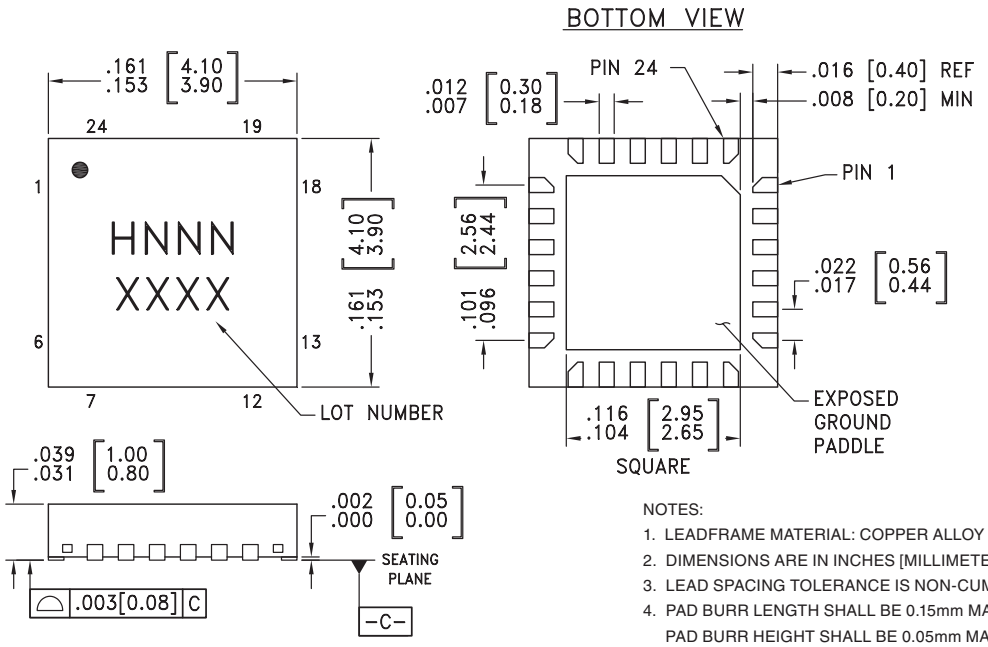
GaAs MMIC MIXER w/ INTEGRATED LO AMPLIFIER, 1.6 - 3.0 GHz

Absolute Maximum Ratings

RF / IF Input (Vcc= +5V)	+31 dBm
LO Drive (Vcc= +5V)	+10 dBm
BIAS	+7 Vdc
Junction Temperature	150°C
Continuous Pdiss (T = 85°C) (derate 9.5 mW/°C above 85°C)	0.6 W
Thermal Resistance (junction to ground paddle)	105.6 °C/W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

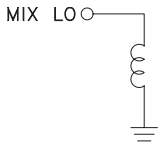
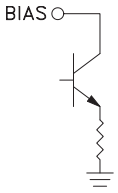
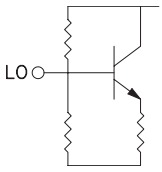
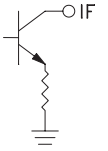
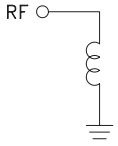
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

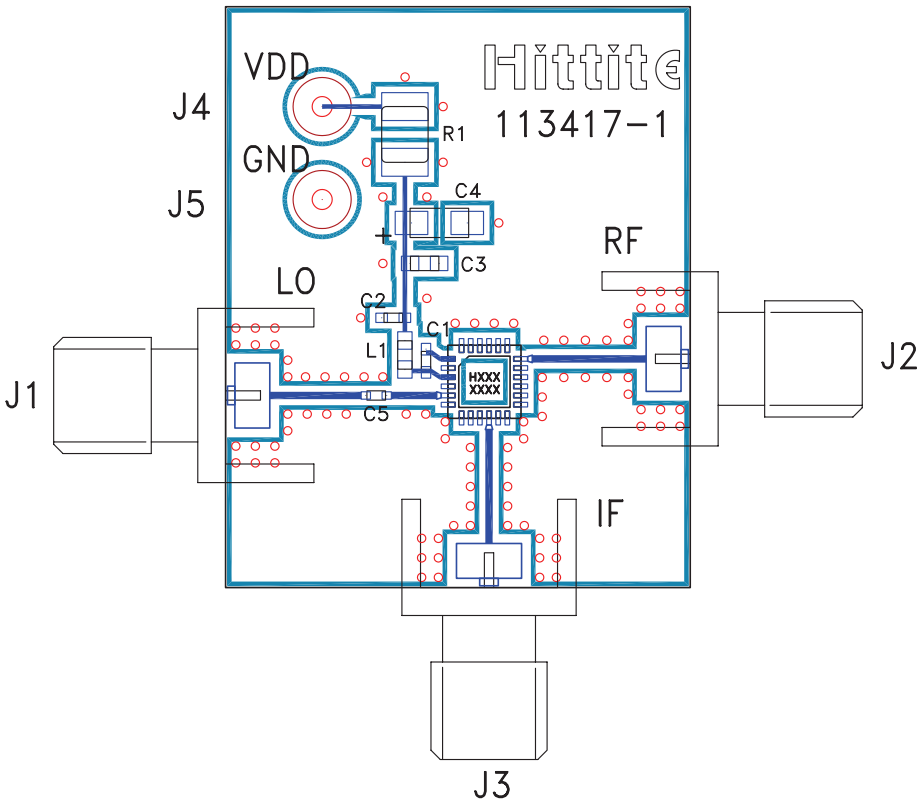
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC552LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H552 XXXX
HMC552LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H552 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	MIX LO	This pin is DC coupled and matched to 50 Ohms from 1.6 to 3.0 GHz. An off chip DC blocking capacitor is required.	
2, 6 - 9, 11 - 17, 19 - 24	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
3	BIAS	Power supply for the second stage LO amplifier. Three external bypass capacitors are recommended for optimum performance, as illustrated in the application circuit.	
4	GND	Backside of package has exposed metal ground paddle that must also be connected to ground.	
5	LO	This pin is DC coupled and matched to 50 Ohms from 1.6 to 3.0 GHz. An off chip DC blocking capacitor is required.	
10	IF	This pin is DC coupled. For applications not requiring operation to DC, this port should be DC blocked externally using a series capacitor whose value has been chosen to pass the necessary IF frequency range. For operation to DC, this pin must not source/sink more than 18 mA of current or die non-function and possible die failure will result.	
18	RF	This pin is DC coupled and matched to 50 Ohms from 1.6 to 3.0 GHz.	

Evaluation PCB



List of Materials for Evaluation PCB 113722 [1]

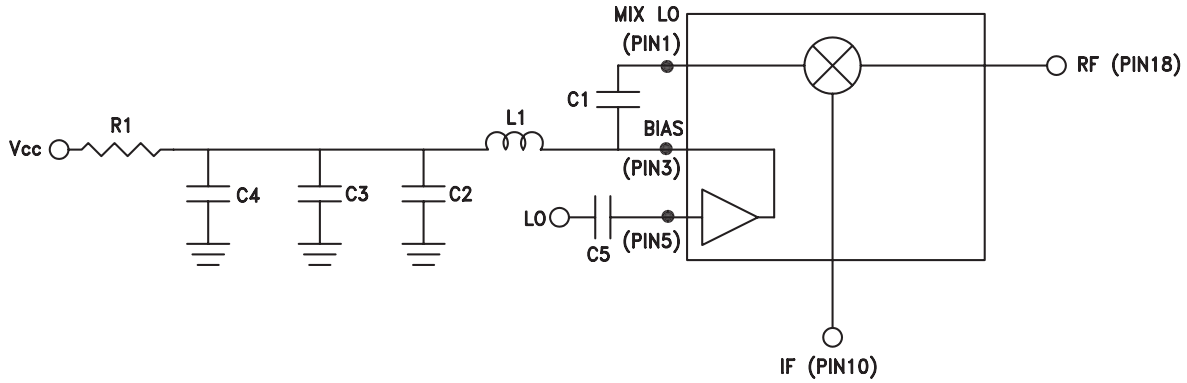
Item	Description
J1 - J3	PCB Mount SMA RF Connector
J4, J5	DC Pin
C1, C2, C5	100 pF Chip Capacitor, 0402 Pkg.
C3	1000 pF Chip Capacitor, 0603 Pkg.
C4	2.2 µF Capacitor, Tantalum
L1	18 nH Chip Inductor, 0603 Pkg.
R1	18 Ohm Resistor, 1210 1/8 watt Pkg.
U1	HMC552LP4 / HMC552LP4E
PCB [2]	113417 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Recommended Components Values (IF = DC - 300 MHz)	
C3	1000 pF
C4	2.2 µF
C1, C2, C5	100 pF
L1	18 nH
R1	18 Ohm