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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR $\mu$ PA2743T1A

# SWITCHING N-CHANNEL POWER MOSFET

#### **DESCRIPTION**

The  $\mu$ PA2743T1A is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

#### **FEATURES**

• Low on-state resistance

 $R_{DS(on)1}$  = 3.3 m $\Omega$  MAX. (VGS = 10 V, ID = 15 A)

 $R_{DS(on)2} = 4.6 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 4.5 \text{ V}, I_{D} = 15 \text{ A)}$ 

- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON (6051))
- RoHS Compliant

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±29	Α
Drain Current (pulse) Note1	I <sub>D(pulse)</sub>	±170	Α
Total Power Dissipation Note2	P <sub>T1</sub>	1.5	W
Total Power Dissipation (PW = 10 sec) Note2	P <sub>T2</sub>	4.6	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	29	Α
Single Avalanche Energy Note3	Eas	84.1	mJ

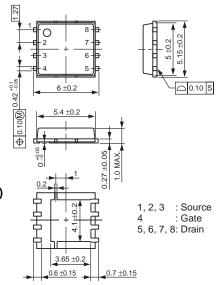
#### THERMAL RESISTANCE

Channel to Ambient Thermal Resistance Note2	Rth(ch-A)	83.3	°C/W
Channel to Case (Drain) Thermal Resistance	Rth(ch-C)	1.5	°C/W

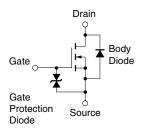
**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- 2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt
- 3. Starting Tch = 25°C, VdD = 15 V, Rg = 25  $\Omega$ , Vgs = 20  $\rightarrow$  0 V, L = 100  $\mu$ H

#### PACKAGE DRAWING (Unit: mm)



#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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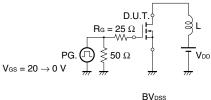


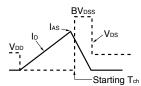
#### ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	Igss	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μΑ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	13			S
Drain to Source On-state Resistance Note	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		2.1	3.3	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		3.7	4.6	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 15 V,		5080		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		650		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		380		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 15 A,		28		ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		29		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		109		ns
Fall Time	tf			32		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 15 V,		39		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 5 V,		16		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 29 A		17		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	I <sub>F</sub> = 29 A, V <sub>GS</sub> = 0 V		0.79	1.2	V
Reverse Recovery Time	trr	I <sub>F</sub> = 29 A, V <sub>GS</sub> = 0 V,		38		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		39		nC

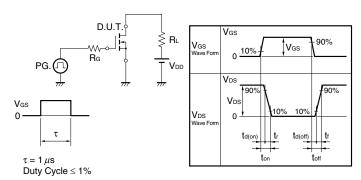
Note Pulsed

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**





#### **TEST CIRCUIT 2 SWITCHING TIME**



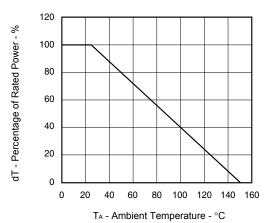
#### **TEST CIRCUIT 3 GATE CHARGE**

$$\begin{array}{c|c} D.U.T. \\ \hline la = 2 \text{ mA} \\ \hline \hline W. \\ \hline \end{array}$$

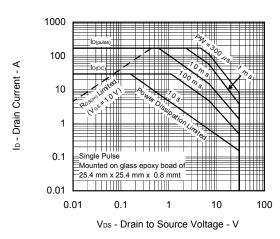
$$\begin{array}{c|c} PG. \\ \hline \end{array} \begin{array}{c} 50 \Omega \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array}$$

#### TYPICAL CHARACTERISTICS (TA = 25°C)

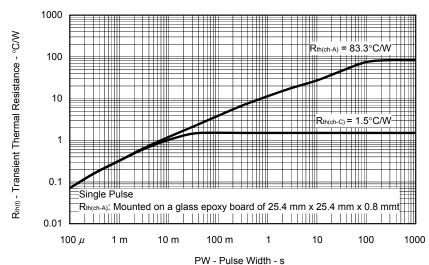
### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



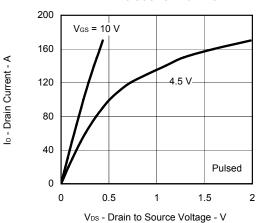
#### FORWARD BIAS SAFE OPERATING AREA



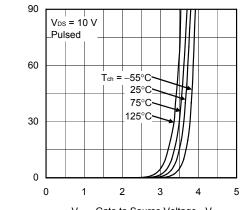
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

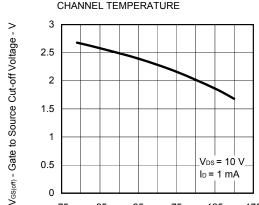


#### FORWARD TRANSFER CHARACTERISTICS



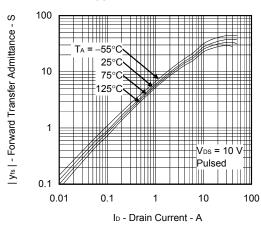
V<sub>GS</sub> - Gate to Source Voltage - V

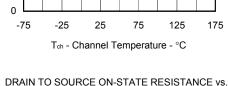
Ib - Drain Current - A



GATE TO SOURCE CUT-OFF VOLTAGE vs.

## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





DRAIN CURRENT

V<sub>GS</sub> = 4.5 V

10 V

10

8

6

4

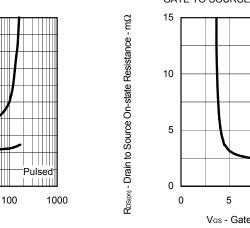
2

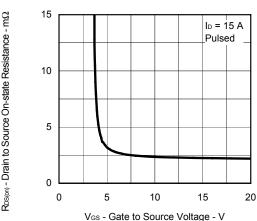
0

0.1

 $\mathsf{Ros}_{(\mathsf{on})}$  - Drain to Source On-state Resistance -  $m\Omega$ 

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

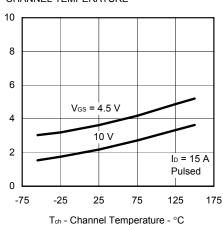




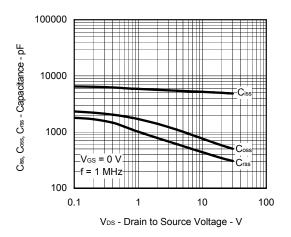
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

10

ID - Drain Current - A

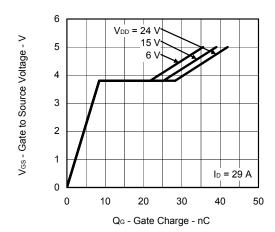


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

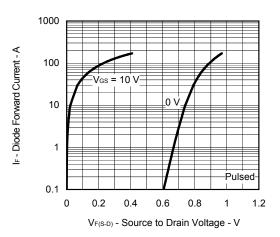


R<sub>DS(m)</sub> - Drain to Source On-state Resistance - mΩ

#### DYNAMIC INPUT CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE



#### **ORDERING INFORMATION**

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μPA2743T1A-E1-AY Note	Dura Ca	Tana 2000 n/mal	8-pin HVSON (6051)
μPA2743T1A-E2-AY Note	Pure Sn	Tape 3000 p/reel	0.10 g TYP.

Note Pb-free (This product does not contain Pb in the external electrode.)

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