

# MOS FIELD EFFECT TRANSISTOR $\mu PA2707GR$

# SWITCHING N-CHANNEL POWER MOS FET

# DESCRIPTION

The  $\mu$  PA2707GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

# FEATURES

- Low on-state resistance
- $\begin{aligned} R_{DS(on)1} &= 4.3 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 9.0 \text{ A}) \\ R_{DS(on)2} &= 5.6 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 9.0 \text{ A}) \end{aligned}$
- Low Ciss: Ciss = 6600 pF TYP. (VDS = 10 V, VGS = 0 V)
- Small and surface mount package (Power SOP8)

# ORDERING INFORMATION

PART NUMBER	PACKAGE		
μ PA2707GR-E1	Power SOP8		
μ PA2707GR-E1-A <sup>Note</sup>	Power SOP8		
μ PA2707GR-E2	Power SOP8		
μ PA2707GR-E2-A Note	Power SOP8		

**Note** Pb-free (This product does not contain Pb in external electrode and other parts.)

# ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (VGs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	D(DC)	±19	А
Drain Current (pulse) Note1	D(pulse)	±76	А
Total Power Dissipation Note2	P <sub>T1</sub>	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	P <sub>T2</sub>	2.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	–55 to +150	°C
Single Avalanche Current Note3	las	19	А
Single Avalanche Energy Note3	Eas	36	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

- 2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm
- 3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 15 V, R<sub>G</sub> = 25  $\Omega$ , L = 100  $\mu$ H, V<sub>GS</sub> = 20  $\rightarrow$  0 V

# THERMAL RESISTANCE

Channel to Ambient Note	Rth(ch-A)	114	°C/W
Channel to Drain Lead <sup>Note</sup>	Rth(ch-L)	22	°C/W

Note Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

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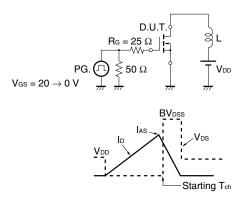
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V			±100	nA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.0		2.5	V
Forward Transfer Admittance Note	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	12			S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		3.3	4.3	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		4.1	5.6	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		6600		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		970		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		530		pF
Turn-on Delay Time	td(on)	Vdd = 15 V, Id = 10 A		24		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		29		ns
Turn-off Delay Time	td(off)	Rg = 10 Ω		130		ns
Fall Time	tr			39		ns
Total Gate Charge	QG	V <sub>DD</sub> = 15 V		52		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 5 V		16		nC
Gate to Drain Charge	Qgd	I <sub>D</sub> = 19 A		18		nC
Body Diode Forward Voltage Note	VF(S-D)	IF = 19 A, VGS = 0 V		0.8		V
Reverse Recovery Time	trr	IF = 19 A, VGS = 0 V		42		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ <i>µ</i> s		41		nC
Gate Resistance	Rg	f = 1 MHz		1.2		Ω

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)

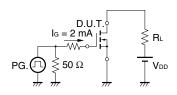
Note Pulsed

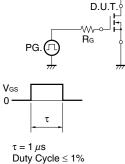
### TEST CIRCUIT 1 AVALANCHE CAPABILITY

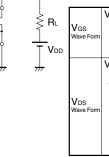
### **TEST CIRCUIT 2 SWITCHING TIME**



# **TEST CIRCUIT 3 GATE CHARGE**

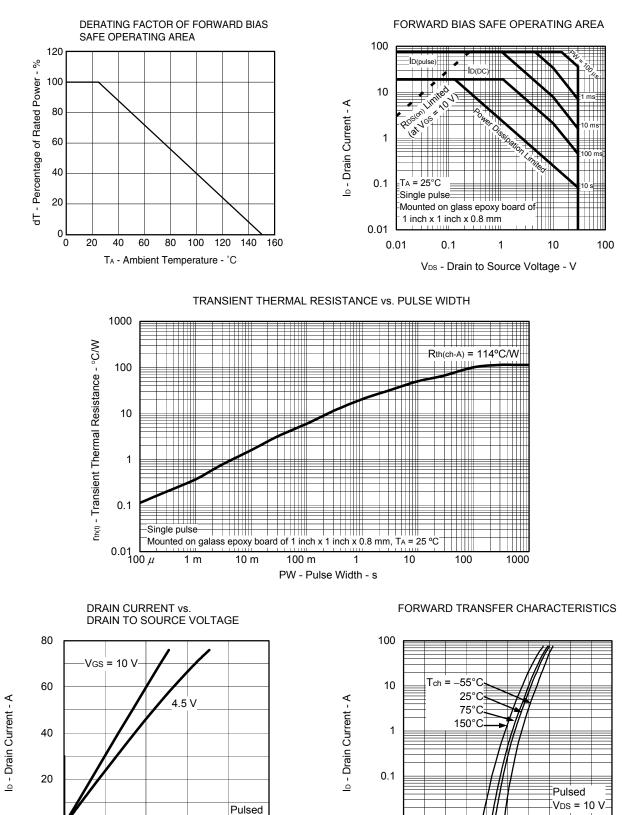






VGS Wave Form	Vgs 0 <u>10%</u> 7	VGS	90%
VDS Wave Form	VDS VDS 0 td(on)	tr td(off)	tr torf

# **TYPICAL CHARACTERISTICS (TA = 25^{\circ}C)**



0

0

0.1

0.2

VDS - Drain to Source Voltage - V

0.3

0.4

0.5

0.01

0

1

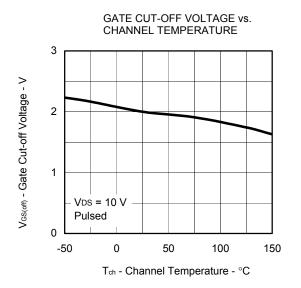
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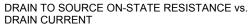
VGS - Gate to Source Voltage - V

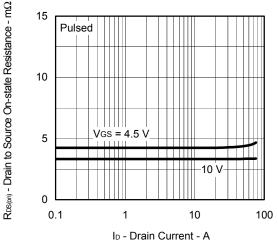
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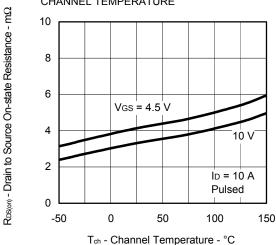
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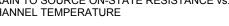
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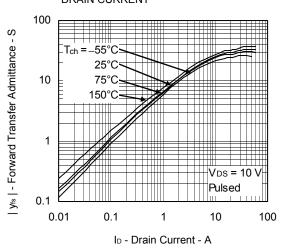




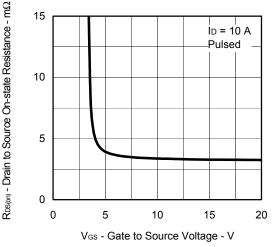




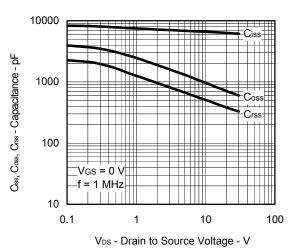
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

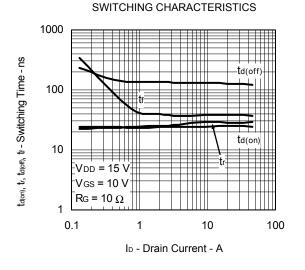


### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

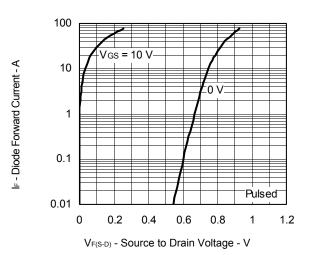


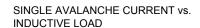
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

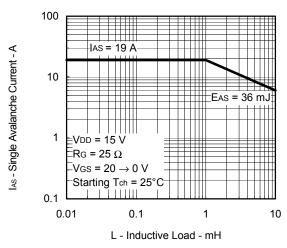




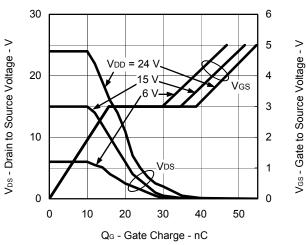
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



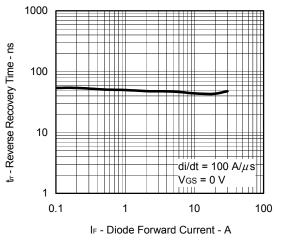


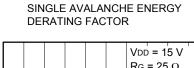


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

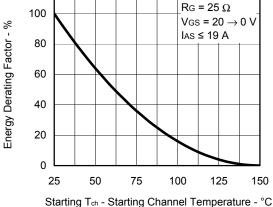








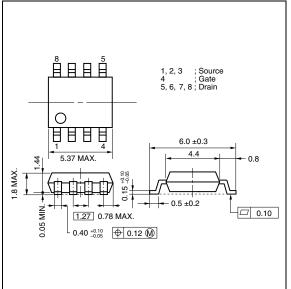
120



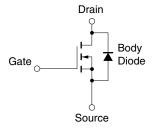
Data Sheet G17032EJ1V0DS

# PACKAGE DRAWING (Unit: mm)

### Power SOP8



# EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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