



**AO4447**

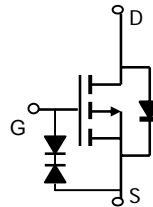
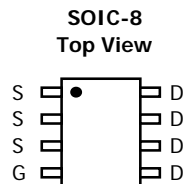
**P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

The AO4447 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , and ultra-low low gate charge. This device is suitable for use as a load switch. The device is ESD protected. *Standard Product AO4447 is Pb-free (meets ROHS & Sony 259 specifications). AO4447L is a Green Product ordering option. AO4447 and AO4447L are electrically identical.*

**Features**

- $V_{DS}$  (V) = -30V
- $I_D$  = -15 A ( $V_{GS}$  = -10V)
- Max  $R_{DS(ON)}$  < 7.5m $\Omega$  ( $V_{GS}$  = -10V)
- Max  $R_{DS(ON)}$  < 12m $\Omega$  ( $V_{GS}$  = -4V)
- ESD Rating: 4KV HBM



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>A</sup>	$T_A=25^\circ\text{C}$ $T_A=70^\circ\text{C}$	$I_D$	-15
			-13.6
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	-60	A
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$ $T_A=70^\circ\text{C}$	$P_D$	3.1
			2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	26	40	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	50	75	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	14	24	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>D</sub> DSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -10	μA
I <sub>G</sub> SS	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.3	-1.6	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-60			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-15A T <sub>J</sub> =125°C		6.7 9.4	8 12	mΩ
		V <sub>GS</sub> =-4V, I <sub>D</sub> =-13A		9.2	12	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-15A		60		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.69	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				5.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		5500	6600	pF
C <sub>OSS</sub>	Output Capacitance			745		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			473		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		3.1	4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-15A		88.8	120	nC
Q <sub>g(4.5V)</sub>	Gate Charge			45.2	60	nC
Q <sub>gs</sub>	Gate Source Charge			10.1		nC
Q <sub>gd</sub>	Gate Drain Charge			19.4		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =1.7Ω, R <sub>GEN</sub> =3Ω		12		ns
t <sub>r</sub>	Turn-On Rise Time			11.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			100		ns
t <sub>f</sub>	Turn-Off Fall Time			40		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-15A, dI/dt=100A/μs		46.6	60	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-15A, dI/dt=100A/μs		67.7		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

Rev 1. June 2006

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

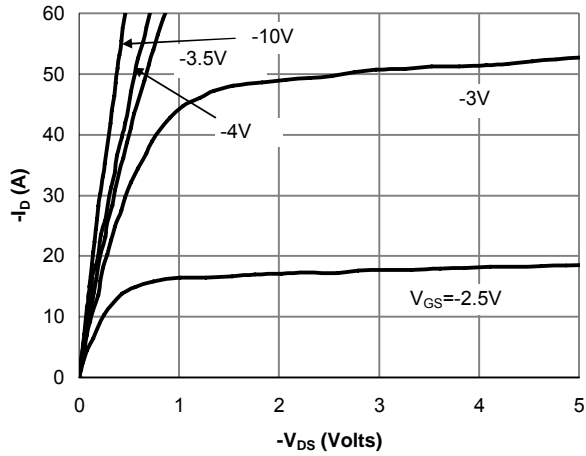


Fig 1: On-Region Characteristics

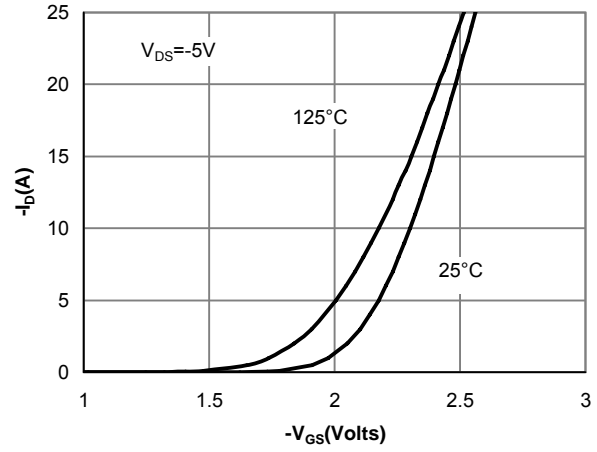


Figure 2: Transfer Characteristics

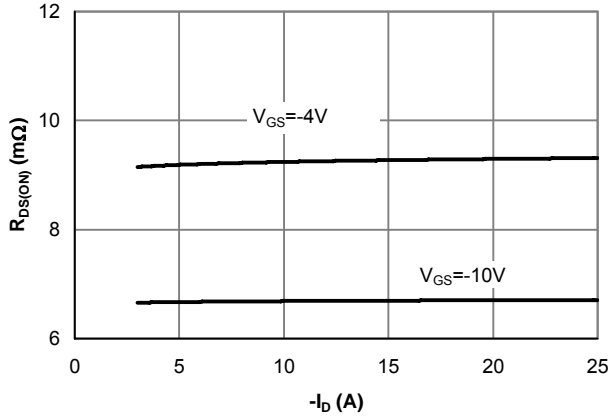


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

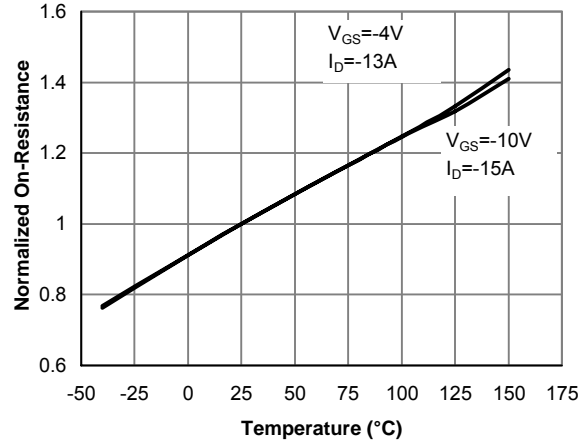


Figure 4: On-Resistance vs. Junction Temperature

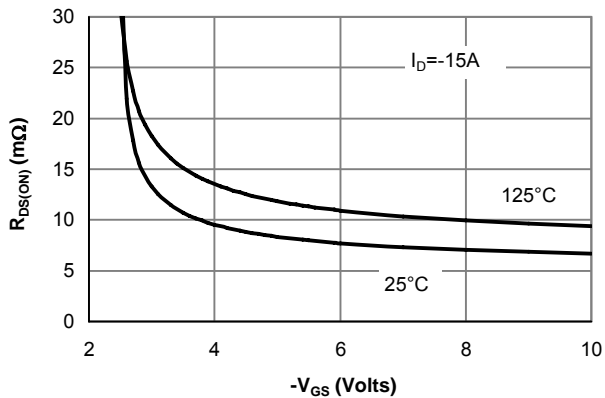


Figure 5: On-Resistance vs. Gate-Source Voltage

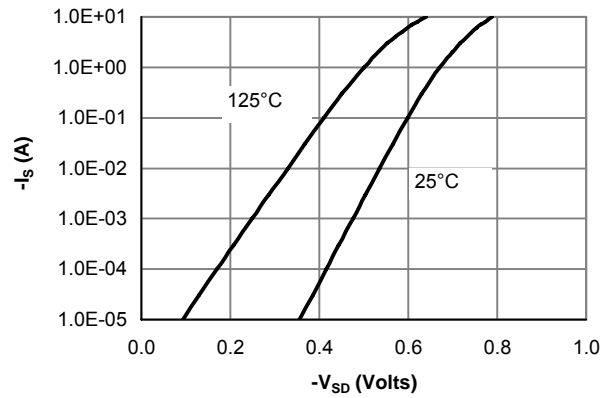


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

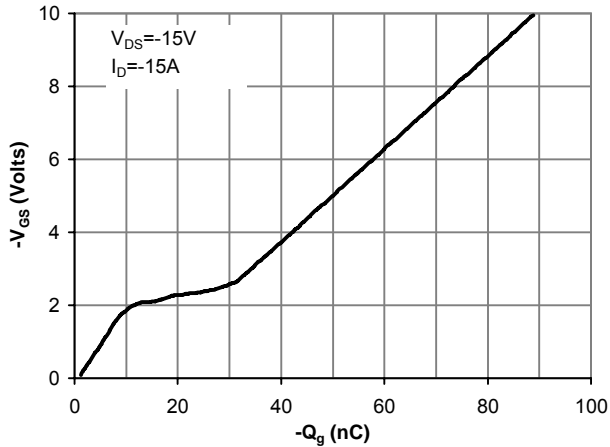


Figure 7: Gate-Charge Characteristics

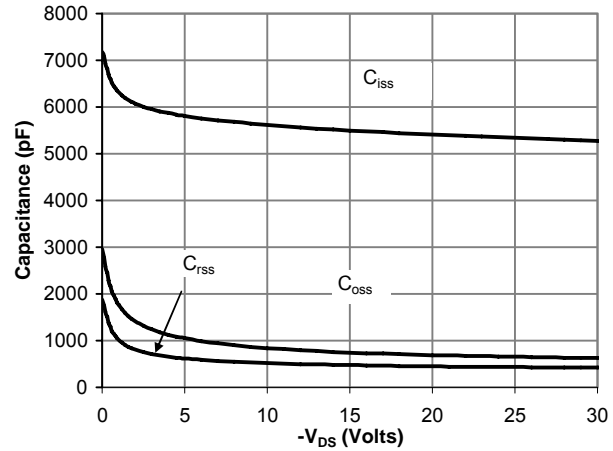


Figure 8: Capacitance Characteristics

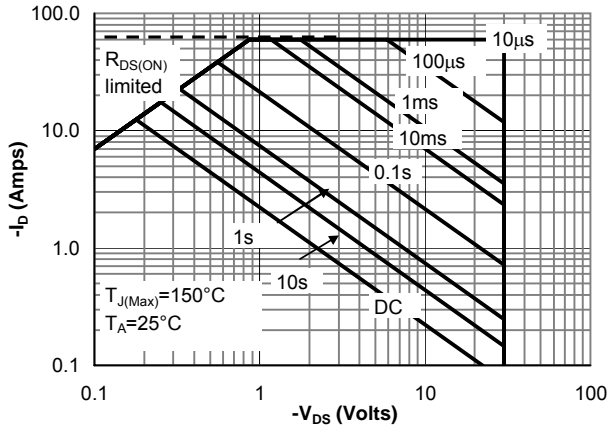


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

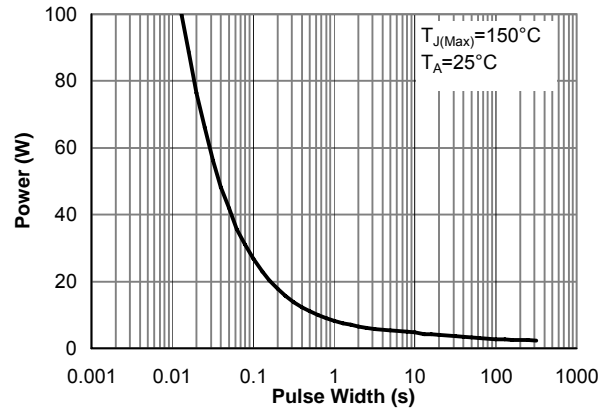


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

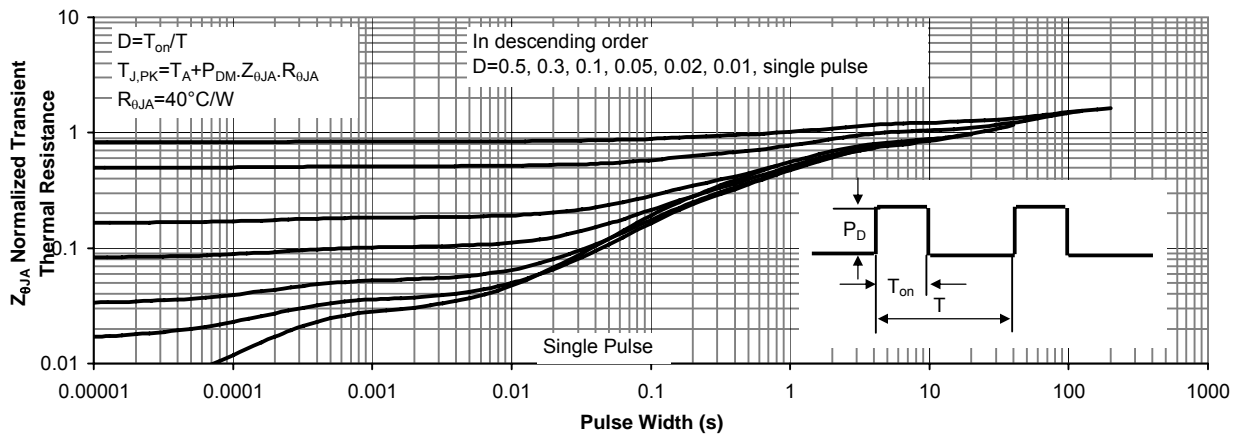
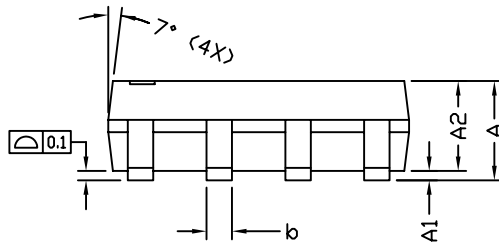
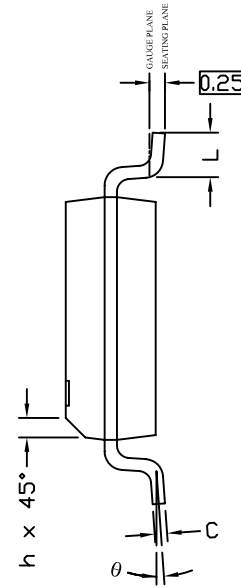
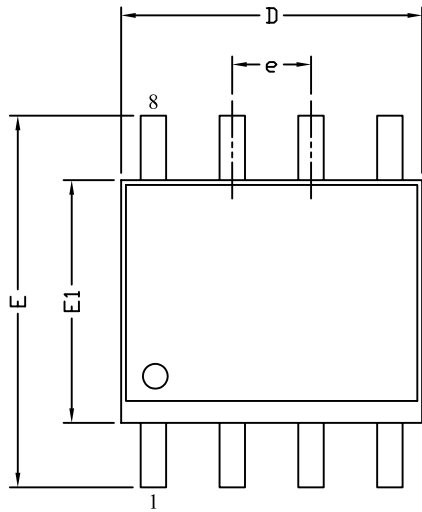


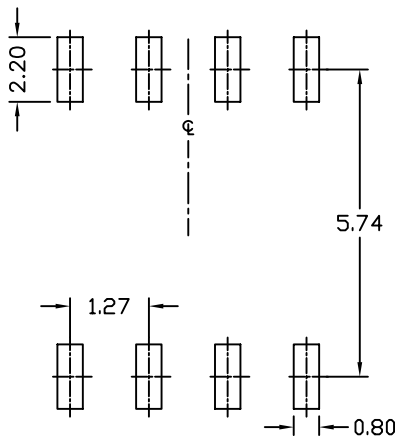
Figure 11: Normalized Maximum Transient Thermal Impedance



### SO-8L PACKAGE OUTLINE



### RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	---	0.25	0.004	---	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	---	0.51	0.012	---	0.020
c	0.17	---	0.25	0.007	---	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	---	0.50	0.010	---	0.020
L	0.40	---	1.27	0.016	---	0.050
$\theta$	$0^\circ$	---	$8^\circ$	$0^\circ$	---	$8^\circ$

UNIT: mm

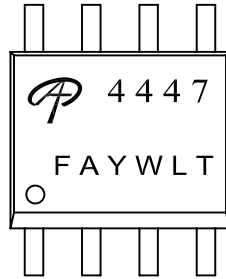
#### NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.



Document No.	PD-00427
Version	B
Title	AO4447 Marking Description

SO-8 PACKAGE MARKING DESCRIPTION



Standard product



Green product

NOTE:

LOGO - AOS Logo  
4447 - Part number code  
F - Fab code  
A - Assembly location code  
Y - Year code  
W - Week code  
L&T - Assembly lot code

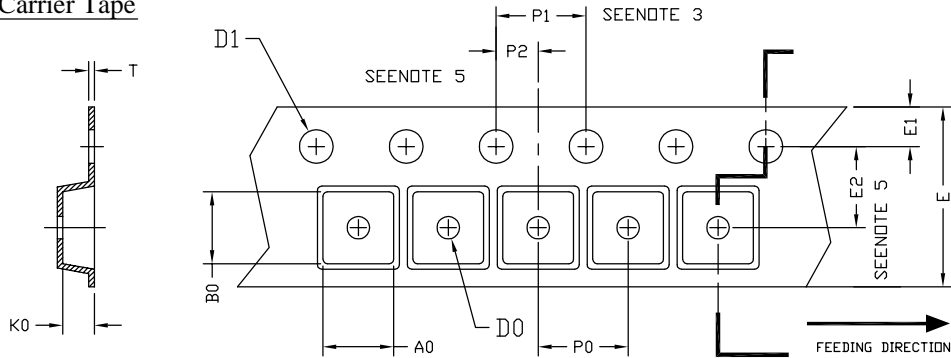
PART NO.	DESCRIPTION	CODE
AO4447	Standard product	4447
AO4447L	Green product	<u>4447</u>



**ALPHA & OMEGA**  
SEMICONDUCTOR, LTD.

## SO-8 Tape and Reel Data

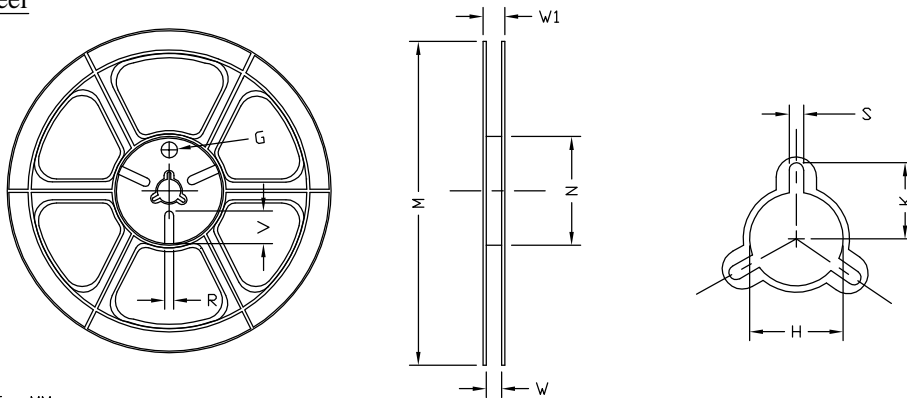
### SO-8 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SD-8 (12 mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 +0.10	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

### SO-8 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

### SO-8 Tape

Leader / Trailer  
& Orientation

