W39L040A Data Sheet

winbond

512K × 8 CMOS FLASH MEMORY

Table of Contents-

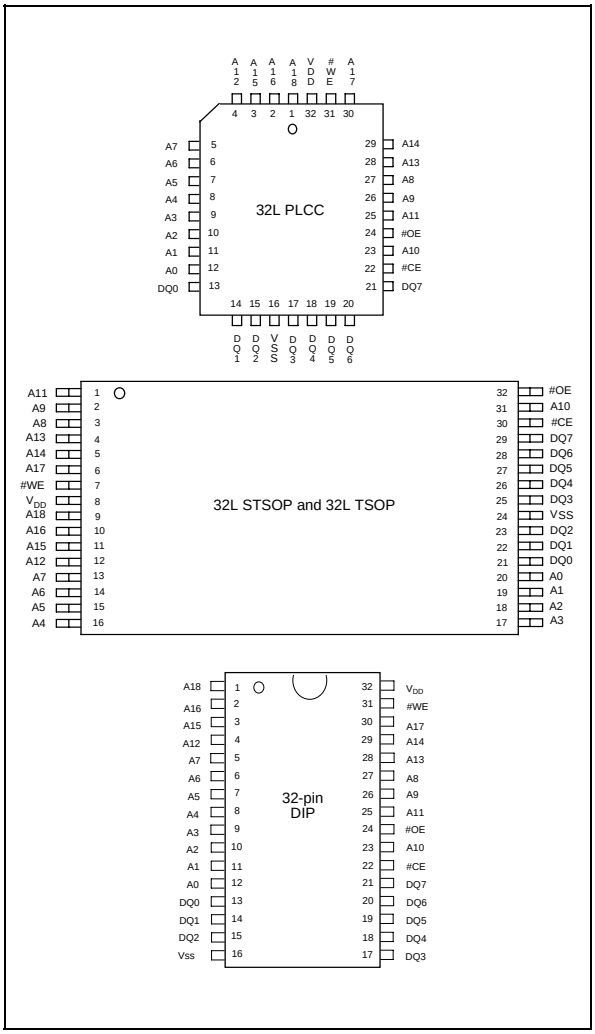
1. GENERAL DESCRIPTION

The W39L040A is a 4Mbit, 3V/3.3V CMOS flash memory organized as 512K × 8 bits. For flexible erase capability, the 4Mbits of data are divided into 8 uniform sectors of 64 Kbytes. The byte-wide (× 8) data appears on DQ7 – DQ0. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W39L040A results in fast program/erase operations with extremely low current consumption (compared to other comparable 3.3-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

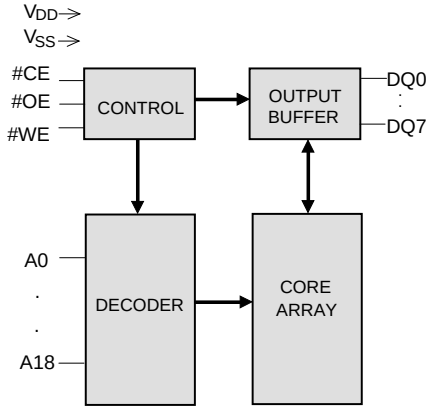
2. FEATURES

- 3V/3.3-Volt Read/Erase/Program Operations
  - 3.0 ~ 3.6V for 70nS
  - 2.7 ~ 3.6V for 90nS
- Fast Program operation:
  - Byte-by-Byte programming: 9 μS (typ.)
- Fast Erase operation:
  - Chip Erase cycle time: 6 S (typ.)
  - Sector Erase cycle time: 0.7 S (typ.)
- Read access time: 70/90 nS
- 8 Even sectors with 64K bytes
- Any individual sector can be erased
- Typical program/erase cycles: 10K
- Twenty-year data retention
- Low power consumption
  - Active read current: 7 mA at 5MHz (typ.)
  - Active program/erase current: 15 mA at 5MHz (typ.)
  - Standby current: 0.2 μA (typ.)
- End of program detection
  - Software method: Toggle bit/#Data polling
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin PLCC Lead free, 32-pin STSOP (8 x 14 mm) Lead free, 32-pin PDIP and 32-pin TSOP (8 x 20 mm)

3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	PIN NAME
A0 – A18	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
#CE	Chip Enable
#OE	Output Enable
#WE	Write Enable
VDD	Power Supply
VSS	Ground

6. FUNCTIONAL DESCRIPTION

6.1 Device Bus Operation

6.1.1 Read Mode

The read operation of the W39L040A is controlled by #CE and #OE, both of which have to be low for the host to obtain data from the outputs. #CE is used for device selection. When #CE is high, the chip is de-selected and only standby power will be consumed. #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either #CE or #OE is high. Refer to the timing waveforms for further details.

6.1.2 Write Mode

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing #WE to logic low state; while #CE is at logic low state and #OE is at logic high state. Addresses are latched on the falling edge of #WE or #CE, whichever happens later; while data is latched on the rising edge of #WE or #CE, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Program Waveforms for specific timing parameters.

6.1.3 Standby Mode

The Standby mode is achieved with the #CE input held at V_{DD} ±0.3V and the current is typically reduced to less than 5μA (max).

In the standby mode the outputs are in the high impedance state, independent of the #OE input.

6.1.4 Output Disable Mode

With the #OE input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

6.1.5 Auto-select Mode

The auto-select mode allows the reading of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5V to 12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don′t cares except A0 and A1 (see "Auto-select Codes").

The manufacturer and device codes may also be read via the command register, for instance, when the W39L040A is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in "Auto-select Codes".

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (Winbond = DAH) and byte 1 (A0 = V_{IH}) the device identifier code (W39L040A = D6hex). All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the Auto-select, A1 must be low state.

6.2 Data Protection

The W39L040A is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from V_{DD} power-up and power-down transitions or system noise.

6.2.1 Low V_{DD} Inhibit

To avoid initiation of a write cycle during V_{DD} power-up and power-down, the W39L040A locks out when V_{DD} < 2.0V (see DC Characteristics section for voltages). The write and read operations are inhibited when V_{DD} is less than 2.0V typical. The W39L040A ignores all write and read operations until V_{DD} > 2,0V. The user must ensure that the control pins are in the correct logic state when V_{DD} > 2.0V to prevent unintentional writes.

6.2.2 Write Pulse "Glitch" Protection

Noise pulses of less than 10 nS (typical) on #OE, #CE, or #WE will not initiate a write cycle.

6.2.3 Logical Inhibit

Writing is inhibited by holding any one of #OE = V_{IL}, #CE = V_{IH}, or #WE = V_{IH}. To initiate a write cycle #CE and #WE must be a logical zero while #OE is a logical one.

6.2.4 Power-up Write and Read Inhibit

Power-up of the device with #WE = #CE = V_{IL} and #OE = V_{IH} will not accept commands on the rising edge of #WE except 5mS delay (see the power up timing in AC Characteristics). The internal state machine is automatically reset to the read mode on power-up.

6.3 Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. "Command Definitions" defines the valid register command sequences.

6.3.1 Read Command

The device will automatically power-up in the read state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition.

The device will automatically returns to read state after completing an Embedded Program or Embedded Erase algorithm.

Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

6.3.2 Auto-select Command

Flash memories are intended for use in applications where the local CPU can alter memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desirable system design practice.

The device contains an auto-select command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the auto-select command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of DAH. A read cycle from address XX01H returns the device code (W39L040A = D6hex).

To terminate the operation, it is necessary to write the auto-select exit command sequence into the register.

6.3.3 Byte Program Command

The device is programmed on a byte-by-byte basis. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two "unlock" write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded program algorithm. Addresses are latched on the falling edge of #CE or #WE, whichever happens later and the data is latched on the rising edge of #CE or #WE, whichever happens first. The rising edge of #CE or #WE (whichever happens first) begins programming using the Embedded Program Algorithm. Upon executing the algorithm, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 (also used as #Data Polling) is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (see "Hardware Sequence Flags"). Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time for #Data Polling operations. #Data Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during the Embedded Program Algorithm will be ignored. If a hardware reset occurs during the programming operation, the data at that particular location will be corrupted.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to program 0 back to 1, the toggle bit will stop toggling. Only erase operations can convert "0"s to "1"s.

Refer to the Programming Command Flow Chart using typical command strings and bus operations.

6.3.4 Chip Erase Command

Chip erase is a six-bus-cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles are asserted, followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically erase and verify the entire memory for an all one data pattern. The erase is performed sequentially on each sectors at the

same time (see "Feature"). The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last #WE pulse in the command sequence and terminates when the data on DQ7 is "1" at which time the device returns to read the mode.

Refer to the Erase Command Flow Chart using typical command strings and bus operations.

6.3.5 Sector Erase Command

Sector erase is a six-bus-cycle operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of #WE, while the command (30H) is latched on the rising edge of #WE.

Sector erase does not require the user to program the device prior to erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last sector erase command pulse and terminates when the data on DQ7, #Data Polling, is "1" at which time the device returns to the read mode. #Data Polling must be performed at an address within any of the sectors being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

6.4 Write Operation Status

6.4.1 DQ7: #Data Polling

The W39L040A device features #Data Polling as a method to indicate to the host that the embedded algorithms are in progress or completed.

During the Embedded Program Algorithm, an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7.

During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a "1" at the DQ7 output.

For chip erase, the #Data Polling is valid after the rising edge of the sixth pulse in the six #WE write pulse sequences. For sector erase, the #Data Polling is valid after the last rising edge of the sector erase #WE pulse. #Data Polling must be performed at sector addresses within any of the sectors being erased. Otherwise, the status may not be valid.

Just prior to the completion of Embedded Algorithm operations DQ7 may change asynchronously while the output enable (#OE) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte′s valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operations and DQ7 has a valid data, the data outputs on DQ0 – DQ6 may be still invalid. The valid data on DQ0 – DQ7 will be read on the successive read attempts.

The #Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see "Command Definitions").

6.4.2 DQ6: Toggle Bit

The W39L040A also features the "Toggle Bit" as a method to indicate to the host system that the embedded algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read (#OE toggling) data from the device at any address will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth #WE pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth #WE pulse in the six write pulse sequence. For sector erase, the Toggle Bit is valid after the last rising edge of the sector erase #WE pulse. The Toggle Bit is active during the sector erase time-out.

Either #CE or #OE toggling will cause DQ6 to toggle.

6.5 Table of Operating Modes

6.5.1 Device Bus Operations

(V_{ID} = 12 ±0.5V)

MODE	PIN						
	#CE	#OE	#WE	A0	A1	A9	DQ0 – DQ7
Read	V_{IL}	V_{IL}	V_{IH}	A0	A1	A9	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A0	A1	A9	Din
Standby	V_{IH}	X	X	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	X	X	High Z/Dout
	X	X	V_{IH}	X	X	X	High Z/Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Auto select Manufacturers ID	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Code
Auto select Device ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	Code

6.5.2 Auto-select Codes (High Voltage Method)

(V_{ID} = 12 ±0.5V)

DESCRIPTION	#CE	#OE	#WE	A9	THE OTHER ADDRESS	DQ[7:0]
Manufacturer ID: Winbond	V_{IL}	V_{IL}	V_{IH}	V_{ID}	All Address = V_{IL}	DAhex
Device ID: W39L040A	V_{IL}	V_{IL}	V_{IH}	V_{ID}	A1 = V_{IH}, All other = V_{IL}	D6hex

6.5.3 Sector Address Table

SECTOR	A18	A17	A16	SECTOR SIZE (KBYTES)	ADDRESS
SA0	0	0	0	64	00000h – 0FFFFh
SA1	0	0	1	64	10000h – 1FFFFh
SA2	0	1	0	64	20000h – 2FFFFh
SA3	0	1	1	64	30000h – 3FFFFh
SA4	1	0	0	64	40000h – 4FFFFh
SA5	1	0	1	64	50000h – 5FFFFh
SA6	1	1	0	64	60000h – 6FFFFh
SA7	1	1	1	64	70000h – 7FFFFh

Note: All sectors are 64K bytes in size.

6.5.4 Command Definitions

COMMAND DESCRIPTION	NO. OF Cycles	1ST CYCLE		2ND CYCLE		3RD CYCLE		4TH CYCLE		5TH CYCLE		6TH CYCLE	
		Addr. (1)	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read	1	A_{IN}	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA(3)	30
Byte Program	4	5555	AA	2AAA	55	5555	A0	A_{IN}	D_{IN}				
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit (2)	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit (2)	1	XXXX	F0										

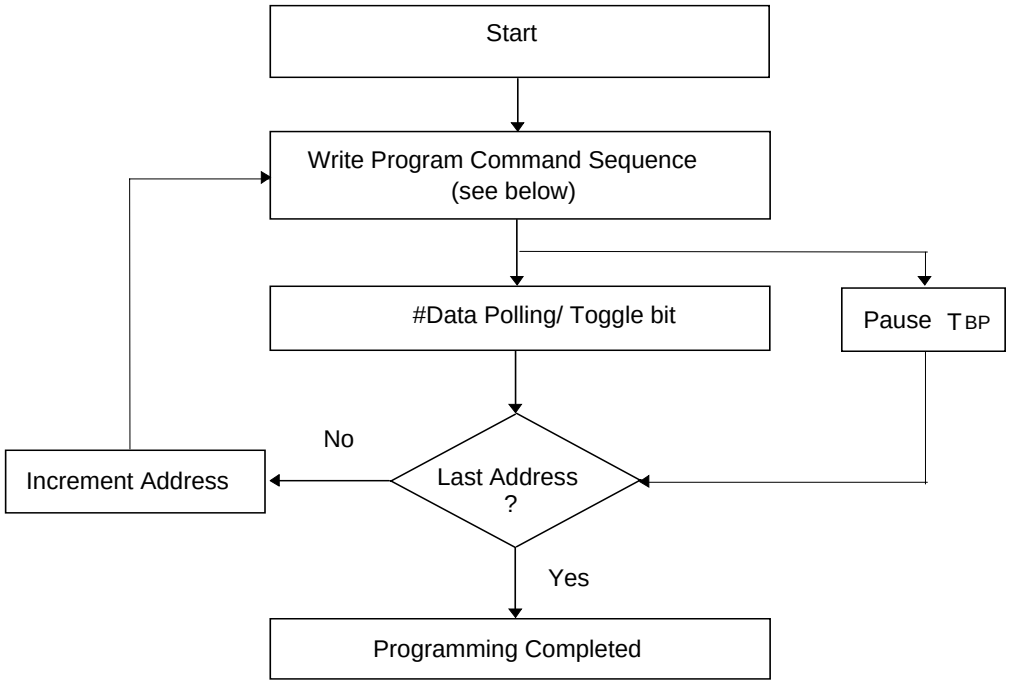
Notes:

1. Address Format: A14 – A0 (Hex); Data Format: DQ7 – DQ0 (Hex)
2. Either one of the two Product ID Exit commands can be used.
3. SA: Sector Address

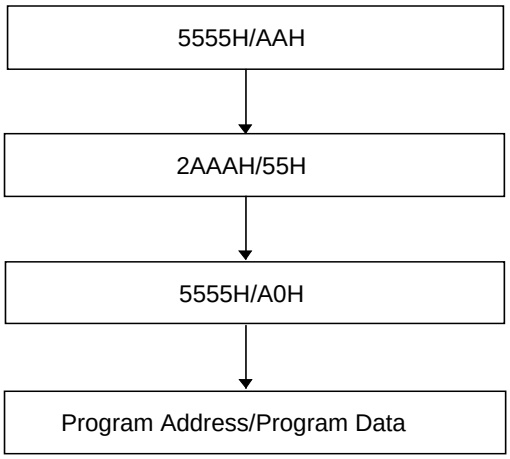
   SA = 7XXXXh for Unique Sector7
   SA = 6XXXXh for Unique Sector6
   SA = 5XXXXh for Unique Sector5
   SA = 4XXXXh for Unique Sector4
   SA = 3XXXXh for Unique Sector3
   SA = 2XXXXh for Unique Sector2
   SA = 1XXXXh for Unique Sector1
   SA = 0XXXXh for Unique Sector0

4. XX: Don't care

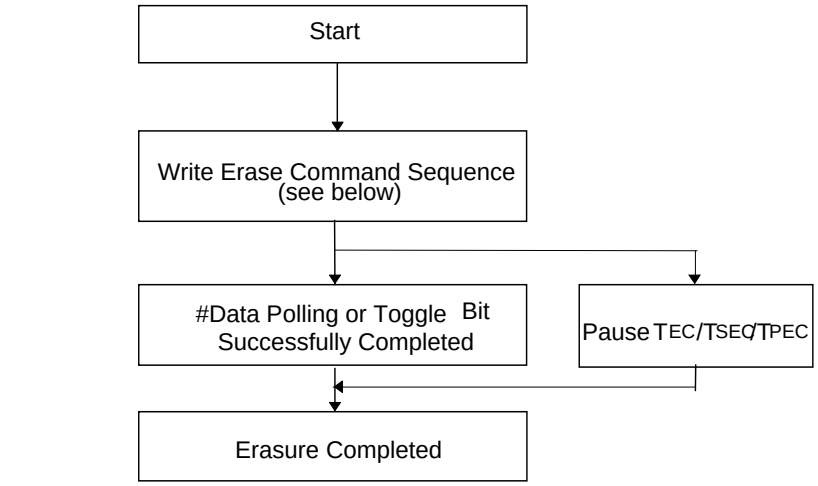
6.6 Embedded Programming Algorithm



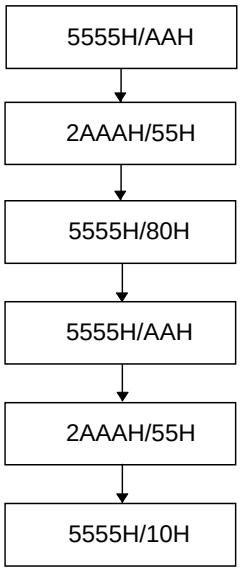
Program Command Sequence (Address/Command):



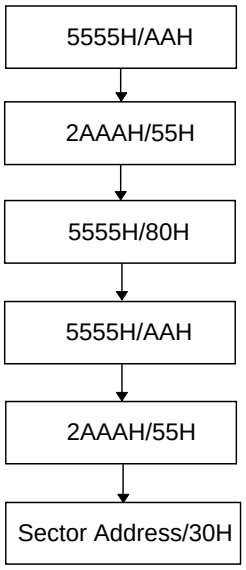
6.7 Embedded Erase Algorithm



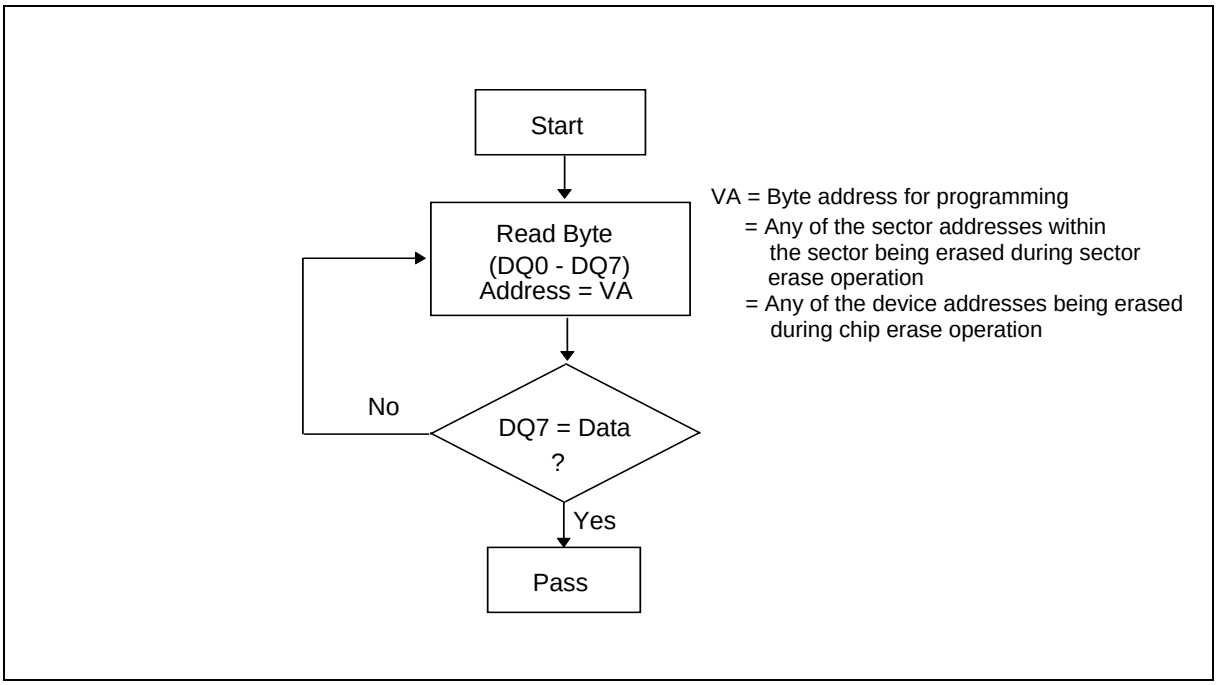
Chip Erase Command Sequence (Address/Command):



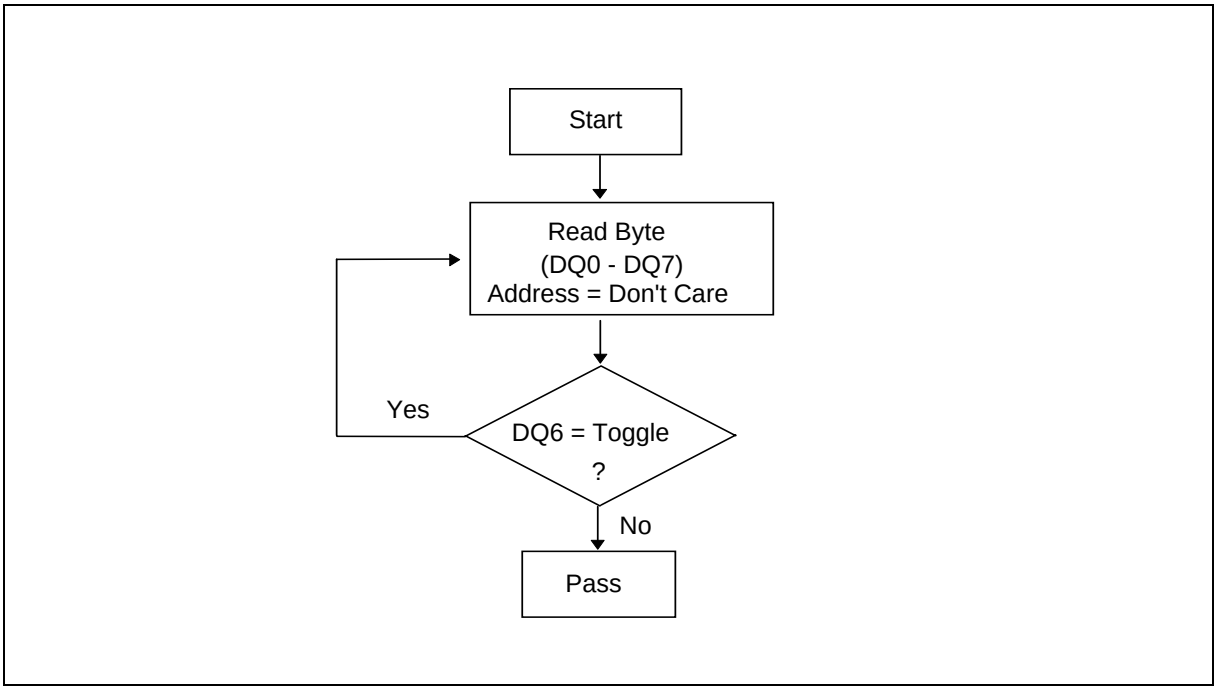
Individual Sector Erase Command Sequence (Address/Command):



6.8 Embedded #Data Polling Algorithm



6.9 Embedded Toggle Bit Algorithm



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
Power Supply Voltage to V_{SS} Potential	-0.5 to V_{DD}+0.5	V
Voltage on Any Pin to Ground Potential except A9	-0.5 to +4.0	V
Voltage on A9, #OE Pin to Ground Potential	-0.5 to +12.5	V

Note: Exposure to conditions beyond those listed under Absolute maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC Operating Characteristics

(V_{DD} = 3.0 ~ 3.6V for 70 nS or V_{DD} = 2.7 ~ 3.6V for 90 nS, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Read Current	I_{DD1}	#CE = V_{IL}, #OE = V_{IH}, at f = 5 MHz	-	7	12	mA
Power Supply Write Current	I_{DD2}	#CE = V_{IL}, #OE = V_{IH}	-	15	30	mA
Standby V_{DD} Current	I_{SB}	#CE = V_{DD} ± 0.3V	-	0.2	5	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max.	-	-	±1	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}, V_{DD} = V_{DD} max.	-	-	±1	µA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	0.7 x V_{DD}	-	V_{DD} +0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, V_{DD} = V_{DD} min.	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{DD} = V_{DD} min.	0.85 V_{DD}	-	-	V
	V_{OH2}	I_{OH} = -100 µA, V_{DD} = V_{DD} min.	V_{DD} -0.4	-	-	V

7.3 Pin Capacitance

(V_{DD} = 3.3V for 70 nS, or V_{DD} = 3.0V for 90 nS, T_A = 25° C, f = 1 MHz)

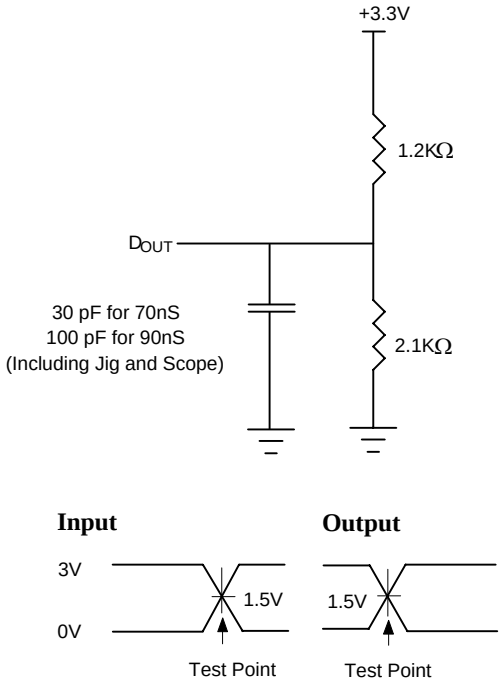
PARAMETER	SYMBOL	CONDITIONS	TYP.	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	7.5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	8.5	12	pF

7.4 AC Characteristics

7.4.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate C_L = 30pF for 70nS/ 100pF for 90nS

7.4.2 AC Test Load and Waveform



AC Characteristics, continued

7.4.3 Read Cycle Timing Parameters

(V_{DD} = 3.0 ~ 3.6V for 70 nS or V_{DD} = 2.7 ~ 3.6V for 90 nS, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	70 nS		90 nS		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	nS
Address Access Time	T_{AA}	-	70	-	90	nS
Output Enable Access Time	T_{OE}	-	30	-	35	nS
#CE High to High-Z Output	T_{CHZ}	-	16	-	16	nS
#OE High to High-Z Output	T_{OHZ}	-	16	-	16	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

7.4.4 Erase/Program Cycle Timing Parameters

PARAMETER	SYM.	70 nS			90 nS			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	T_{WC}	70	-	-	90	-	-	nS
Address Setup Time	T_{AS}	0	-	-	0	-	-	nS
Address Hold Time	T_{AH}	45	-	-	45	-	-	nS
#CE Setup Time	T_{CS}	0	-	-	0	-	-	nS
#CE Hold Time	T_{CH}	0	-	-	0	-	-	nS
#OE Setup Time	T_{OES}	0	-	-	0	-	-	nS
#WE Pulse Width	T_{WP}	35	-	-	35	-	-	nS
#WE High Width	T_{WPH}	30	-	-	30	-	-	nS
Data Setup Time	T_{DS}	35	-	-	45	-	-	nS
Data Hold Time	T_{DH}	0	-	-	0	-	-	nS
Byte Programming Time	T_{BP}	-	9	200	-	9	200	µS
Chip Programming Time	T_{CP}	-	4.5	13.5	-	4.5	13.5	S
Chip Erase Cycle Time	T_{EC}	-	6	50	-	6	50	S
Sector Erase Cycle Time	T_{EP}	-	0.7	6	-	0.7	6	S

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is V_{IH} and (b) low level signal's reference level is V_{IL}.

AC Characteristics, continued

7.4.5 Power-up Timing

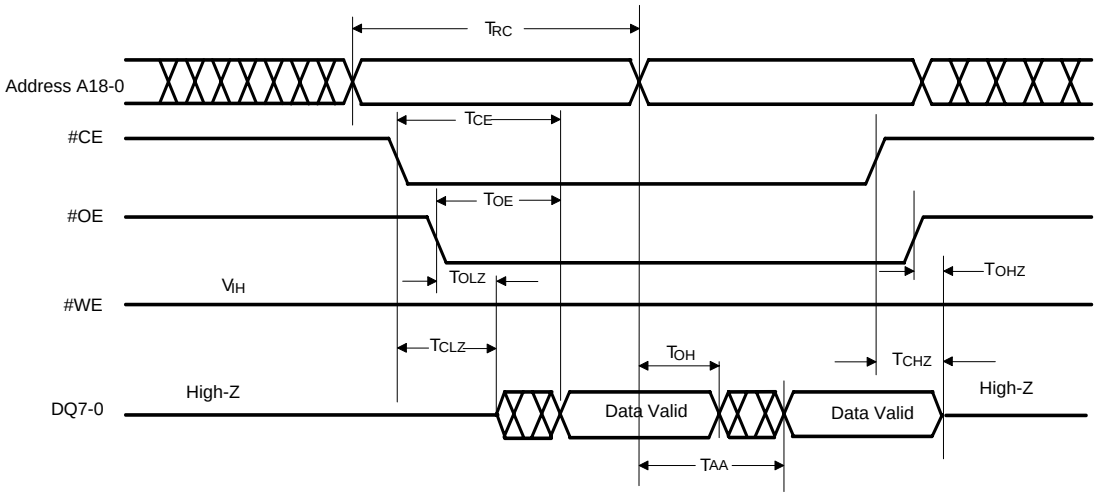
PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	μS
Power-up to Write Operation	TPU. WRITE	5	mS

7.4.6 #Data Polling and Toggle Bit Timing Parameters

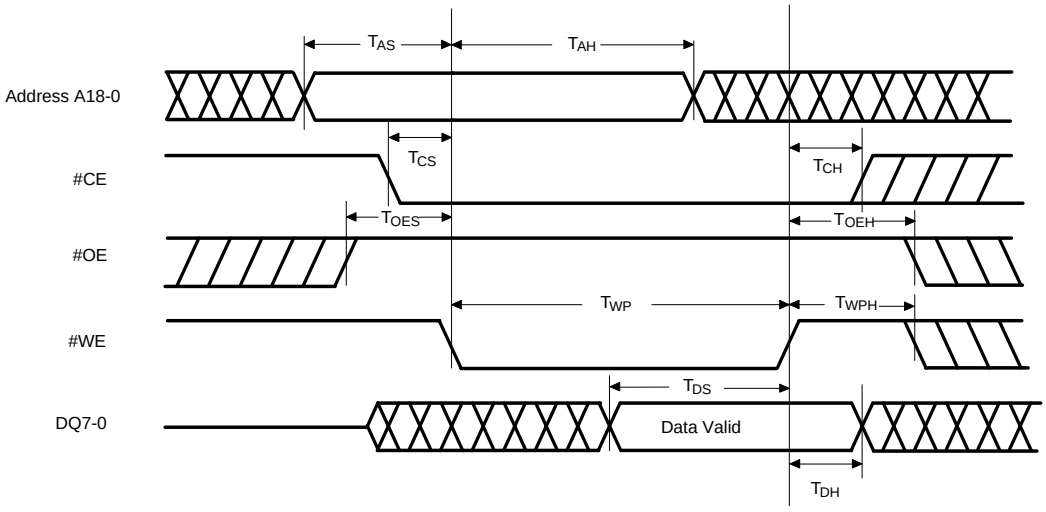
PARAMETER	SYM.	70 nS		90 nS		UNIT
		MIN.	MAX.	MIN.	MAX.	
#OE to #Data Polling Output Delay	TOEP	10	-	10	-	nS
#CE to #Data Polling Output Delay	TCEP	-	70	-	90	nS
#OE to Toggle Bit Output Delay	TOET	10	-	10	-	nS
#CE to Toggle Bit Output Delay	TCET	-	70	-	90	nS

8. TIMING WAVEFORMS

8.1 Read Cycle Timing Diagram

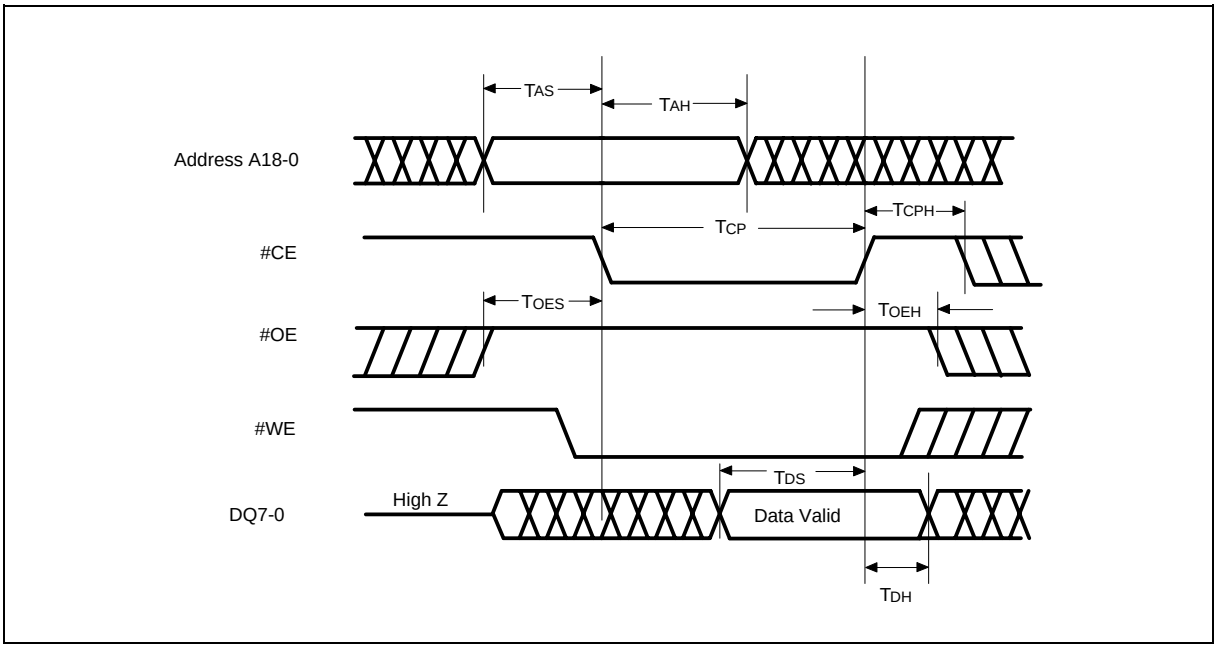


8.2 #WE Controlled Command Write Cycle Timing Diagram

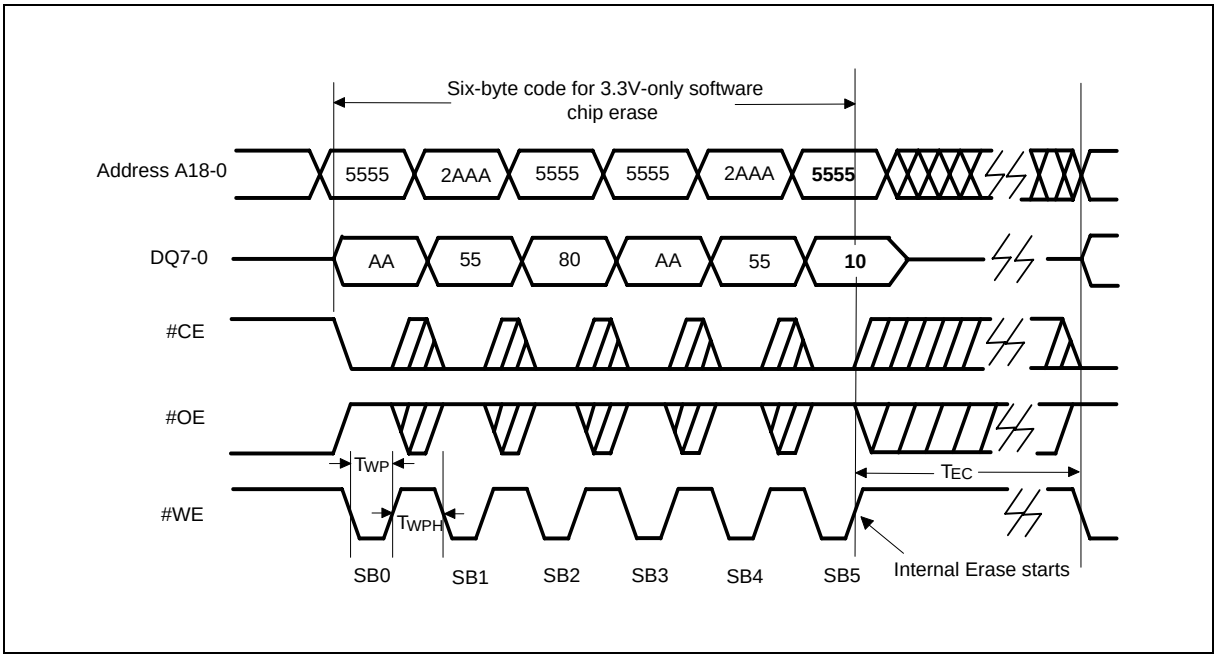


Timing Waveforms, continued

8.3 #CE Controlled Command Write Cycle Timing Diagram

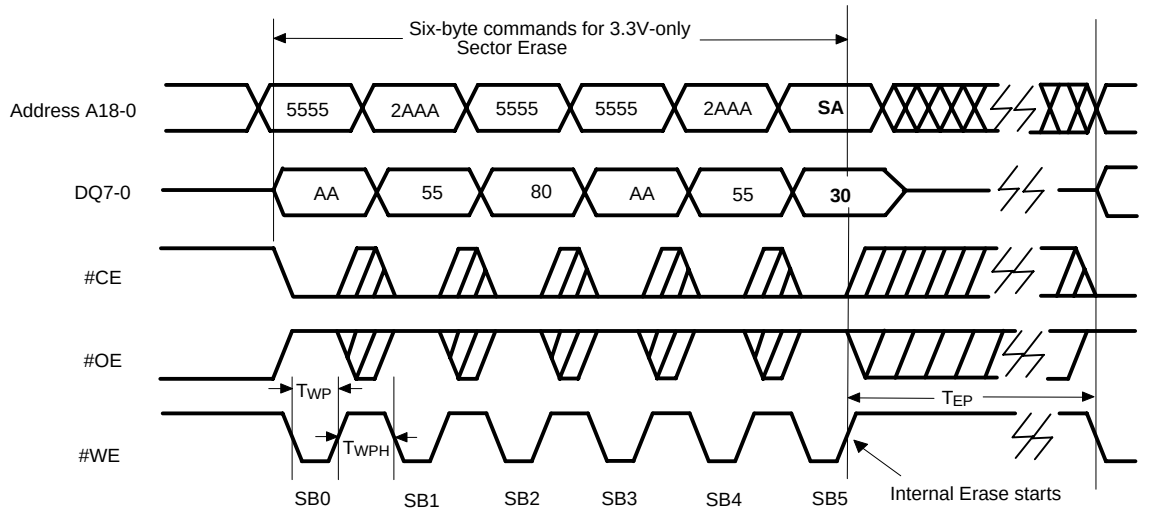


8.4 Chip Erase Timing Diagram



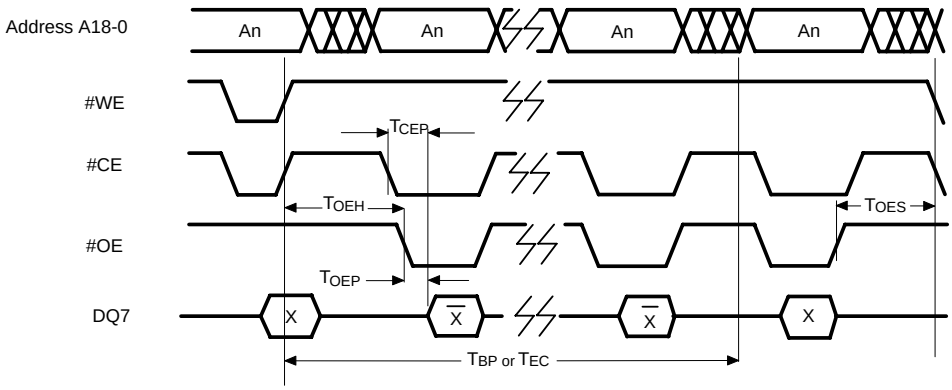
Timing Waveforms, continued

8.5 Sector Erase Timing Diagram



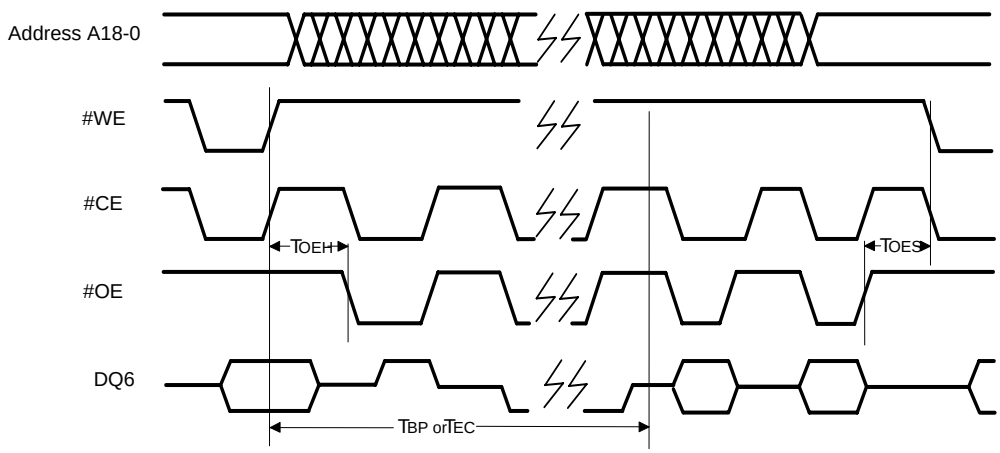
SA = Sector Address

8.6 #Data Polling Timing Diagram



Timing Waveforms, continued

8.7 Toggle Bit Timing Diagram



9. ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (µA)	PACKAGE	OPERATING TEMP. (°C)	CYCLE
W39L040AP70B	70	12	5	32L PLCC	0 – 70	10K
W39L040AP90B	90	12	5	32L PLCC	0 – 70	10K
W39L040AQ70B	70	12	5	32L STSOP (8x14 mm)	0 – 70	10K
W39L040AQ90B	90	12	5	32L STSOP (8x14 mm)	0 – 70	10K
W39L040AT70B	70	12	5	32L TSOP (8 x 20 mm)	0 – 70	10K
W39L040AT90B	90	12	5	32L TSOP (8 x 20 mm)	0 – 70	10K
W39L040A70B	70	12	5	32L PDIP	0 – 70	10K
W39L040A90B	90	12	5	32L PDIP	0 – 70	10K
W39L040AT70Z	70	12	5	32L TSOP (8 x 20 mm) Lead free	0 – 70	10K
W39L040AT90Z	90	12	5	32L TSOP (8 x 20 mm) Lead free	0 – 70	10K
W39L040AP70Z	70	12	5	32L PLCC Lead free	0 – 70	10K
W39L040AP90Z	90	12	5	32L PLCC Lead free	0 – 70	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

10. HOW TO READ THE TOP MARKING

Example: The top marking of 32-pin TSOP W39L040AT-70

1st line: Winbond logo

2nd line: the part number: W39L040AT70B

3rd line: the lot number

4th line: the tracking code: 325 O B SA

325: Packages made in '03, week 25

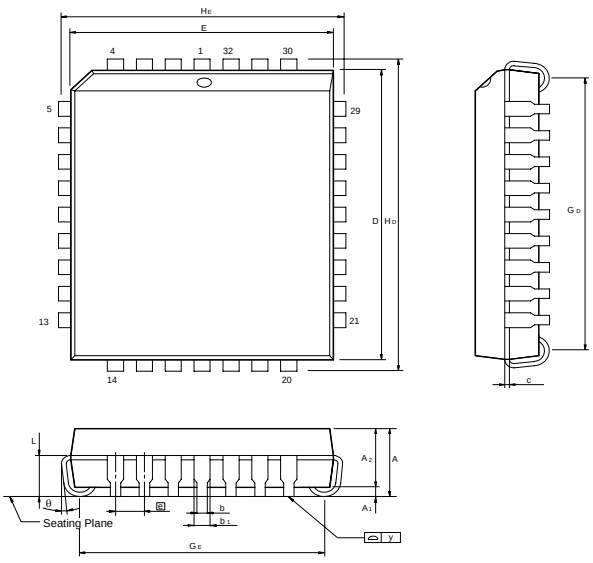
O: Assembly house ID: A means ASE, O means OSE, ...etc.

B: IC revision; A means version A, B means version B, ...etc.

FA: Process code

11. PACKAGE DIMENSIONS

11.1 32L PLCC

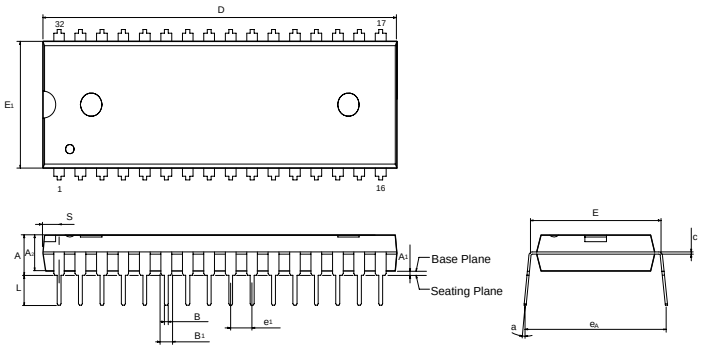


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

11.2 32L PDIP

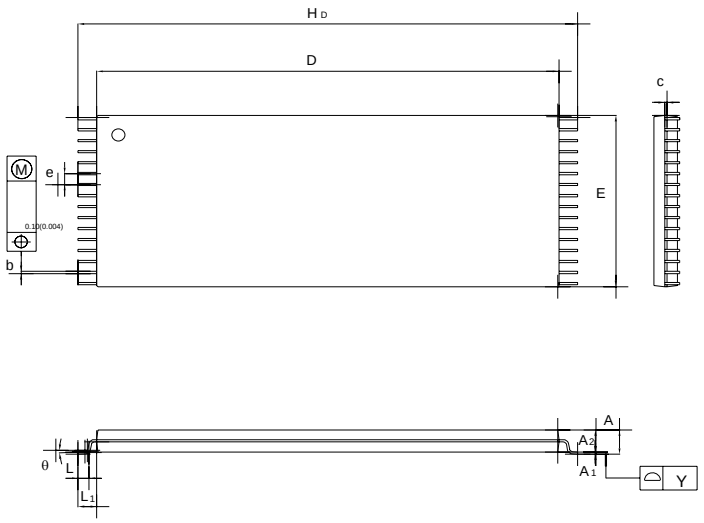


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches
6. General appearance spec. should be based on final visual inspection spec.

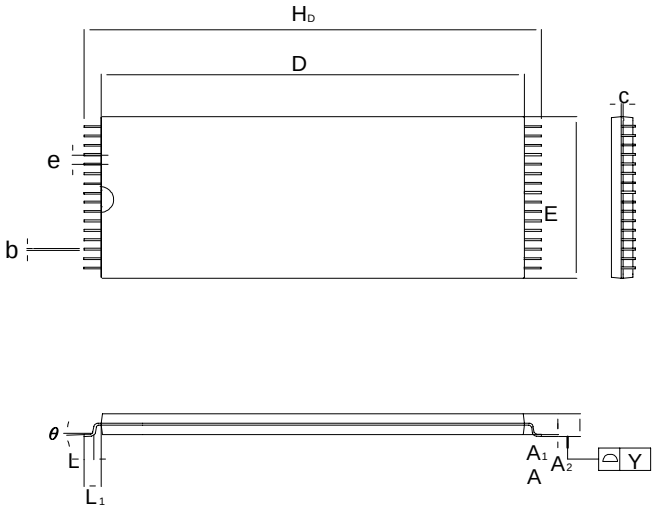
11.3 32L TSOP (8 x 20 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:
Controlling dimension: Millimeters

11.4 32L STSOP (8 x 14 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

12. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Sep. 24, 2004	-	Initial Issued
A2	Nov. 25, 2004	3, 24, 25	Added 32L PDIP and 32L TSOP package dimensions
A3	April 14,2005	26	Add important notice

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.