# HA16158P/FP

PFC & PWM Control IC

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## Description

The HA16158 is a power supply controller IC combining an AC-DC converter switching controller for power factor correction and an off-line power supply switching controller. The PFC (power factor correction) section employs average current mode PWM and the off-line power supply control section employs peak current mode PWM.

The HA16158 allows the operating frequency to be varied with a single timing resistance, enabling it to be used for a variety of applications.

The PFC operation can be turned on and off by an external control signal. Use of this on/off function makes it possible to disable PFC operation at a low line voltage, or to perform remote control operation from the transformer secondary side.
The PWM controller includes a power-saving function that reduces the operating frequency to a maximum of 1/64 in the standby state, greatly decreasing switching loss.

The PFC section and PWM section are each provided with a soft start control pin, enabling a soft start time to be set easily.

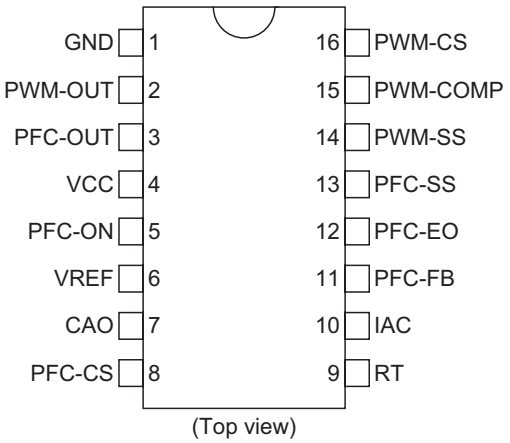
## Features

<Maximum Ratings>
- Supply voltage Vcc: 24 V
- Operating junction temperature Tjopr: –40°C to +125°C

<Electrical Characteristics>
- VREF output voltage VREF: 5.0 V ± 2%
- UVLO start threshold VH: 16.0 V ± 1.0 V
- UVLO shutdown threshold VL: 10.0 V ± 0.6 V
- PFC output maximum duty cycle Dmax-pfc: 95% typ.
- PWM output maximum duty cycle Dmax-pwm: 45% typ.

<Functions>
- Synchronized PFC and PWM timing
- PFC function on/off control
- PWM power-saving function (frequency reduced to maximum of 1/64)
- PWM overvoltage latch protection circuit
- Soft start control circuits for both PFC and PWM
- Package lineup: SOP-16/DILP-16

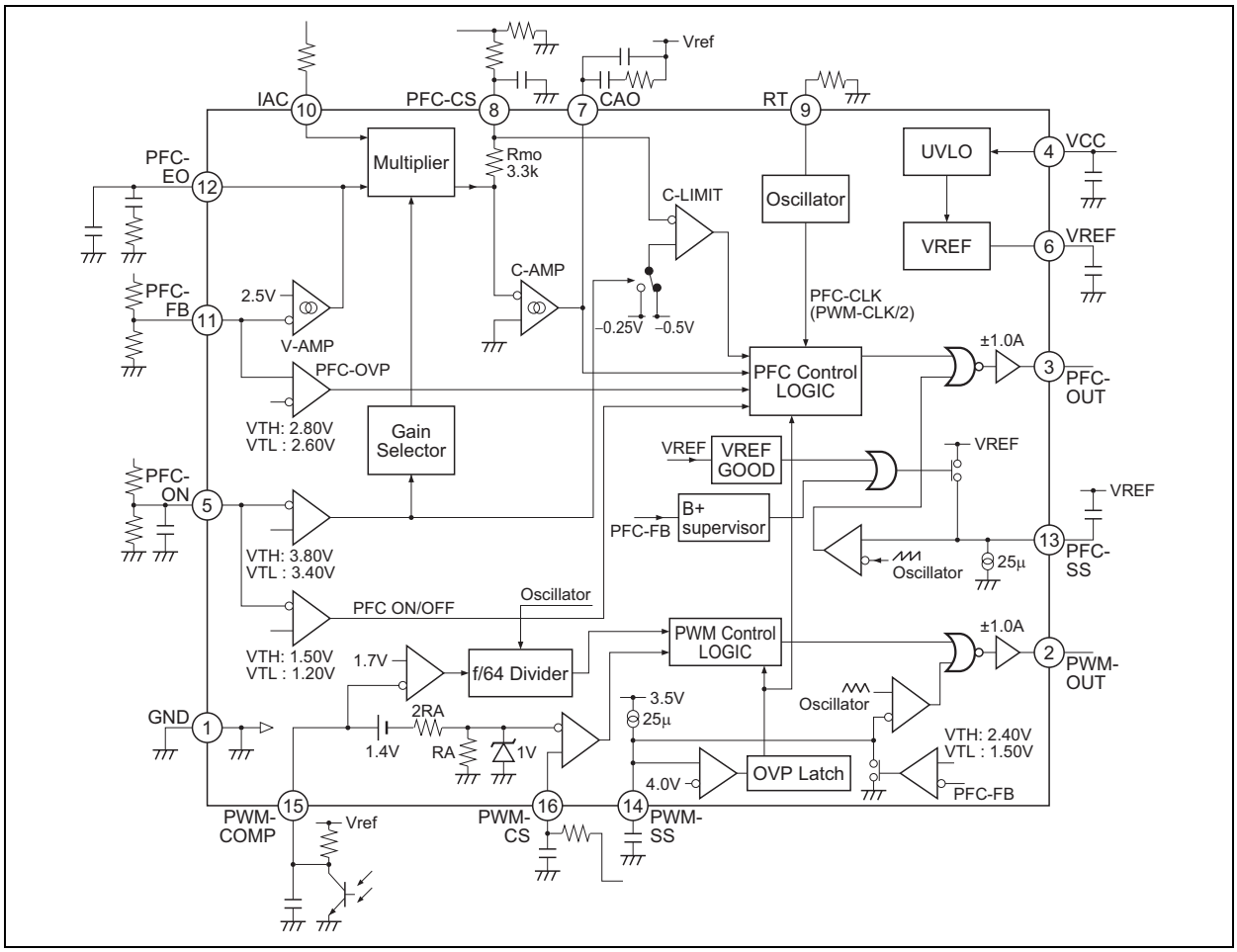
## Pin Arrangement




## Pin Functions

| Pin No. | Pin Name | Pin Functions |
|---|---|---|
| 1 | GND | Ground |
| 2 | PWM-OUT | Power MOS FET driver output (PWM control) |
| 3 | PFC-OUT | Power MOS FET driver output (PFC control) |
| 4 | VCC | Supply voltage |
| 5 | PFC-ON | PFC function on/off signal input |
| 6 | VREF | Reference voltage |
| 7 | CAO | Average current control error amplifier output |
| 8 | PFC-CS | PFC control current sense signal input |
| 9 | RT | Operating frequency setting timing resistance connection |
| 10 | IAC | Multiplier reference current input |
| 11 | PFC-FB | PFC control error amplifier input |
| 12 | PFC-EO | PFC control error amplifier output |
| 13 | PFC-SS | PFC control soft start time setting capacitance connection |
| 14 | PWM-SS | PWM control soft start time setting capacitance connection |
| 15 | PWM-COMP | PWM control voltage feedback |
| 16 | PWM-CS | PWM control current sense signal input |

## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit | Note |
|---|---|---|---|---|
| Power supply voltage | Vcc | 24 | V | |
| PFC-OUT output current (peak) | Ipk-out1 | ±1.0 | A | 3 |
| PWM-OUT output current (peak) | Ipk-out2 | ±1.0 | A | 3 |
| PFC-OUT output current (DC) | Idc-out1 | ±0.1 | A | |
| PWM-OUT output current (DC) | Idc-out2 | ±0.1 | A | |
| Pin voltage | Vi-group1 | –0.3 to Vcc | V | 4 |
| | Vi-group2 | –0.3 to Vref | V | 5 |
| CAO pin voltage | Vcao | –0.3 to Veoh-ca | V | |
| PFC-EO pin voltage | Vpfc-eo | –0.3 to Veoh-pfc | V | |
| PFC-ON pin voltage | Vpfc-on | –0.3 to 7 | V | |
| RT pin current | Irt | 50 | μA | |
| IAC pin current | Iiac | 1 | mA | |
| PFC-CS pin voltage | Vi-cs | –1.5 to 0.3 | V | |
| VREF pin current | Io-ref | –20 | mA | |
| VREF pin voltage | Vref | –0.3 to Vref | V | |
| Operating junction temperature | Tj-opr | –40 to +125 | °C | 6 |
| Storage temperature | Tstg | –55 to +150 | °C | |

Notes: 1. Rated voltages are with reference to the GND (SGND, PGND) pin.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. Shows the transient current when driving a capacitive load.
4. Group1 is the rated voltage for the following pins:
   PFC-OUT, PWM-OUT
5. Group2 is the rated voltage for the following pins:
   PFC-FB, PWM-CS, PWM-COMP, IAC, PFC-SS, PWM-SS, RT
6. HA16158P (DILP): θja = 120°C/W
   HA16158FP (SOP): θja = 120°C/W
   This value is based on actual measurements on a 10% wiring density glass epoxy circuit board (40 mm × 40 mm × 1.6 mm).

## Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Supply | Start threshold | VH | 15.0 | 16.0 | 17.0 | V | |
| | Shutdown threshold | VL | 9.4 | 10.0 | 10.6 | V | |
| | UVLO hysteresis | $dV_{UVL}$ | 5.2 | 6.0 | 6.8 | V | |
| | Start-up current | Is | 160 | 220 | 280 | μA | Vcc = 14.8V |
| | Is temperature stability | dIs/dTa | – | –0.3 | – | %/°C | *1 |
| | Operating current | Icc | 5.5 | 7.0 | 8.5 | mA | IAC = 0A, CL = 0F |
| | Shunt zenner voltage | Vz | 25.5 | 27.5 | 29.5 | V | Icc = 14mA |
| | Vz temperature stability | dVz/dTa | – | –4 | – | mV/°C | Icc = 14mA *1 |
| | Latch current | ILATCH | 180 | 250 | 320 | μA | Vcc = 9V |
| VREF | Output voltage | Vref | 4.9 | 5.0 | 5.1 | V | Isource = 1mA |
| | Line regulation | Vref-line | – | 5 | 20 | mV | Isource = 1mA, Vcc = 12V to 23V |
| | Load regulation | Vref-load | – | 5 | 20 | mV | Isource = 1mA to 20mA |
| | Temperature stability | dVref | – | 80 | – | ppm/°C | Ta = –40 to 125°C *1 |
| Oscillator | Initial accuracy | fpwm | 117 | 130 | 143 | kHz | Measured pin: PWM-OUT |
| | | fpfc | 58.5 | 65 | 71.5 | kHz | Measured pin: PFC-OUT |
| | fpwm temperature stability | dfpwm/dTa | – | ±0.1 | – | %/°C | Ta = –40 to 125°C *1 |
| | fpwm voltage stability | fpwm(line) | –1.5 | +0.5 | +1.5 | % | VCC = 12V to 18V |
| | Ramp peak voltage | Vramp-H | – | 3.6 | 4.0 | V | PFC *1 |
| | Ramp valley voltage | Vramp-L | – | 0.65 | – | V | PFC *1 |
| | CT peak voltage | Vct-H | – | 3.2 | – | V | PWM *1 |
| | CT valley voltage | Vct-L | 1.50 | 1.60 | – | V | PWM *1 |
| | RT voltage | Vrt | 0.85 | 1.00 | 1.15 | V | Measured pin: RT |
| Supervisor | PFC on voltage | Von-pfc | 1.4 | 1.5 | 1.6 | V | |
| | PFC off voltage | Voff-pfc | 1.1 | 1.2 | 1.3 | V | |
| | PFC on-off hysteresis | dVon-off | 0.2 | 0.3 | 0.4 | V | |
| | Input current | Ipfc-on | – | 0.1 | 1.0 | μA | PFC-ON = 2V |
| | PFC OVP set voltage | Vovps-pfc | 2.65 | 2.80 | 2.95 | V | Input pin: PFC-FB |
| | PFC OVP reset voltage | Vovpr-pfc | 2.45 | 2.60 | 2.75 | V | Input pin: PFC-FB |
| | PFC OVP hysteresis | dVovp | 0.10 | 0.20 | 0.30 | V | |
| | B+ good voltage | Vb-good | 2.25 | 2.40 | 2.55 | V | Measured pin: PFC-FB |
| | B+ fail voltage | Vb-fail | 1.4 | 1.5 | 1.6 | V | Measured pin: PFC-FB |
| OVP latch | Latch threshold voltage | Vlatch | 3.76 | 4.00 | 4.24 | V | Input pin: PWM-SS |
| | Latch reset voltage | Vcc-res | 6.1 | 7.1 | 8.1 | V | |
| Power saving for PWM | Power saving on voltage | Von-save | 1.53 | 1.70 | 1.87 | V | Measured pin: PWM-COMP |
| | Minimum frequency at light load | fpwm-min | – | 2 | – | kHz | PWM-COMP = 1.5V Measured pin: PWM-OUT *1 |

Note: 1. Reference values for design.

## Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Soft start for PWM | Soft start time | tss-pwm | – | 4.2 | – | ms | PWM-SS = 0V to Vct-h *1 |
| | Source current | Iss-pwm | –20.0 | –25.0 | –30.0 | μA | Measured pin: PWM-SS |
| | High voltage | Vh-ss | 3.25 | 3.5 | 3.75 | V | Measured pin: PWM-SS |
| Soft start for PFC | Soft start time | tss-pfc | – | 5.7 | – | ms | PFC-SS = Vref to Vramp-I *1 |
| | Source current | Iss-pfc | +20.0 | +25.0 | +30.0 | μA | Measured pin: PFC-SS |
| PWM current sense | Delay to output | td-cs | – | 210 | 300 | ns | PWM-EO = 5V, PWM-CS = 0 to 2V |
| PFC current limit | Threshold voltage | VLM1 | –0.45 | –0.50 | –0.55 | V | PFC-ON = 2V |
| | Threshold voltage | VLM2 | –0.22 | –0.25 | –0.28 | V | PFC-ON = 4V |
| | Delay to output | td-LM | – | 280 | 500 | ns | PFC-CS = 0 to –1V |
| PFC-$V_{AMP}$ | Feedback voltage | Vfb-pfc | 2.45 | 2.50 | 2.55 | V | PFC-EO = 2.5V |
| | Input bias current | Ifb-pfc | –0.3 | 0 | 0.3 | μA | Measured pin: PFC-FB |
| | Open loop gain | Av-pfc | – | 65 | – | dB | *1 |
| | High voltage | Veoh-pfc | 5.0 | 5.7 | 6.4 | V | PFC-FB = 2.3V, PFC-EO: Open |
| | Low voltage | Veol-pfc | – | 0.1 | 0.3 | V | PFC-FB = 2.7V, PFC-EO: Open |
| | Source current | Isrc-pfc | – | –90 | – | μA | PFC-FB = 1.0V, PFC-EO: 2.5V *1 |
| | Sink current | Isnk-pfc | – | 90 | – | μA | PFC-FB = 4.0V, PFC-EO: 2.5V *1 |
| | Transconductance | Gm-pfcv | 150 | 200 | 250 | μA/V | PFC-FB = 2.5V, PFC-EO: 2.5V |
| PFC-OUT | Minimum duty cycle | Dmin-pfc | – | – | 0 | % | CAO = 4.0V |
| | Maximum duty cycle | Dmax-pfc | 90 | 95 | 98 | % | CAO = 0V |
| | Rise time | tr-pfc | – | 30 | 100 | ns | CL = 1000pF |
| | Fall time | tf-pfc | – | 30 | 100 | ns | CL = 1000pF |
| | Peak current | Ipk-pfc | – | 1.0 | – | A | CL = 0.01μF *1 |
| | Low voltage | Vol1-pfc | – | 0.05 | 0.2 | V | Iout = 20mA |
| | | Vol2-pfc | – | 0.5 | 2.0 | V | Iout = 200mA |
| | | Vol3-pfc | – | 0.03 | 0.7 | V | Iout = 10mA, VCC = 5V |
| | High voltage | Voh1-pfc | 11.5 | 11.9 | – | V | Iout = –20mA |
| | | Voh2-pfc | 10.0 | 11.0 | – | V | Iout = –200mA |
| PWM-OUT | Minimum duty cycle | Dmin-pwm | – | – | 0 | % | PWM-COMP = 0V |
| | Maximum duty cycle | Dmax-pwm | 42 | 45 | 49 | % | PWM-COMP = Vref |
| | Rise time | tr-pwm | – | 30 | 100 | ns | CL = 1000pF |
| | Fall time | tf-pwm | – | 30 | 100 | ns | CL = 1000pF |
| | Peak current | Ipk-pwm | – | 1.0 | – | A | CL = 0.01μF *1 |
| | Low voltage | Vol1-pwm | – | 0.05 | 0.2 | V | Iout = 20mA |
| | | Vol2-pwm | – | 0.5 | 2.0 | V | Iout = 200mA |
| | | Vol3-pwm | – | 0.03 | 0.7 | V | Iout = 10mA, VCC = 5V |
| | High voltage | Voh1-pwm | 11.5 | 11.9 | – | V | Iout = –20mA |
| | | Voh2-pwm | 10.0 | 11.0 | – | V | Iout = –200mA |

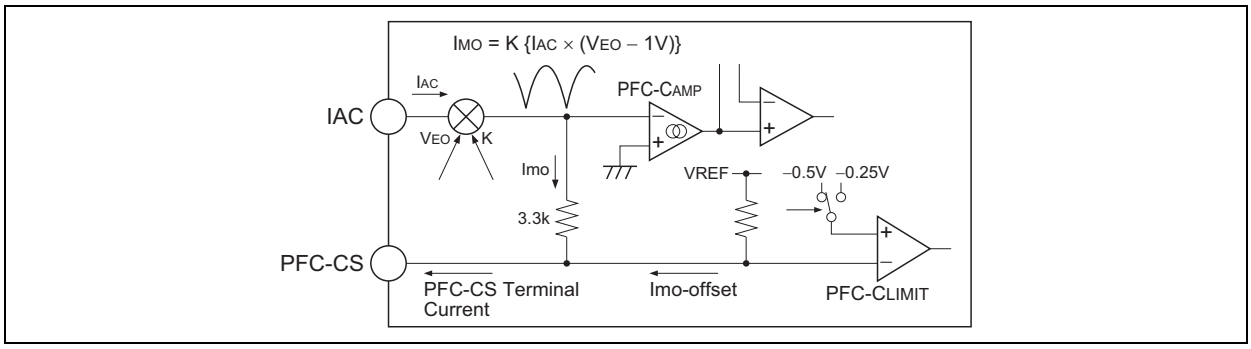
Note: 1. Reference values for design.

## Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

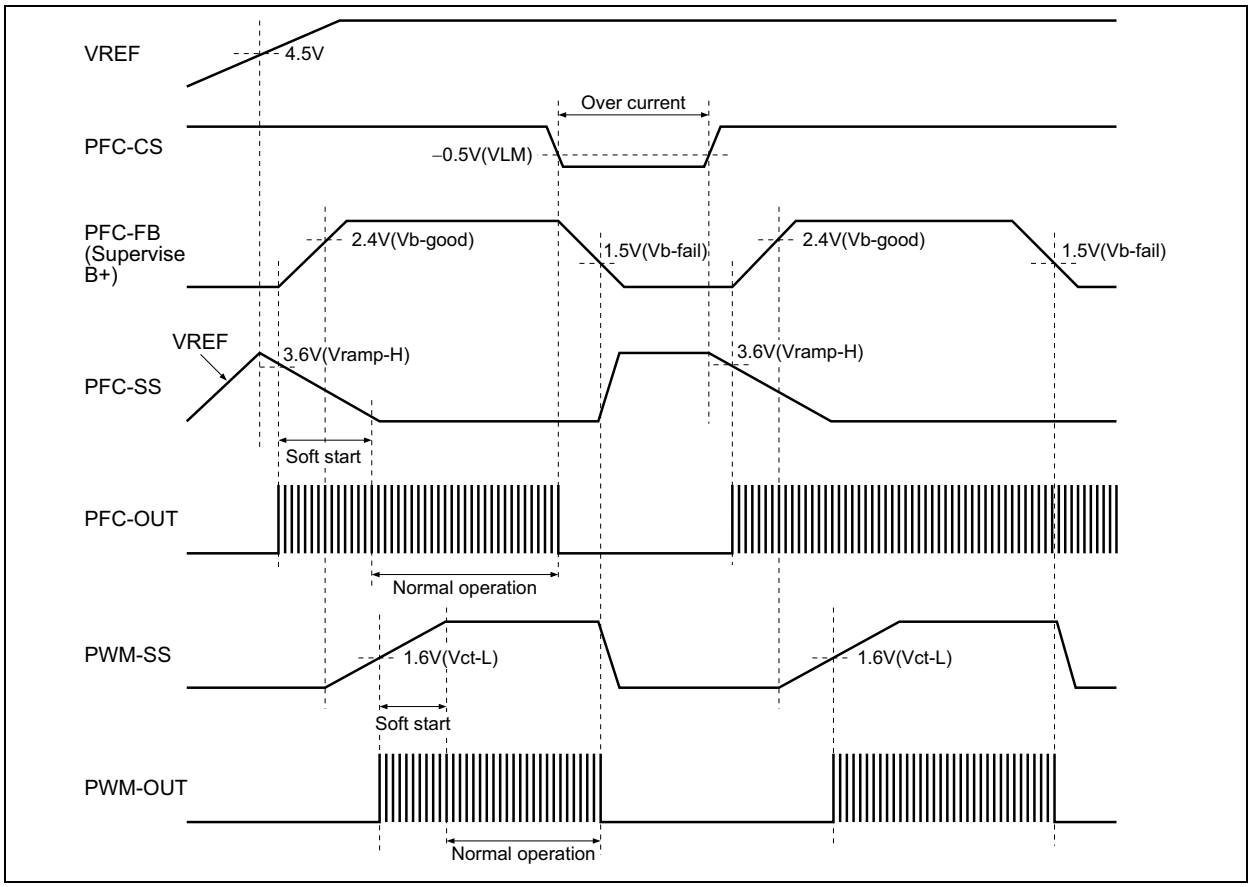
| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| PFC-CAMP | Input offset voltage | Vio-ca | – | ±7 | – | mV | *1 |
| | Open loop gain | Av-ca | – | 65 | – | dB | *1 |
| | High voltage | Veoh-ca | 5.0 | 5.7 | 6.4 | V | |
| | Low voltage | Veol-ca | – | 0.1 | 0.3 | V | |
| | Source current | Isrc-ca | – | –90 | – | μA | CAO = 2.5V *1 |
| | Sink current | Isnk-ca | – | 90 | – | μA | CAO = 2.5V *1 |
| | Transconductance | Gm-pfcc | 150 | 200 | 250 | μA/V | *1 |
| IAC/Multiplier | IAC pin voltage | Viac | 0.7 | 1.0 | 1.3 | V | IAC = 100μA |
| | Terminal offset current | Imo-offset1 | –67 | –90 | –113 | μA | IAC = 0A, PFC-ON = 2V |
| | | Imo-offset2 | –60 | –80 | –100 | μA | IAC = 0A, PFC-ON = 4V |
| | Output current (PFC-ON = 2.0V) | Imo1 | – | –20 | – | μA | PFC-EO = 2V, IAC = 100μA *1, 2 |
| | | Imo2 | – | –60 | – | μA | PFC-EO = 4V, IAC = 100μA *1, 2 |
| | Output current (PFC-ON = 4.0V) | Imo3 | – | –5 | – | μA | PFC-EO = 2V, IAC = 100μA *1, 2 |
| | | Imo4 | – | –15 | – | μA | PFC-EO = 4V, IAC = 100μA *1, 2 |
| | PFC-CS resistance | Rmo | – | 3.3 | – | kΩ | *1 |
| Gain selector | Threshold voltage for K = 0.05 | VK-H | 3.60 | 3.80 | 4.00 | V | Measured pin: PFC-ON |
| | Threshold voltage for K = 0.25 | VK-L | 3.20 | 3.40 | 3.60 | V | Measured pin: PFC-ON |
| | VK hysteresis | dVK | 0.30 | 0.40 | 0.50 | V | *1 |

Notes: 1. Reference values for design.
2. Imo1 to Imo4 are defined as:
Imo = (PFC-CS pin current) – (Imo-offset)

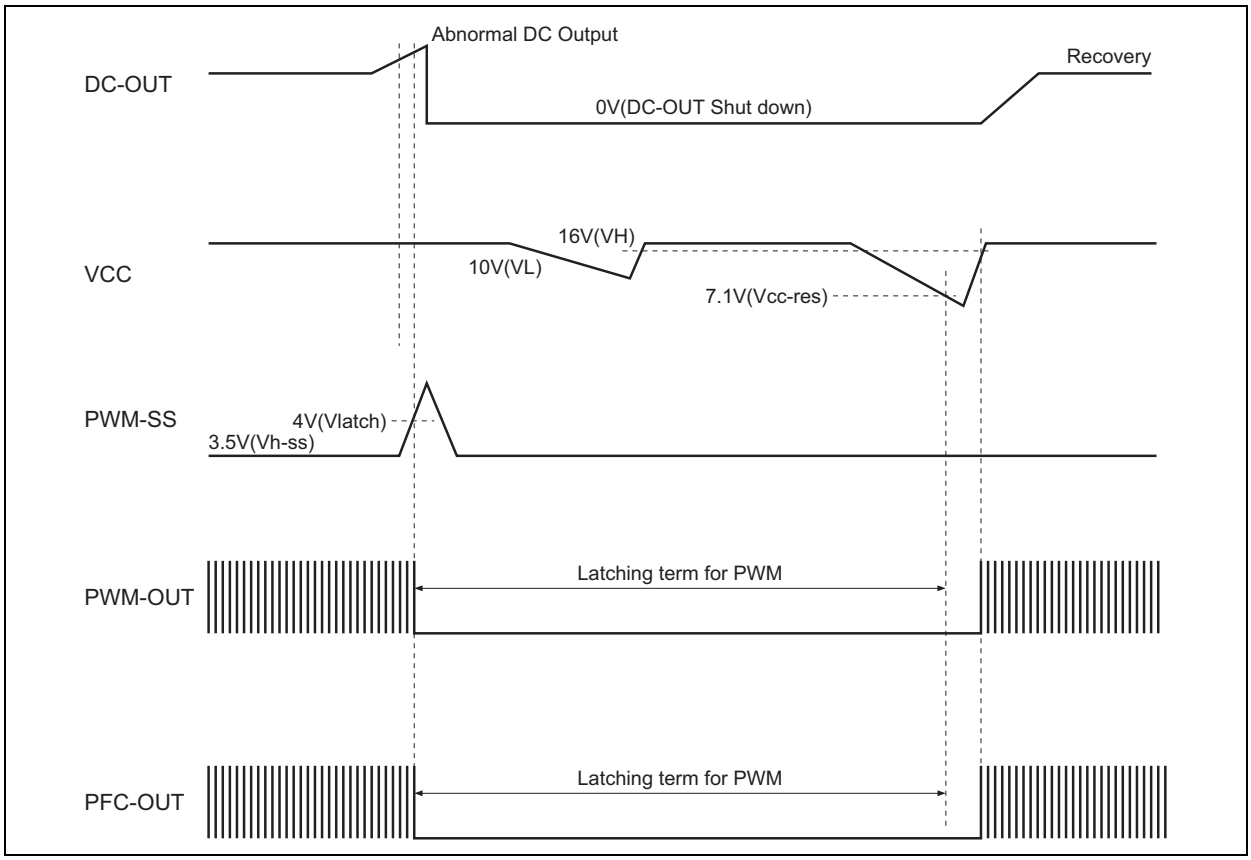


## Timing Diagram

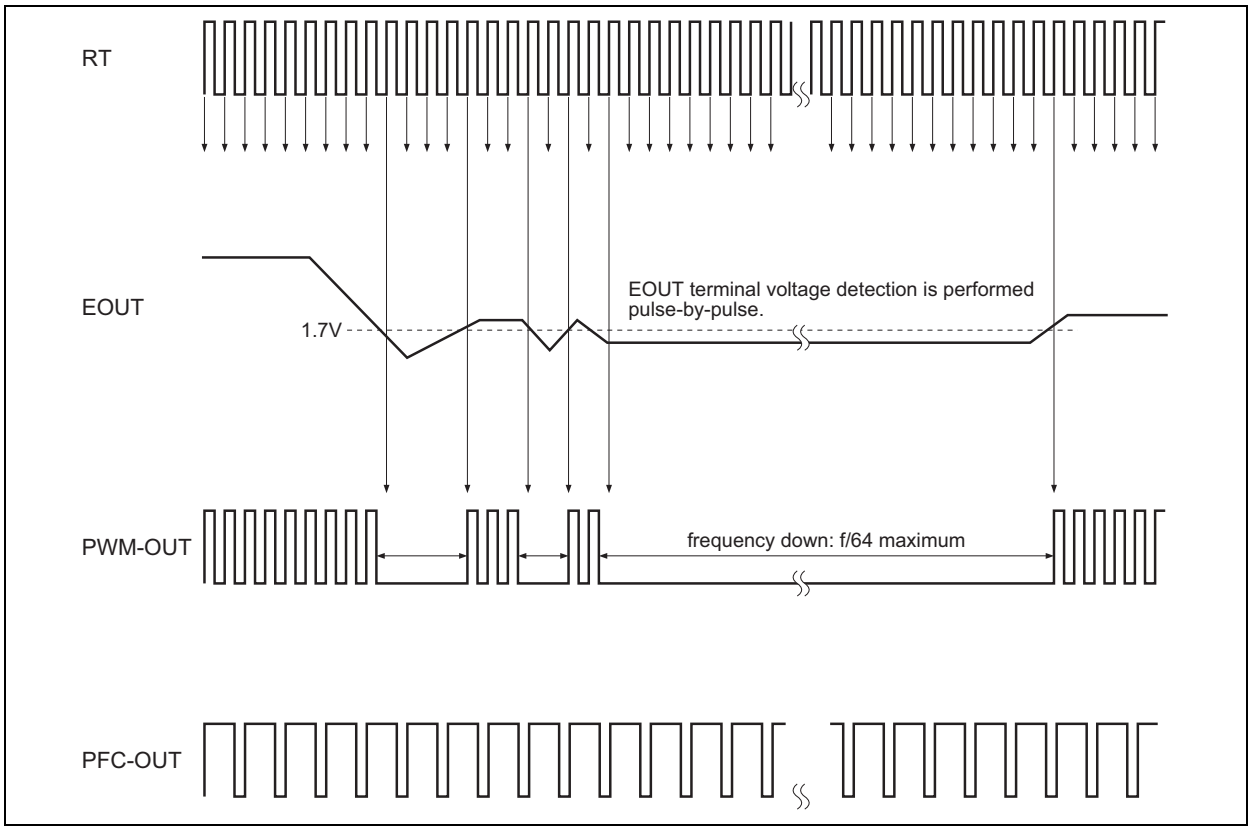
### 1. Start-up Timing



## 2. PWM OVP Latch



### 3. PWM Power Saving



## Functional Description

### 1. UVL Circuit

The UVL circuit monitors the Vcc voltage and halts operation of the IC in the event of a low voltage.

The voltage for detecting Vcc has a hysteresis characteristic, with 16.0 V as the start threshold and 10.0 V as the shutdown threshold.

When the IC has been halted by the UVL circuit, control is performed to fix driver circuit output low and halt VREF output and the oscillator.

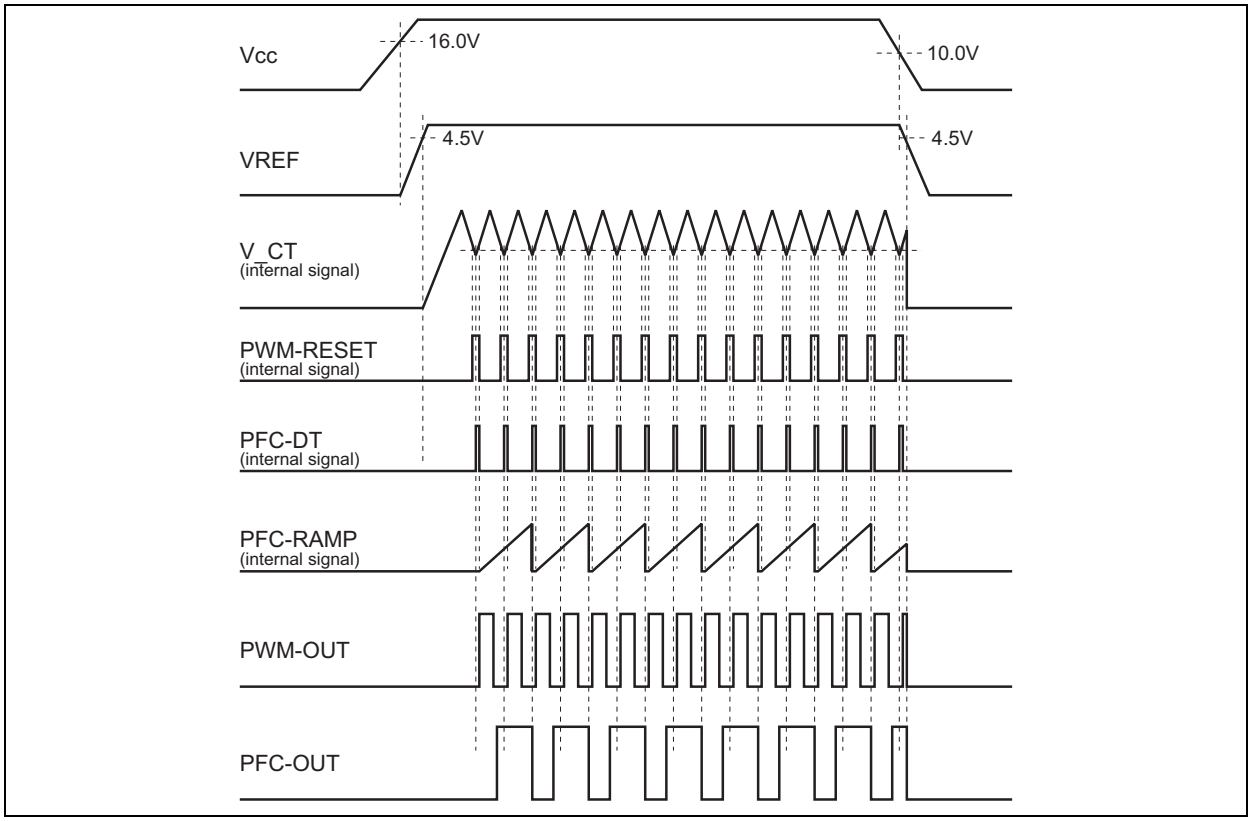



**Figure 1**

### 2. Soft Start Circuit (for PWM Control)

This function gradually increases the pulse width of the PWM-OUT pin from a 0% duty cycle at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the secondary-side output voltage.

The soft start time can easily be set with a single external capacitance.

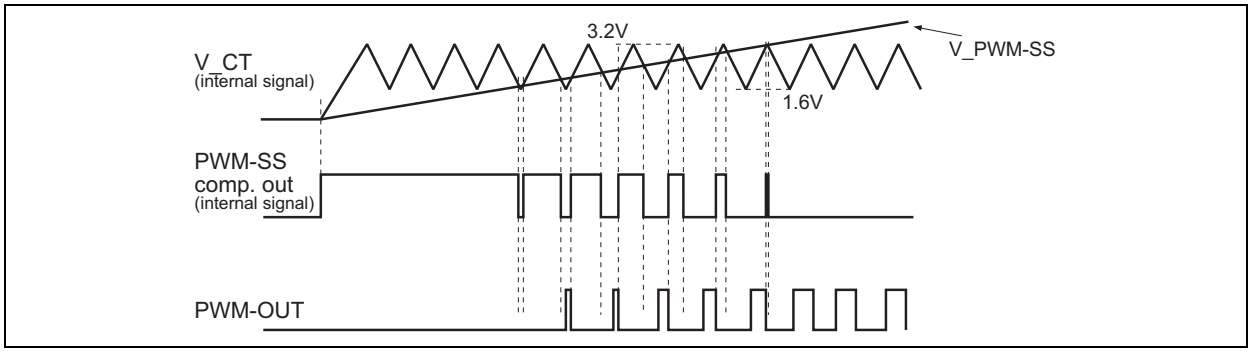



**Figure 2**

Soft start time tss-pwm is determined by PWM-SS pin connection capacitance Css-pwm and an internal constant, and can be estimated using the equation shown below.

Soft start time tss-pwm is the time until the PWM-SS pin voltage reaches upper-end voltage 3.2 V of the IC-internal CT voltage waveform after VREF starts up following UVLO release.

Soft start time tss-pwm when Css-pwm is 3.3 nF is given by the following equation.

$$\text{tss-pwm} = \frac{\text{Css-pwm} \times \text{Vct-H}}{\text{Iss-pwm}} = \frac{33\ [\text{nF}] \times 3.2\ [\text{V}]}{25\ [\mu\text{A}]} \approx 4.2\ [\text{ms}]$$

* Iss-pwm: PWM-SS pin source current, 25 μA typ.

### 3. Soft Start Circuit (for PFC Control)

This function gradually increases the pulse width of the PFC-OUT pin from a 0% duty cycle at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the PFC output voltage (B+ voltage).

The soft start time can easily be set with a single external capacitance.

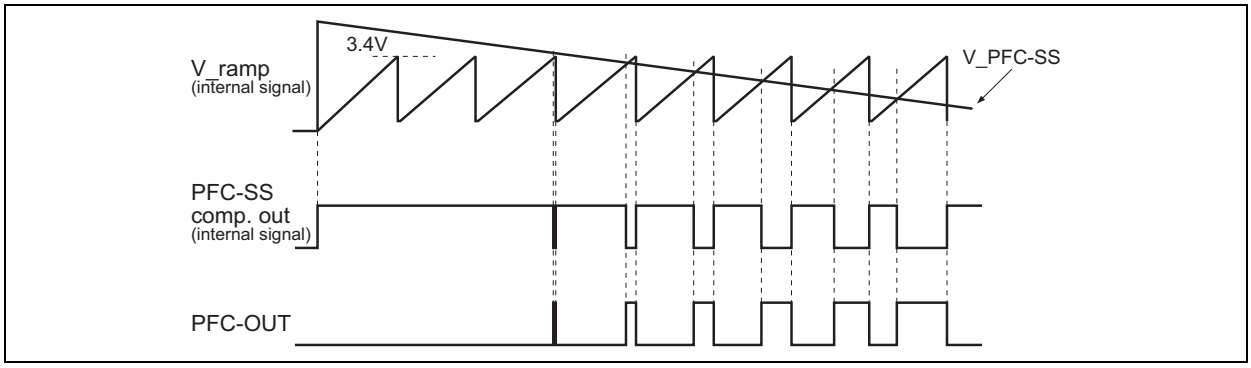



**Figure 3**

Soft start time tss-pfc is determined by PFC-SS pin connection capacitance Css-pfc and an internal constant, and can be estimated using the equation shown below.

Soft start time tss-pfc is the time until the PFC-SS pin voltage reaches lower-end voltage 0.65 V of the IC-internal RAMP voltage waveform after VREF starts up following UVLO release.

Soft start time tss-pfc when Css-pfc is 3.3 nF is given by the following equation.

$$tss\text{-}pfc = \frac{Css\text{-}pfc \times (VREF - Vramp\text{-}L)}{Iss\text{-}pwm} = \frac{33\ [nF] \times (5 - 0.65)}{25\ [\mu A]}$$

$$\approx 5.7\ [ms]$$

* Iss-pfc: PFC-SS pin sink current, 25 μA typ.

In addition, when you do not use a soft start function, please ground this terminal.

### 4. PFC On/Off Function

On/off control of the PFC function can be performed using the PFC-ON pin.

If an AC voltage that has undergone primary rectification and has been divided by an external resistance is input, it is possible to halt PFC operation in the event of a low input voltage. On/off control is also possible by using a logic signal.

When the PFC function is turned on/off by using the PFC-ON pin, however, the PFC-SS pin cannot be reset. Therefore, a soft start is not operated at the start-up by the PFC-ON pin.

The figure below illustrates an example of circuit for simultaneous reset of the PFC-SS pin and PWM-SS pin.

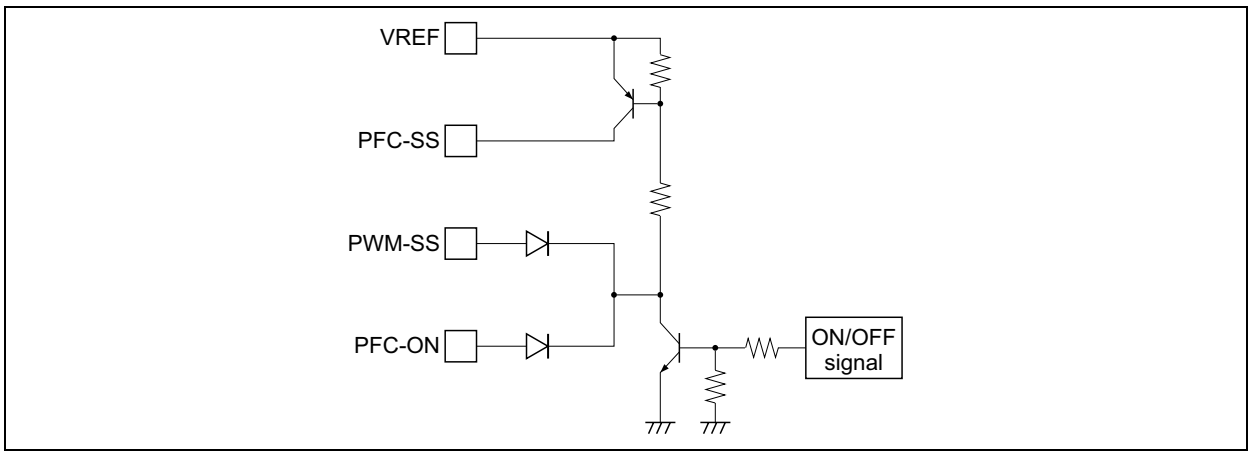



**Figure 4 Example of Circuit Configuration to Turn On/Off PFC & PWM Functions**

This IC also incorporates a function that automatically detects a 100 V system or 200 V system AC voltage at the PFC-ON pin, and switches multiplier gain and the PFC-CS comparison voltage.

These functions simplify the design of a power supply compatible with worldwide input.

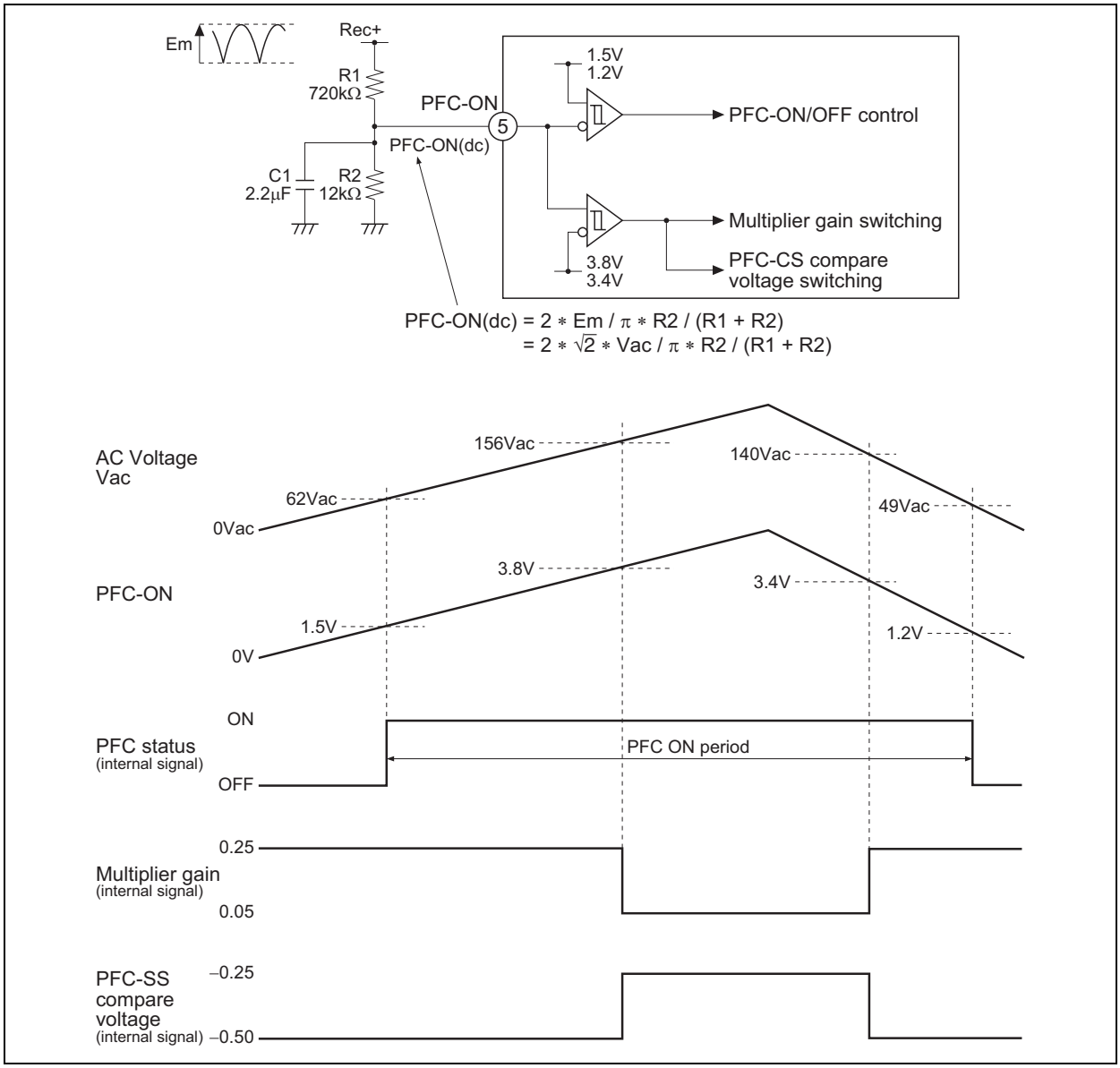



**Figure 5**

### 5. Power Saving in Standby State (for PWM Control)

When the output load is light, as in the standby state, the operating frequency of the PWM control section is automatically decreased in order to reduce switching loss.

Standby detection is performed by monitoring the PWM-COMP voltage, and the operating frequency is decreased to a maximum of 1/64 of the reference frequency determined by an external timing resistance.

As standby detection is performed on a reference frequency pulse-by-pulse basis, the frequency varies gently according to the output load.

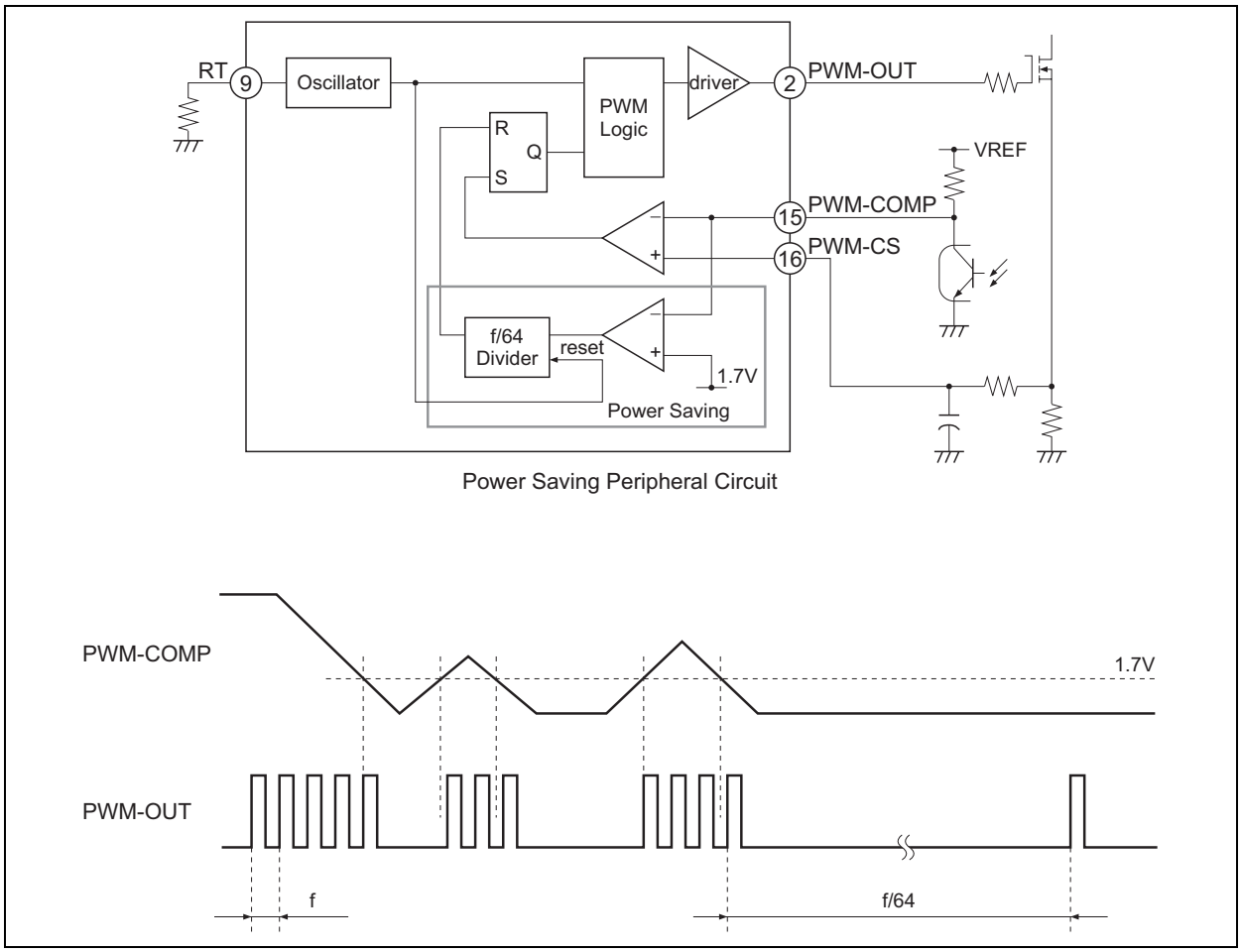


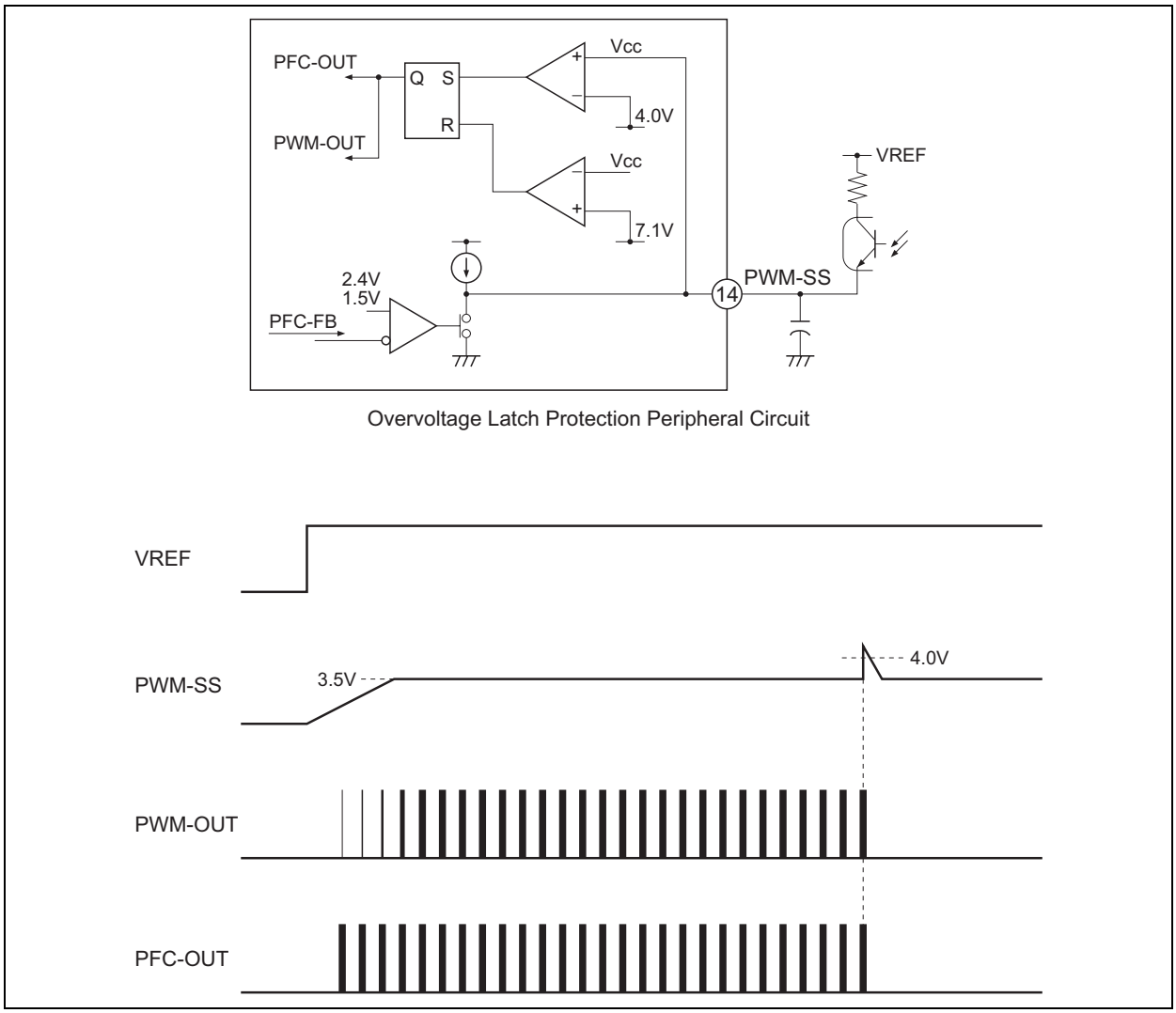

**Figure 6**

### 6. Overvoltage Latch Protection (for PWM Control)

This is a protection function that halts PWM-OUT and PFC-OUT if the secondary-side PWM output voltage is abnormally high.

Overvoltage signal input is shared with the PWM-SS pin. When this pin is pulled up to 4.0 V or higher, the control circuit identifies an overvoltage error and halts PWM-OUT and PFC-OUT.

The power supply is turned off, and the latch is released when the VCC voltage falls to 7.1 V or below.




Overvoltage Latch Protection Peripheral Circuit

**Figure 7**

## 7. Operating Frequency

The operating frequency is adjusted by timing resinstance RT.

Adjustment examples are shown in the graph below. The operating frequency fpwm in the PWM section is determined by the RT. The operating frequency fpfc in the PFC section is half the value of fpwm.

The operating frequency in the PWM section can be estimated using the approximate equation shown below.
RT = 200 kΩ:

$$fpwm \approx \frac{2.60 \times 10^{10}}{RT} = 130 \text{ [kHz]}$$

$$fpfc = \frac{fpwm}{2} = 65 \text{ [kHz]}$$

This is only an approximate equation, and the higher the frequency, the greater will be the degree of error of the approximate equation due to the effects of the delay time in the internal circuit, etc.

When the operating frequency is adjusted, it is essential to confirm operation using the actual system.

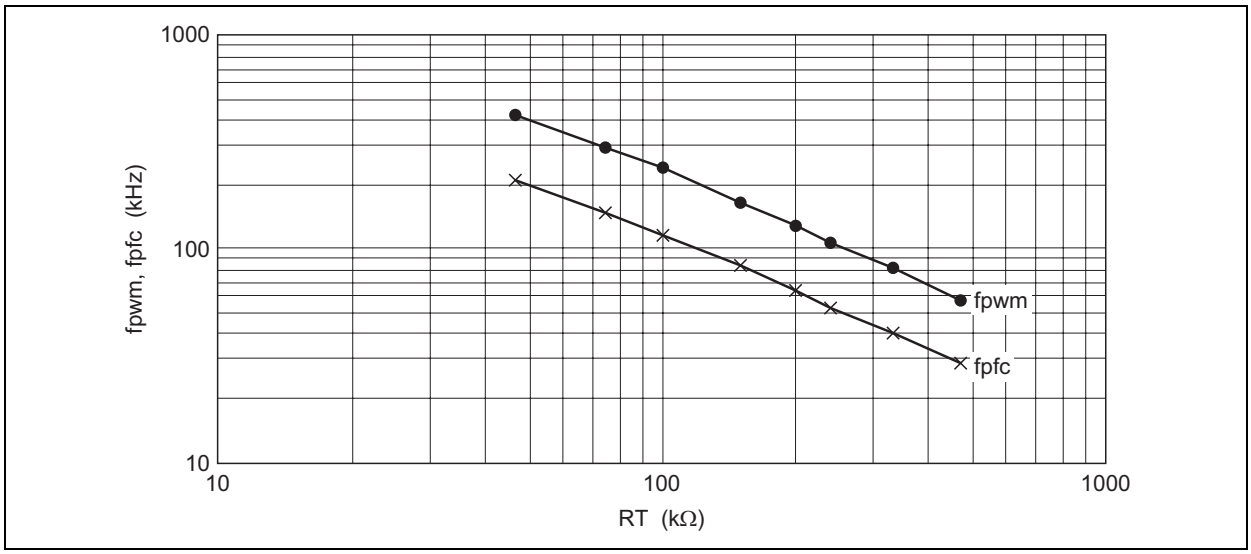
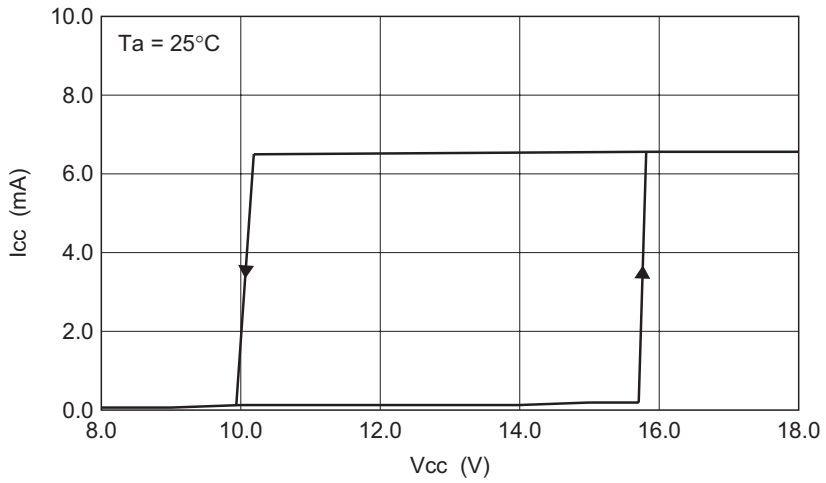


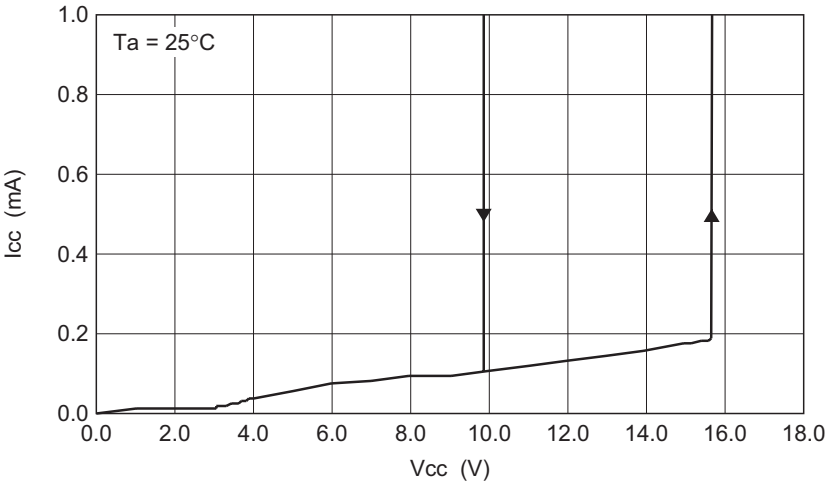

**Figure 8**

## Characteristic Curves

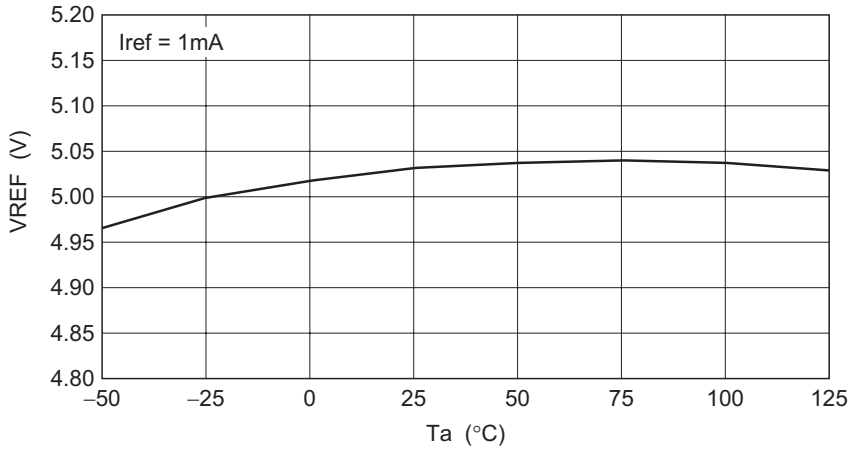
Power Supply Current vs. Power Supply Voltage Characteristics



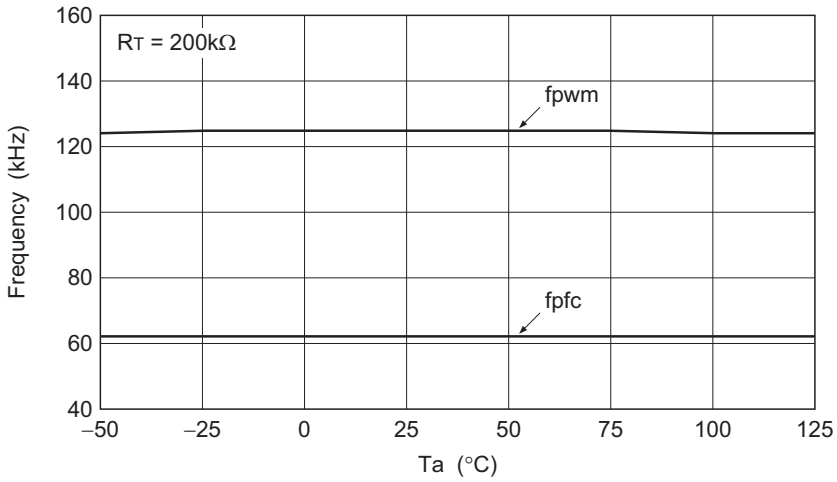

Standby Current vs. Power Supply Voltage Characteristics



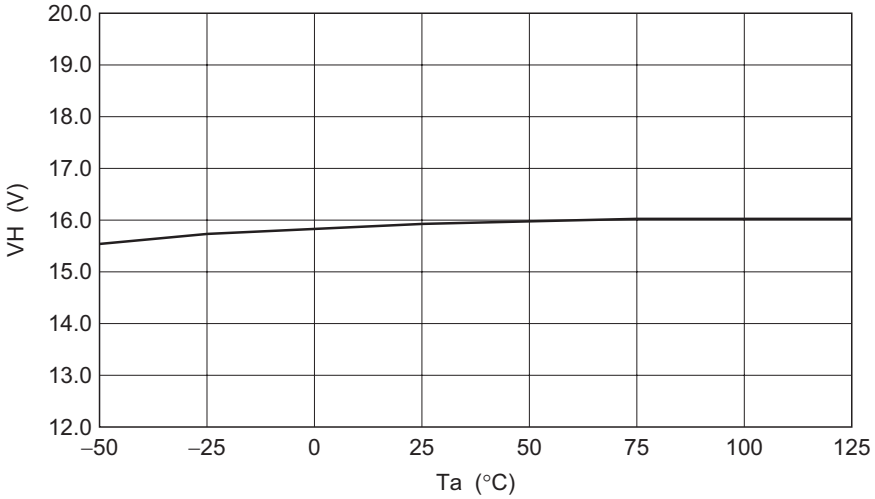
VREF Output Voltage vs. Ambient Temperature Characteristics



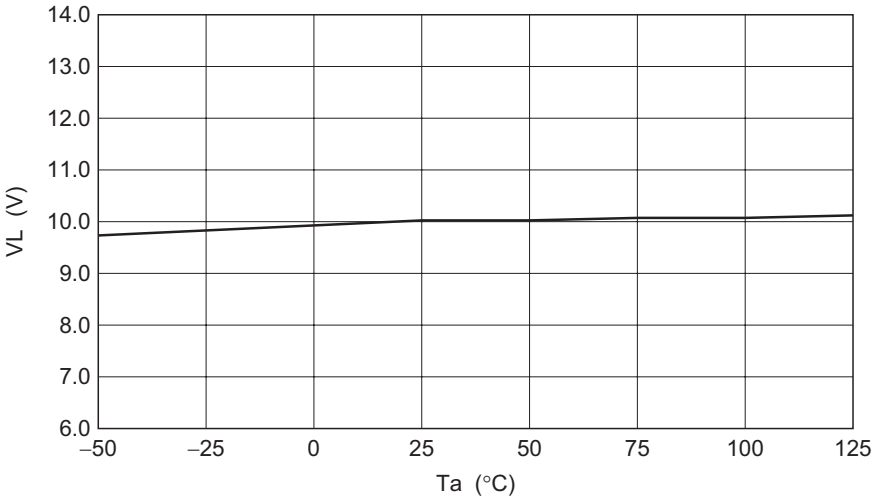

Operating Frequency vs. Ambient Temperature Characteristics



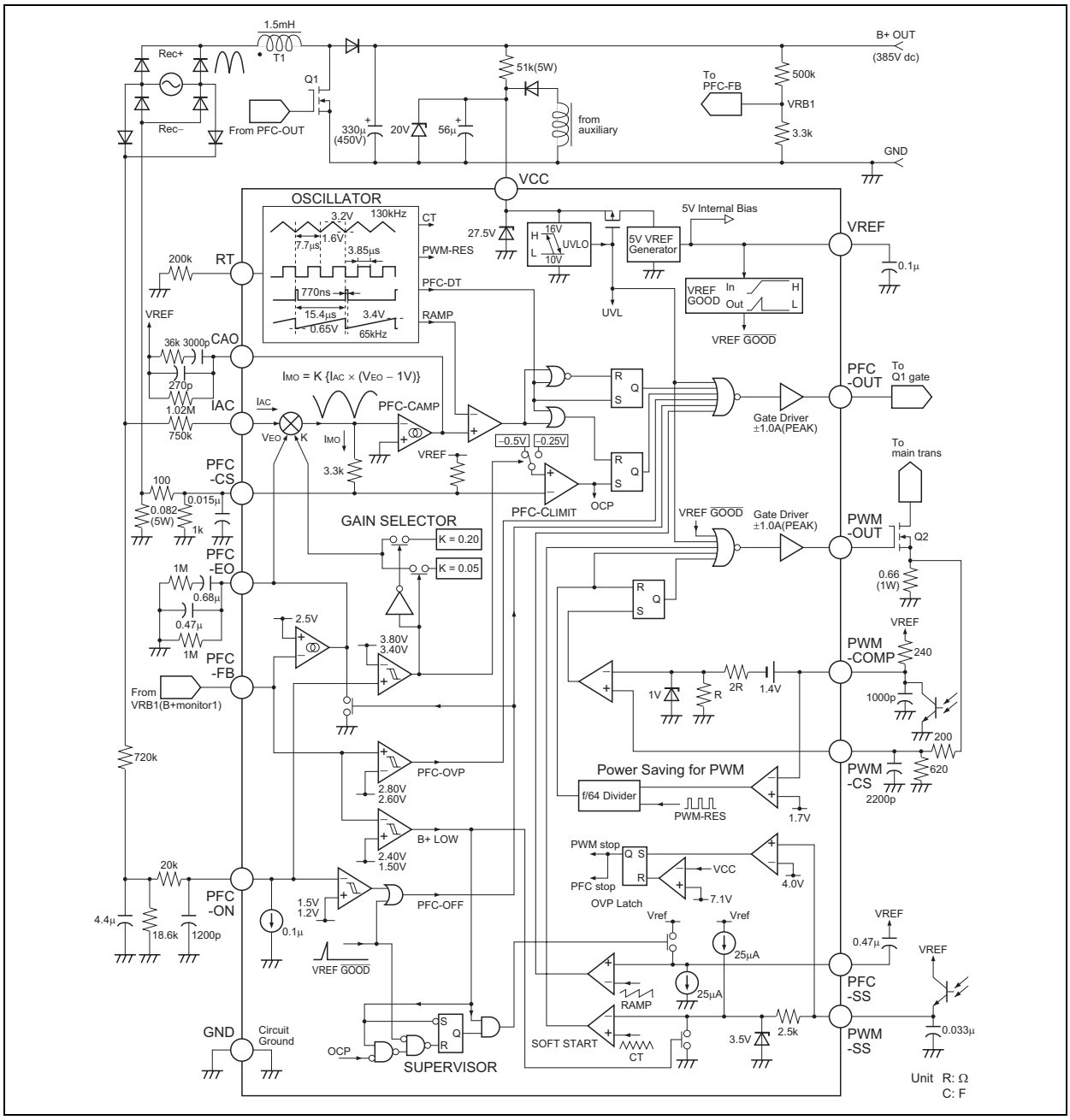
UVL Start-up Voltage vs. Ambient Temperature Characteristics




UVL Shutdown Voltage vs. Ambient Temperature Characteristics

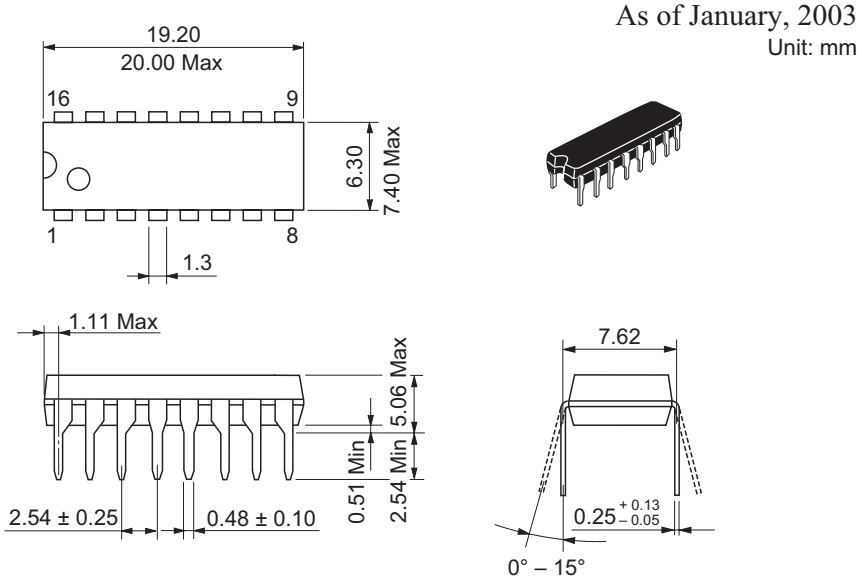


## Application Circuit Example



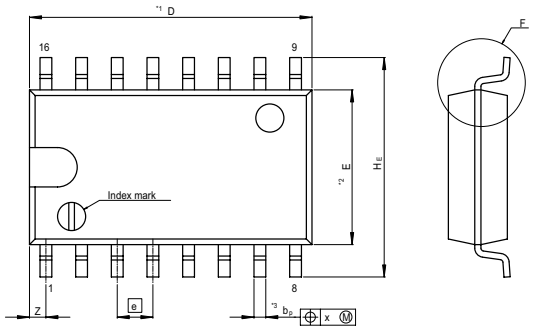
## Package Dimensions

As of January, 2003
Unit: mm



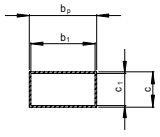

| | |
|---|---|
| Package Code | DP-16 |
| JEDEC | Conforms |
| JEITA | Conforms |
| Mass (reference value) | 1.07 g |

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-A | FP-16DA | 0.24g |

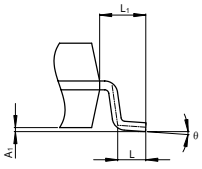









Terminal cross section




Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.5 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.42 | 0.50 |
| $b_1$ | — | 0.40 | — |
| c | 0.17 | 0.22 | 0.27 |
| $c_1$ | — | 0.20 | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

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Colophon .7.0