DATA SHEET

NEC

# MOS FIELD EFFECT TRANSISTOR

# μPA1770

## SWITCHING
## DUAL P-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

The μPA1770 is a P-channel MOS Field Effect Transistor designed for power management applications of portable machines.

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA1770G | Power SOP8 |

### FEATURES

- Dual chip type
- Low on-resistance
  $R_{DS(on)1}$ = 37 mΩ MAX. ($V_{GS}$ = –4.5 V, $I_D$ = –3.0 A)
  $R_{DS(on)2}$ = 39 mΩ MAX. ($V_{GS}$ = –4.0 V, $I_D$ = –3.0 A)
  $R_{DS(on)3}$ = 59 mΩ MAX. ($V_{GS}$ = –2.5 V, $I_D$ = –3.0 A)
- Low input capacitance
  $C_{iss}$ = 1300 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, All terminals are connected.)

| | | | | |
|---|---|---|---|---|
| | Drain to Source Voltage | $V_{DSS}$ | –20 | V |
| | Gate to Source Voltage | $V_{GSS}$ | ∓12 | V |
| | Drain Current (DC) | $I_{D(DC)}$ | ∓6.0 | A |
| | Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ∓24 | A |
| | Total Power Dissipation (1 unit) Note2 | $P_T$ | 0.40 | W |
| | Total Power Dissipation (2 unit) Note2 | $P_T$ | 0.75 | W |
| ★ | Total Power Dissipation (1 unit) Note3 | $P_T$ | 1.7 | W |
| ★ | Total Power Dissipation (2 unit) Note3 | $P_T$ | 2.0 | W |
| | Channel Temperature | $T_{ch}$ | 150 | °C |
| | Storage Temperature | $T_{stg}$ | –55 to +150 | °C |

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

**2.** Mounted on FR4 Board of 1600 $mm^2$ x 1.6 mm, Drain Pad size : 4.5 $mm^2$ x 35 μm, $T_A$ = 25°C

★ **3.** Mounted on ceramic substrate of 1200 $mm^2$ x 2.2 mm, $T_A$ = 25°C

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**Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

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**The mark ★ shows major revised points.**

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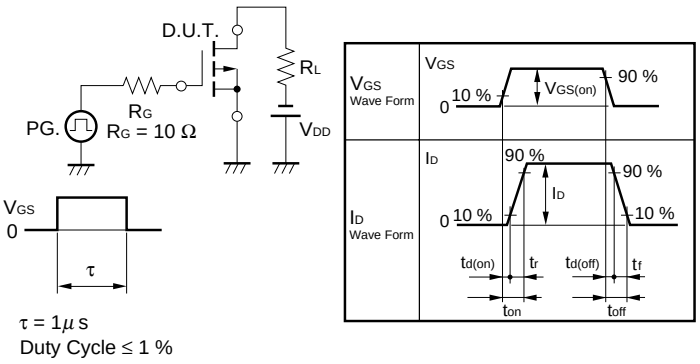
## ★ ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, All terminals are connected.)

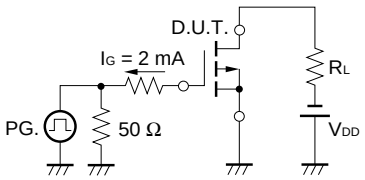
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = –4.5 V, $I_D$ = –3.0 A | | 28 | 37 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = –4.0 V, $I_D$ = –3.0 A | | 29.5 | 39 | mΩ |
| | $R_{DS(on)3}$ | $V_{GS}$ = –2.5 V, $I_D$ = –3.0 A | | 44 | 59 | mΩ |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = –10 V, $I_D$ = 1 mA | –0.5 | –1.0 | –1.5 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = –10 V, $I_D$ = –3.0 A | 5.0 | 11 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = –20 V, $V_{GS}$ = 0 V | | | –1 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ∓ 12 V, $V_{DS}$ = 0 V | | | ∓ 10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –10 V | | 1300 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 325 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 155 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = –3.0 A | | 25 | | ns |
| Rise Time | $t_r$ | $V_{GS(on)}$ = –4.5 V | | 110 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $V_{DD}$ = –10 V | | 130 | | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 140 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = –6.0 A | | 11 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{DD}$ = –16 V | | 2.0 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $V_{GS}$ = –4.5 V | | 4.0 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 6.0 A, $V_{GS}$ = 0 V | | 0.8 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 6.0 A, $V_{GS}$ = 0 V | | 60 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A / μs | | 40 | | nC |

### TEST CIRCUIT 1 SWITCHING TIME




τ = 1μs
Duty Cycle ≤ 1 %

### TEST CIRCUIT 2 GATE CHARGE



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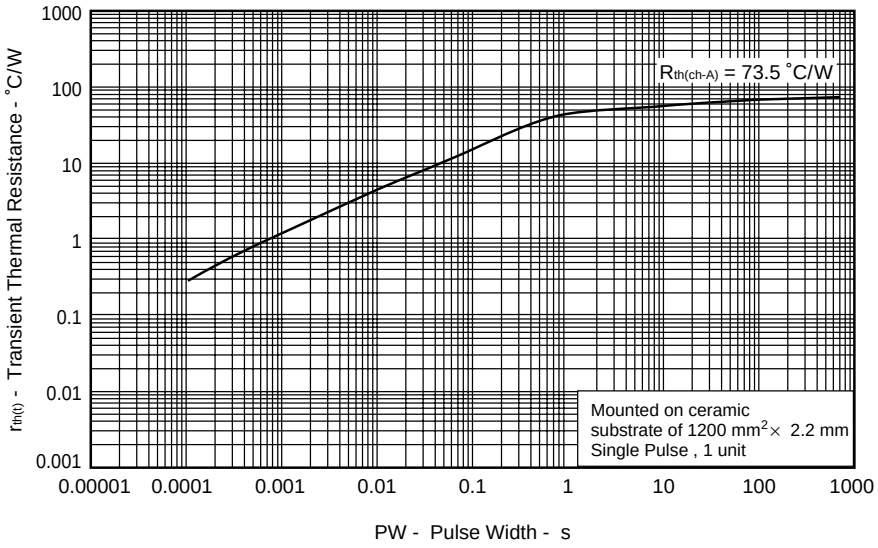
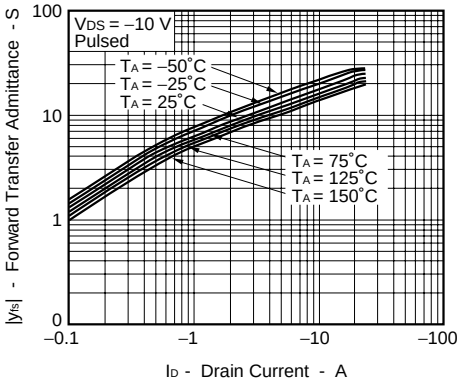
## ★ TYPICAL CHARACTERISTICS($T_A$ = 25 °C, All terminals are connected.)

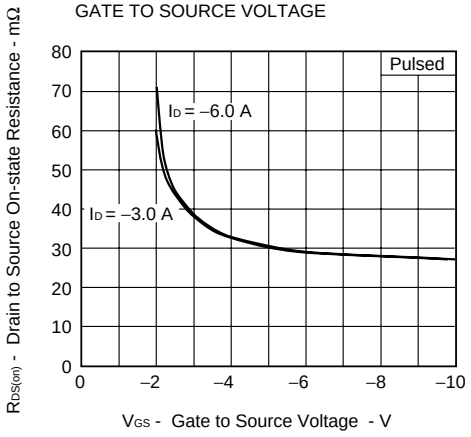
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



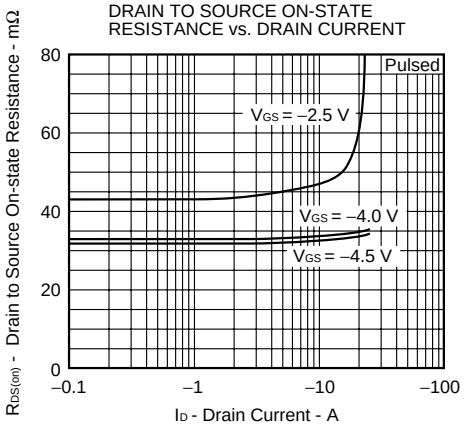

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



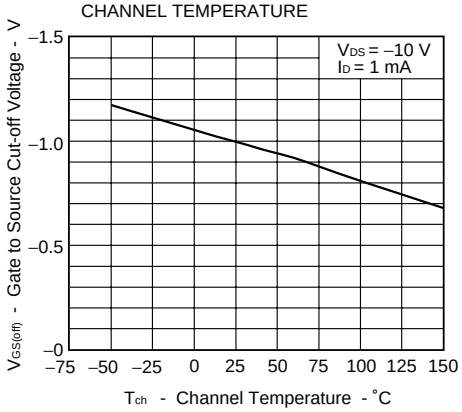

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE




DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT




GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



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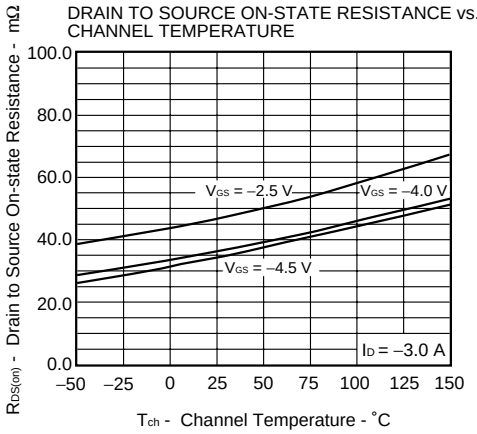
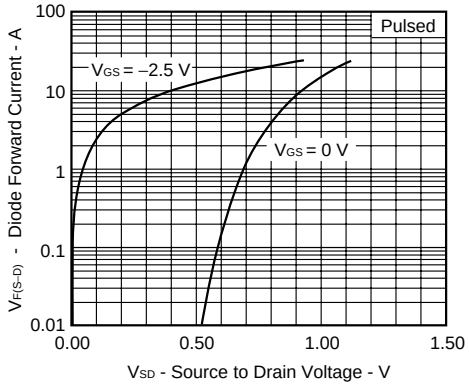
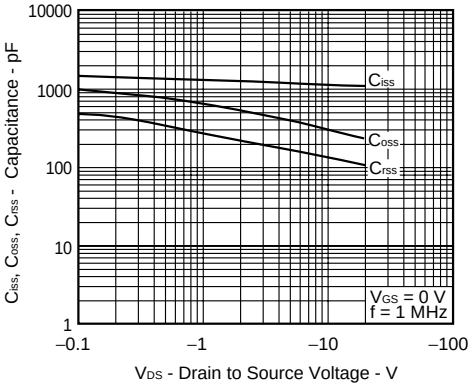
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



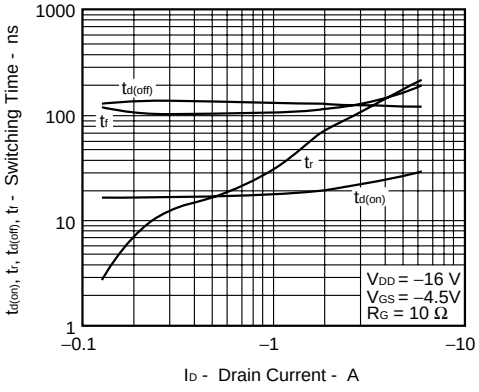

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



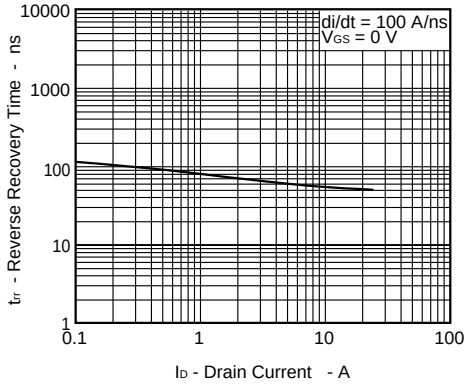

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



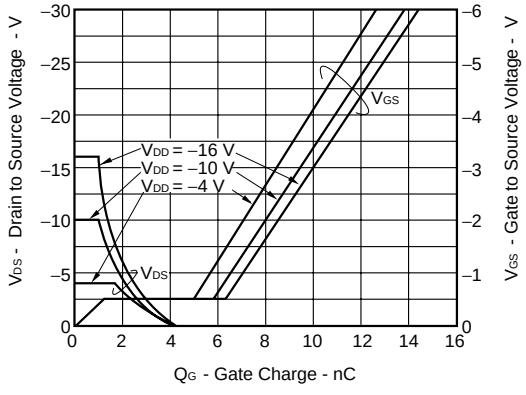

SWITCHING CHARACTERISTICS




REVERSE RECOVERY TIME vs. DRAIN CURRENT




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



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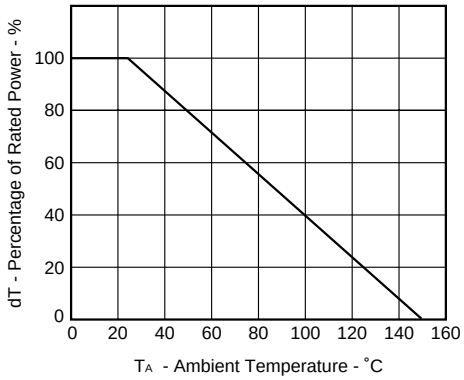
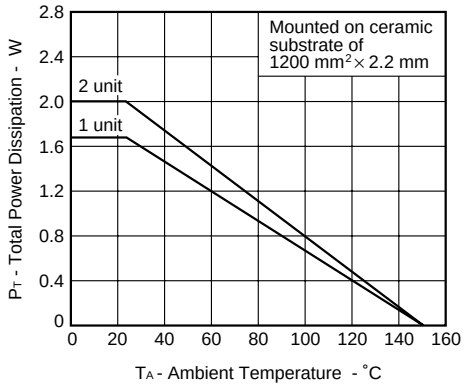
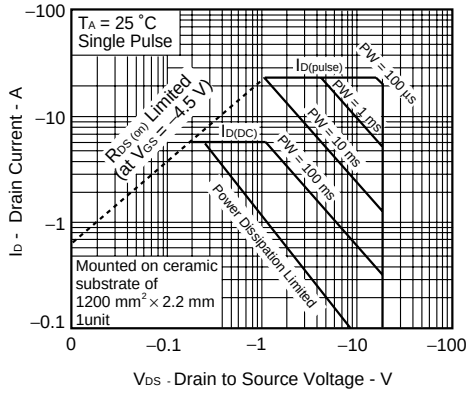
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



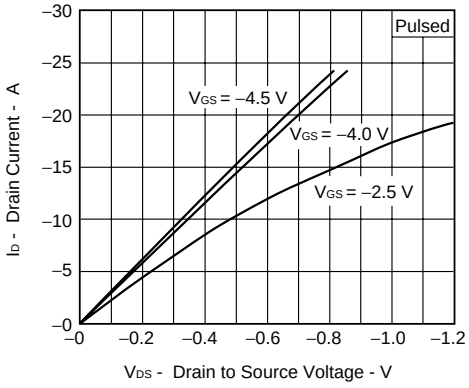

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



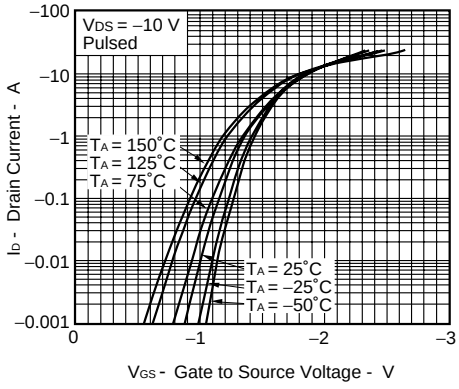

FORWARD BIAS SAFE OPERATING AREA




DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE




FORWARD TRANSFER CHARACTERISTICS



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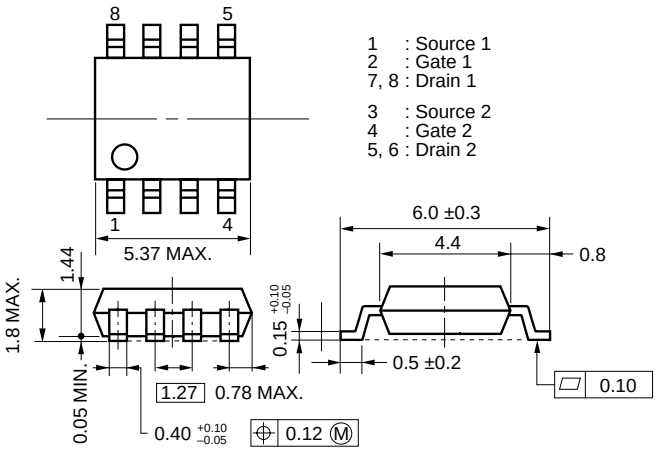
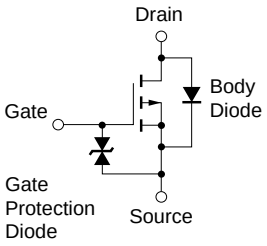
**PACKAGE DRAWING (Unit : mm)**

Power SOP8




**EQUIVALENT CIRCUIT**

(1/2 circuit)




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



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