M62398P,FP

8BIT 12CH I^{2}C BUS D–A CONVERTER WITH BUFFER AMPLIFIERS

GENERAL DESCRIPTION

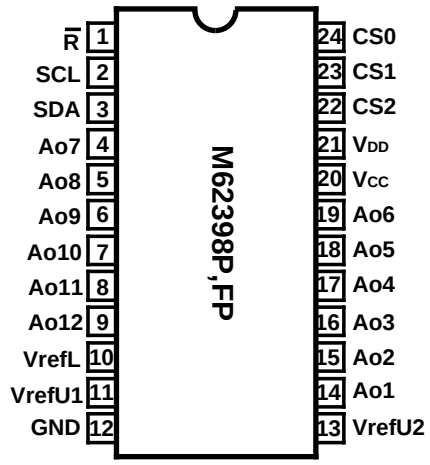
The M62398P,FP is a 12V type CMOS 12-channel D–A converters with output buffer amplifiers.

It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I2C BUS.

The output buffer amplifier employs AB class output with sinking and sourcing capability of more than 2.5mA ,and an output voltage range is nearly between ground and VrefU.

Maximum 8 ICs can be connected to a bus by using three chip-set pins , so that it is possible to handle up to 96 channels.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D (P)
24P2N-B (FP)

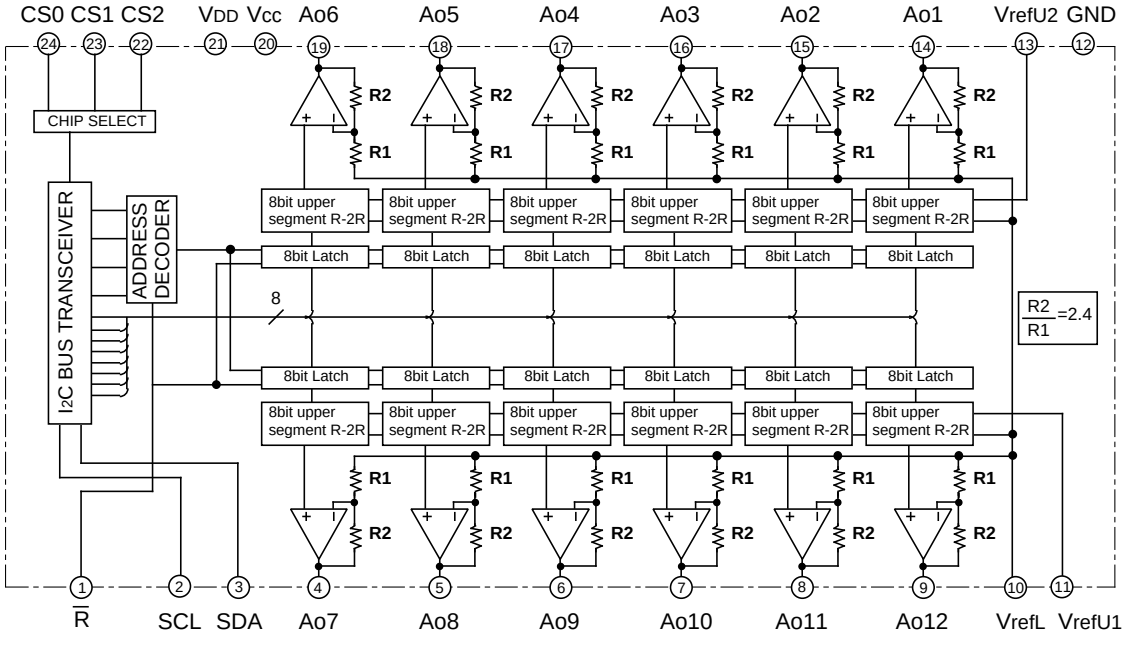
FEATURES

- I2C BUS serial data method
- Wide output range
  Nearly between ground and VrefU(0~12V).
- High output current drive capability
  Over ±2.5mA
- 2 setting voltage ranges by dual input pins for upper voltage references (VrefU1,U2)

APPLICATION

Conversion from digital control data to analog control data for both consumer and industrial equipment.
Gain control and automatic adjustment of DISPLAY-MONITOR or CTV.

BLOCK DIAGRAM



EXPLANATION OF TERMINALS

PIN No.	Symbol	Function
3	SDA	Serial data input terminal
1	$\overline{R}$	Reset signal input terminal
2	SCL	Serial clock input terminal
14	Ao1	8bit D–A converter output terminal
15	Ao2	
16	Ao3	
17	Ao4	
18	Ao5	
19	Ao6	
4	Ao7	
5	Ao8	
6	Ao9	
7	Ao10	
8	Ao11	
9	Ao12	
20	VCC	Analog power supply terminal
21	VDD	Digital power supply terminal
12	GND	Analog and digital common GND
10	VrefL	D–A converter low level reference voltage input terminal
11	VrefU1	D–A converter high level reference voltage input terminal 1
13	VrefU2	D–A converter high level reference voltage input terminal 2
22	CS2	Chip select data input terminal 2
23	CS1	Chip select data input terminal 1
24	CS0	Chip select data input terminal 0

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.3~13.5	V
V_{DD}	Supply voltage		–0.3~7.0	V
VrefU1,2	D–A converter upper reference voltage		V_{DD}	V
V_{IND}	Digital input voltage		–0.3~V_{DD}+0.3	V
Pd	Power dissipation		465(DIP) /421(FP)	mW
Topr	Operating temperature		–20~85	°C
Tstg	Storage temperature		–40~125	°C

ELECTRIC CHARACTERISTICS

< Digital part > (V_{CC}=13V,V_{DD}=Vref U1,2=+5V±10%,GND=VrefL=0V,Ta=–20~85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Ratings			Unit
			MIN	TYP	MAX	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	CLK=1MHz operation I_{AO}=0µA			1	mA
I_{ILK}	Input leak current	V_{IN}=0~V_{DD}	–10		10	µ A
V_{IL}	Input low voltage				0.2V_{DD}	V
V_{IH}	Input high voltage		0.8V_{DD}			V

< Analog part > (V_{CC}=13V,V_{DD}=VrefU1,2=+5V±10%,GND=VrefL=0V,Ta=–20~85°C,unless otherwise noted)

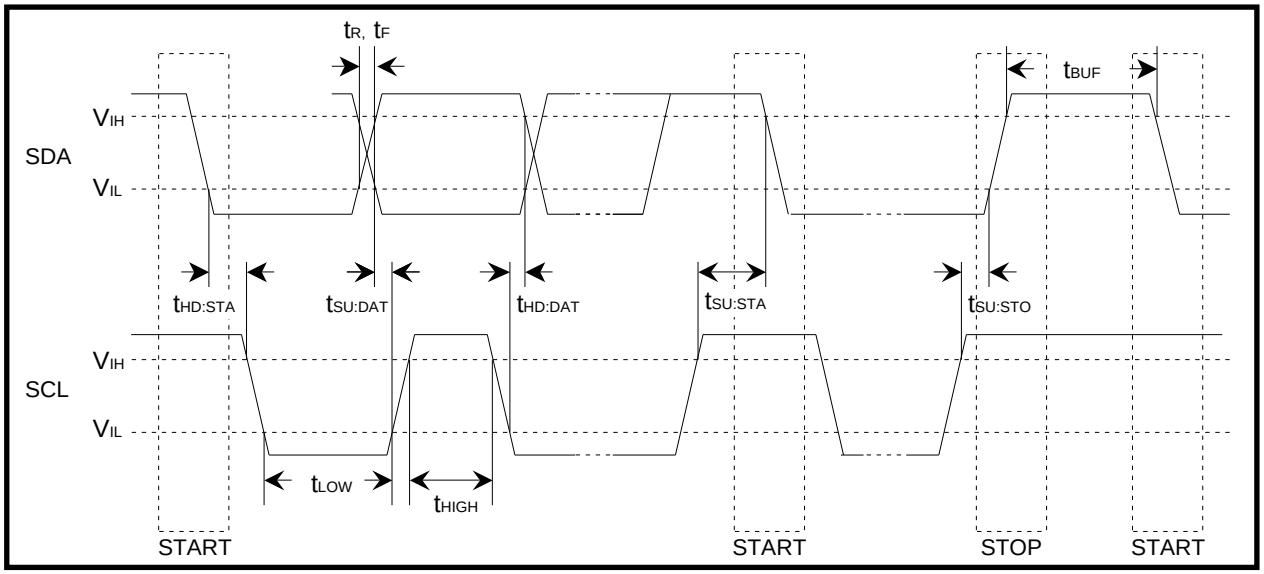
Symbol	Parameter	Test conditions	Ratings			Unit
			MIN	TYP	MAX	
V_{CC}	Supply voltage		2.4V_{DD}		13	V
I_{CC}	Supply current	CLK=1MHz Operation I_{AO}=0µA		2.0	4.0	mA
IrefU	D–A converter upper reference voltage input current	VrefU=5V,VrefL=0V Data condition: at maximum current		1.2	2.5	mA
VrefU	D–A converter upper reference voltage range	The output dose not necessarily be the values within the reference voltage setting range.	3.5		V_{DD}	V
VrefL	D–A converter lower reference voltage range		GND		1.5	V
V_{AO}	Buffer amplifier output voltage range	I_{AO}=±500µA	0.1		V_{CC}-0.1	V
		I_{AO}=±1.0mA	0.2		V_{CC}-0.2	V
I_{AO}	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	–2.5		2.5	mA
S_{DL}	Differential nonlinearity error	VrefU=4.79V VrefL=0.95V V_{CC}=13V(36mV/LSB) without load (I_{AO}=0)	–1.0		1.0	LSB
S_L	Nonlinearity error		–1.5		1.5	LSB
S_{ZERO}	Zero code error		–2.0		2.0	LSB
S_{FULL}	Full scale error		–2.0		2.0	LSB
SR	Output slew rate			0.2		V/µs

I2C BUS LINE CHARACTERISTICS

Symbol	Parameter	Normal mode		High speed mode		units
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	KHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold time START Condition. After this period,the first clock pulse is generated.	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the clock	4.7	-	1.3	-	µs
t_{HIGH}	High period of the clock	4.0	-	0.6	-	µs
$t_{SU:STA}$	Set-up time for START condition (Only relevant for a repeated START condition)	4.7	-	4.7	-	µs
$t_{HD:DAT}$	Hold time DATA	0	-	0	0.9	µs
$t_{SU:DAT}$	Set-up time DATA	250	-	100	-	ns
t_R	Rise time of both SDA and SCL lines	-	1000	20+	300	ns
t_F	Fall time of both SDA and SCL lines	-	300	20+	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max.300 ns) of the falling edge of SCL.

TIMING CHART



I2C- BUS FORMAT

STA	SLAVE ADDRESS	W	A	SUB ADDRESS	A	DAC DATA	A	STP

DIGITAL DATA FORMAT

•SLAVE ADDRESS

First → Last

1	0	0	1	A2	A1	A0
(SLAVE ADDRESS)				CHIP SELECT DATA		

•SUB ADDRESS

First → Last

X	X	X	X	S3	S2	S1	S0
Don't care				CHANNEL SELECT DATA			

•DAC DATA

First MSB → Last LSB

D7	D6	D5	D4	D3	D2	D1	D0

(1)CHIP SELECT DATA

MSB LSB

A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1

Lower 3bits(A0,A1,A2) are a programmable address. This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CS0 to CS2.(refer to the upper table)

(2)CHANNEL SELECT DATA

MSB LSB

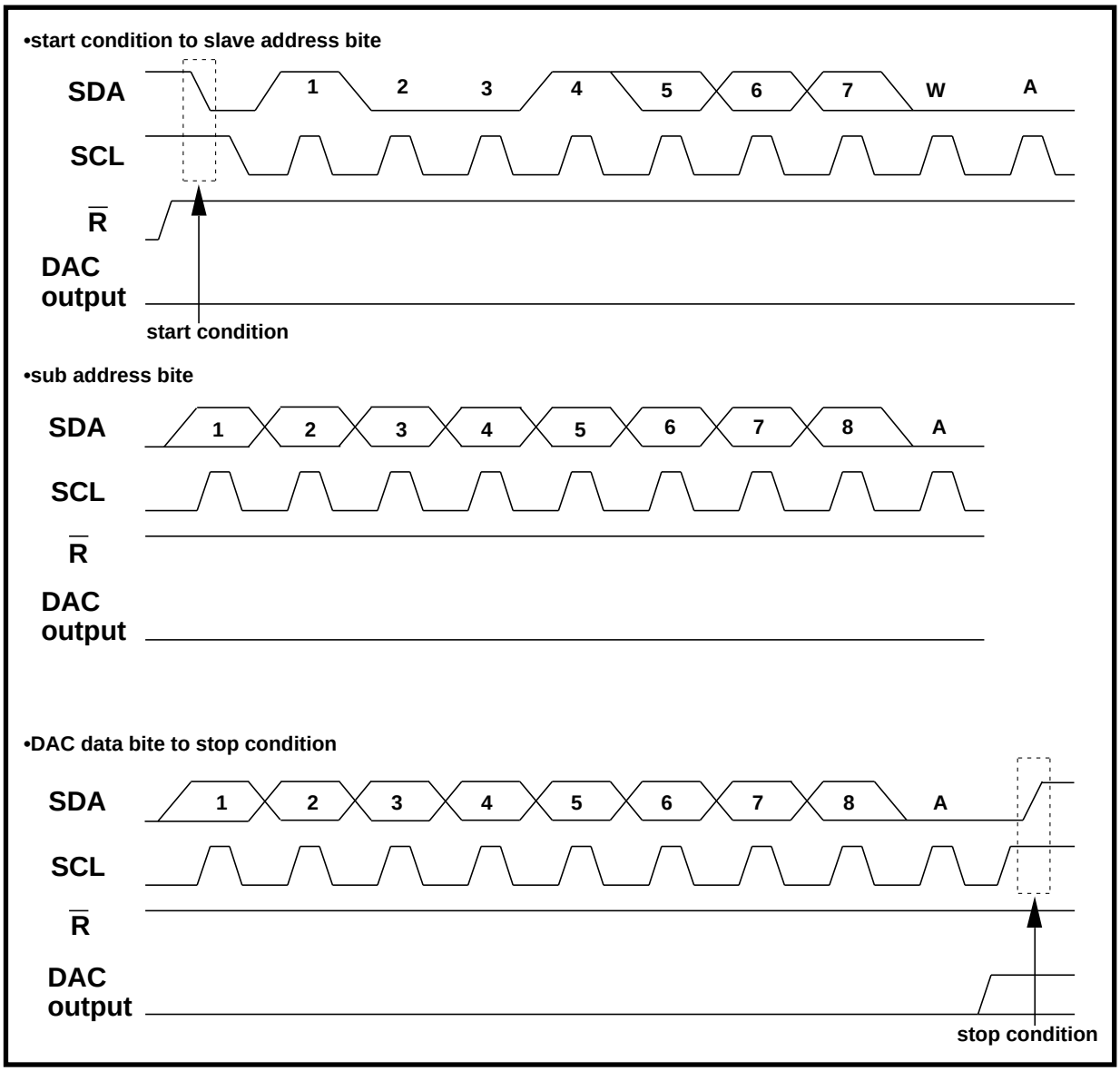
S3	S2	S1	S0	Channel selection
0	0	0	0	Don't care.
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
1	0	1	1	ch11 selection
1	1	0	0	ch12 selection
1	1	0	1	Don't care.
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care.

(3)DAC DATA

First MSB → Last LSB

D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$(V_{refU}-V_{refL})/256 \times 1 \times 2.4 + V_{refL}$
0	0	0	0	0	0	0	1	$(V_{refU}-V_{refL})/256 \times 2 \times 2.4 + V_{refL}$
0	0	0	0	0	0	1	0	$(V_{refU}-V_{refL})/256 \times 3 \times 2.4 + V_{refL}$
0	0	0	0	0	0	1	1	$(V_{refU}-V_{refL})/256 \times 4 \times 2.4 + V_{refL}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(V_{refU}-V_{refL})/256 \times 255 \times 2.4 + V_{refL}$
1	1	1	1	1	1	1	1	$(V_{refU}-V_{refL}) \times 2.4 + V_{refL}$

TIMING CHART (MODEL)



•Start condition ……. With SCL at HIGH,SDA line goes from HIGH to LOW

•Stop condition ……. With SCL at HIGH,SDA line goes from LOW to HIGH

(*Under normal circumstances,SDA is changed when SCL is LOW)

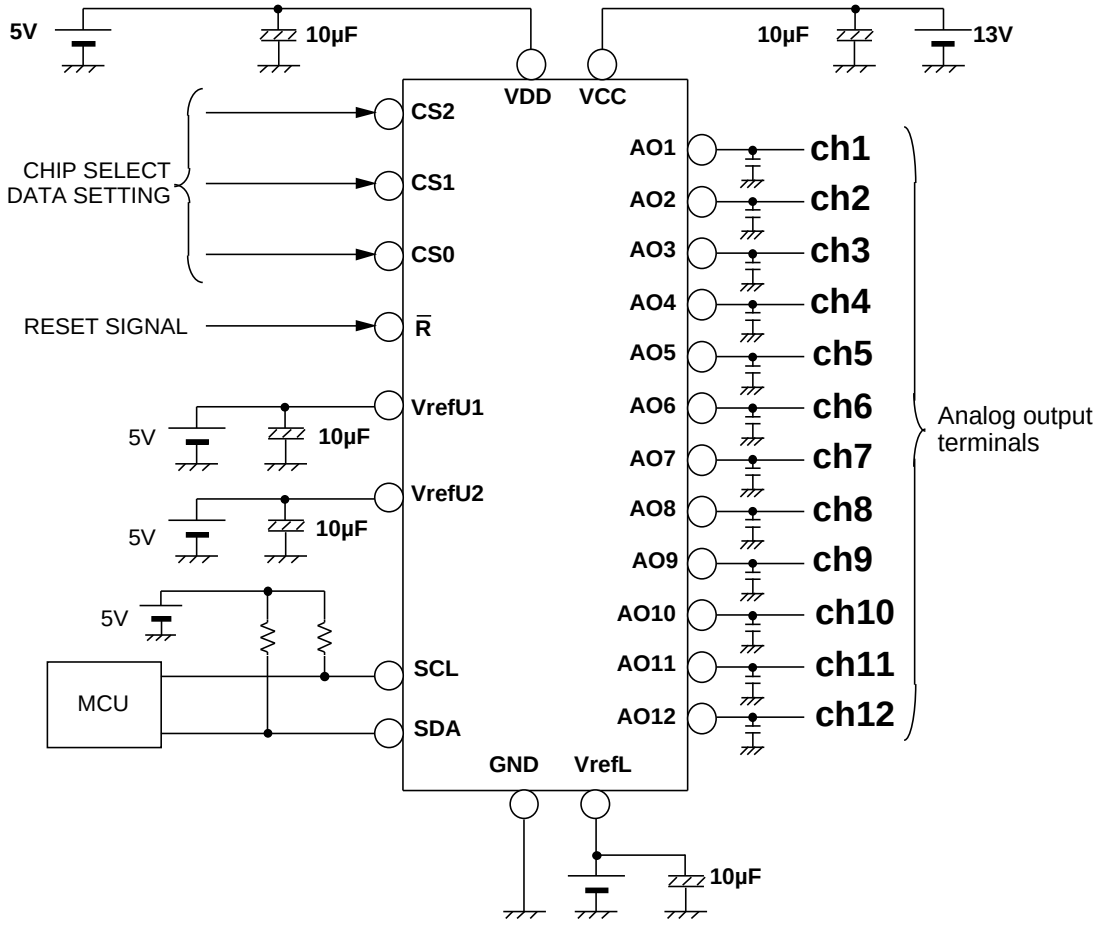
•Acknowledge bit …… The receiving IC has to pull down SDA line whenever receive slave data.
(The transmitting IC releases the SDA line just then transmit 8bit data.)

PRECAUTION FOR USE

M62398 have 5 terminals (VDD,VCC,VrefU1,VrefU2,VrefL) for input constant voltage at use.
IF ripple or spike is input these terminals,accuracy of D-A conversion is down. So,when use this device,please connect capacitor among each terminal to GND for stable D-A conversion.

This IC's output amplifier has an advantage to capacitive load.So it's no problem at device action when connect capacitor (0.1μF MAX) among output to GND for every noise eliminate.

<Standard application circuit>



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