

## HAT2200R

Silicon N Channel Power MOS FET  
Power Switching

REJ03G0232-0200Z

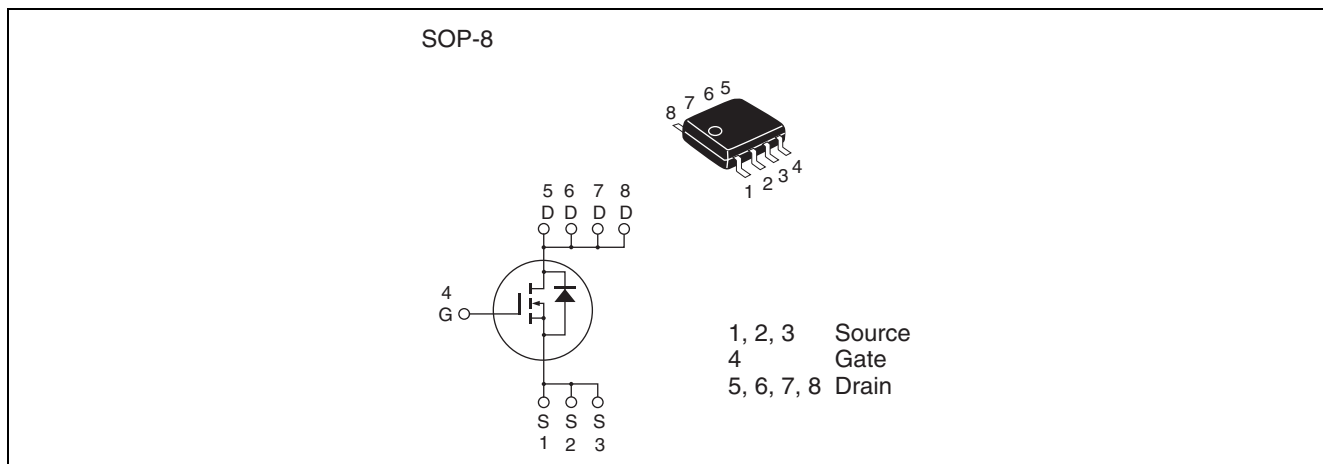
Rev.2.00

Apr.05.2004

### Features

- Capable of 8 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 22 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )

### Outline



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	100	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	8	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	64	A
Body-drain diode reverse drain current	I <sub>DR</sub>	8	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	8	A
Avalanche energy	E <sub>AR</sub> <sup>Note 2</sup>	6.4	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	2.5	W
Channel to Ambient Thermal Impedance	θ <sub>ch-a</sub> <sup>Note3</sup>	50	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
 2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
 3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

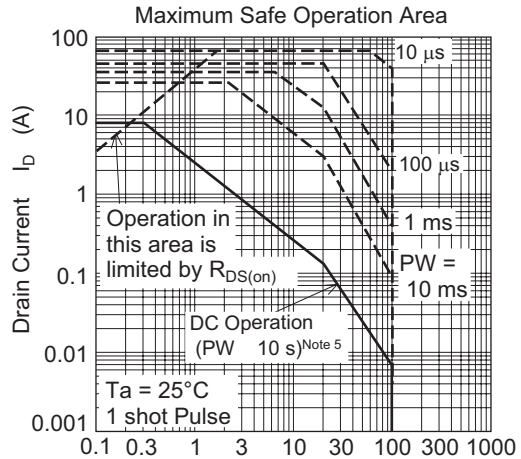
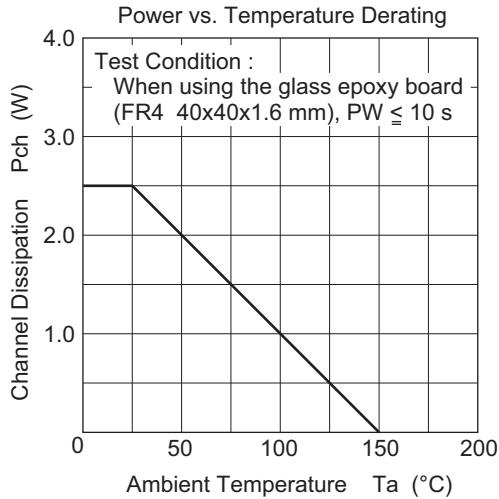
## Electrical Characteristics

(Ta = 25°C)

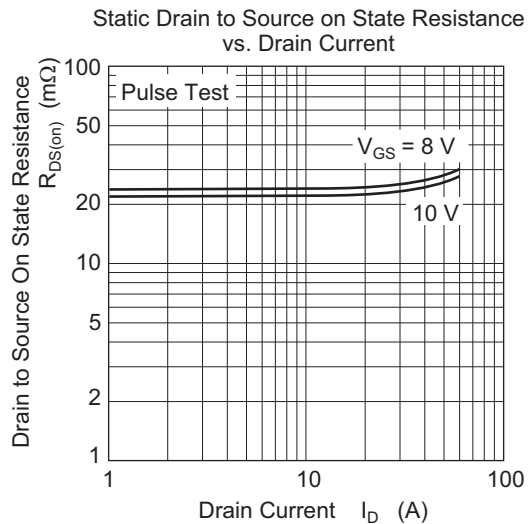
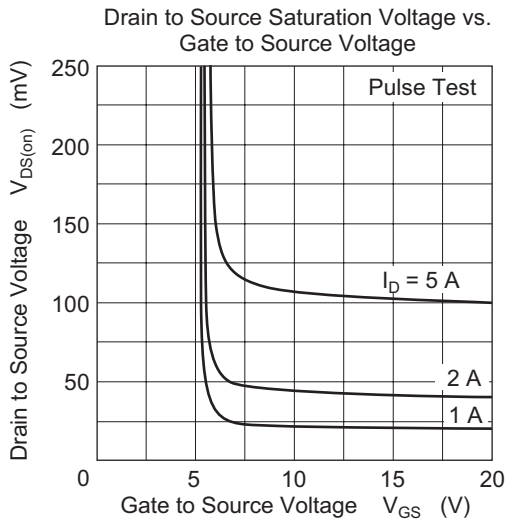
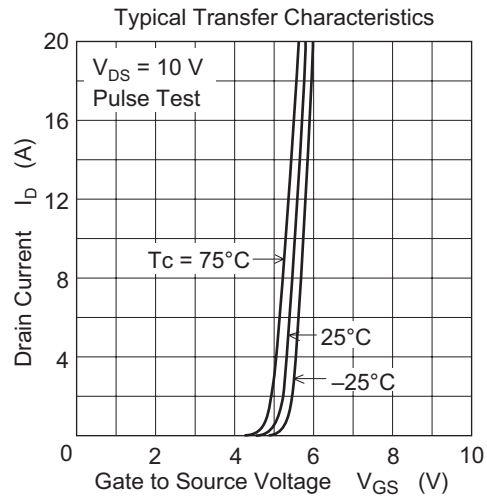
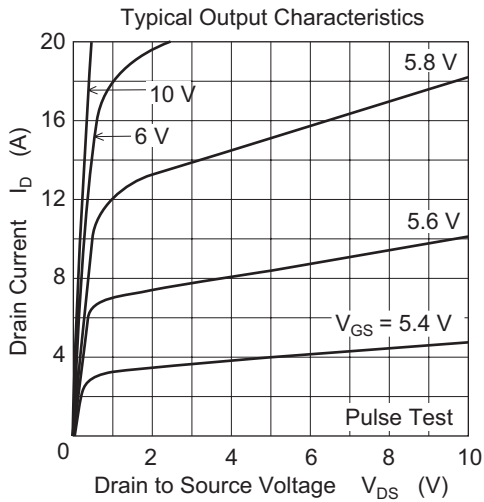
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	100	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	± 0.1	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	3.5	—	5.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	22	28	mΩ	I <sub>D</sub> = 4 A, V <sub>GS</sub> = 10 V <sup>Note4</sup>
	R <sub>DS(on)</sub>	—	23	33	mΩ	I <sub>D</sub> = 4 A, V <sub>GS</sub> = 8 V <sup>Note4</sup>
Forward transfer admittance	y <sub>fs</sub>	8	14	—	S	I <sub>D</sub> = 4 A, V <sub>DS</sub> = 10 V <sup>Note4</sup>
Input capacitance	C <sub>iss</sub>	—	2300	—	pF	V <sub>DS</sub> = 10 V
Output capacitance	C <sub>oss</sub>	—	280	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	90	—	pF	f = 1 MHz
Gate Resistance	R <sub>g</sub>	—	1.3	—	Ω	
Total gate charge	Q <sub>g</sub>	—	32	—	nC	V <sub>DD</sub> = 50 V
Gate to source charge	Q <sub>gs</sub>	—	12	—	nC	V <sub>GS</sub> = 10 V
Gate to drain charge	Q <sub>gd</sub>	—	8	—	nC	I <sub>D</sub> = 8 A
Turn-on delay time	t <sub>d(on)</sub>	—	16	—	ns	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A
Rise time	t <sub>r</sub>	—	4	—	ns	V <sub>DD</sub> ≅ 30 V
Turn-off delay time	t <sub>d(off)</sub>	—	32	—	ns	R <sub>L</sub> = 7.5 Ω
Fall time	t <sub>f</sub>	—	4.5	—	ns	R <sub>g</sub> = 4.7 Ω
Body–drain diode forward voltage	V <sub>DF</sub>	—	0.79	1.03	V	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 <sup>Note4</sup>
Body–drain diode reverse recovery time	t <sub>rr</sub>	—	45	—	ns	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0 diF/ dt = 100 A/ μs

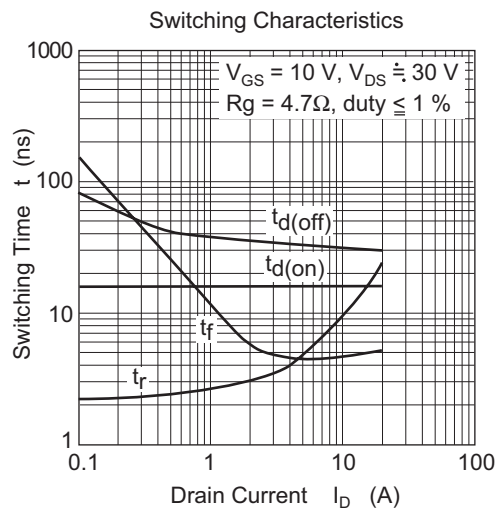
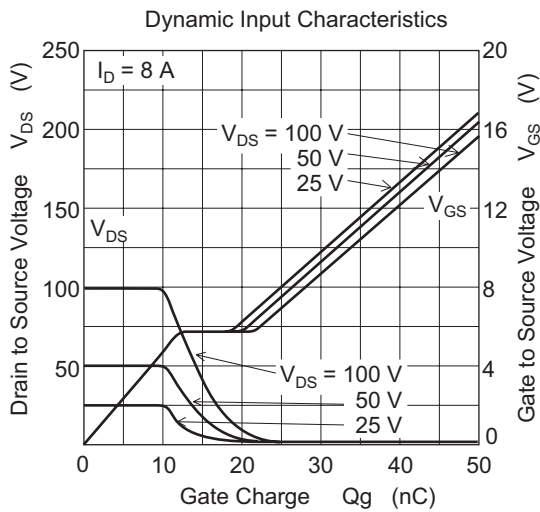
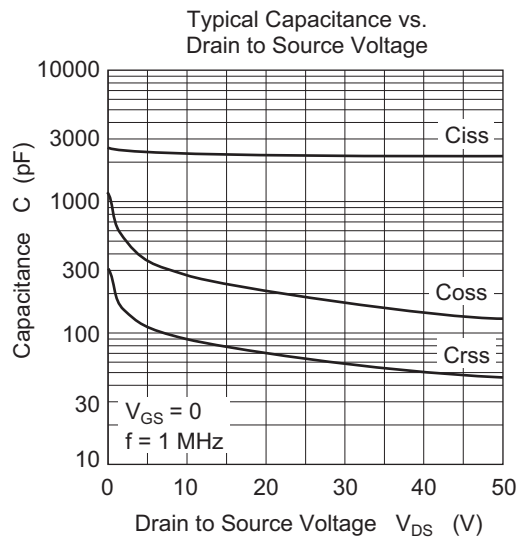
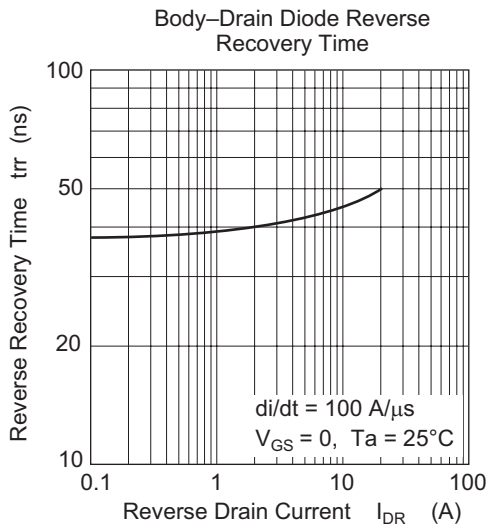
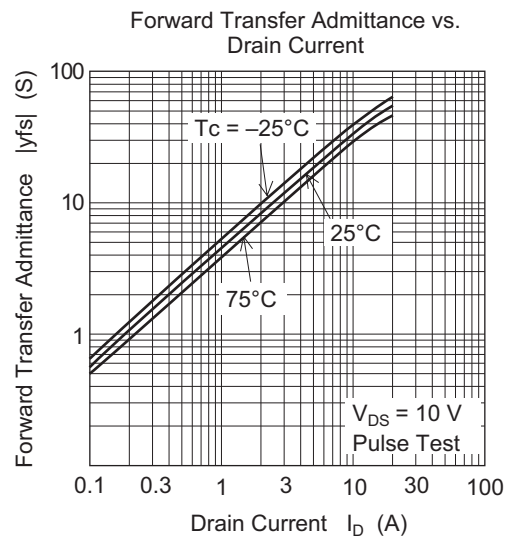
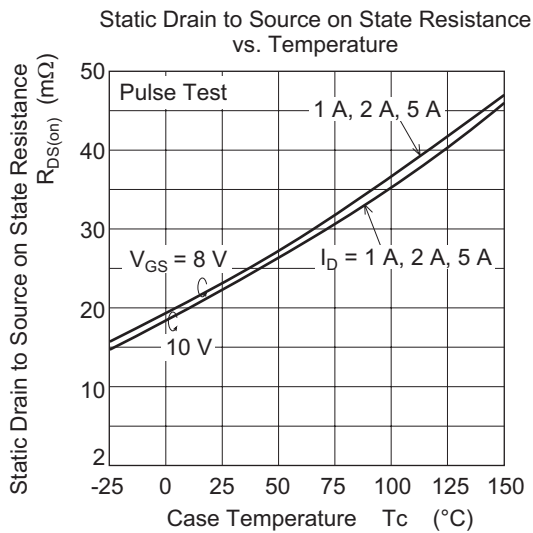
- Notes: 4. Pulse test

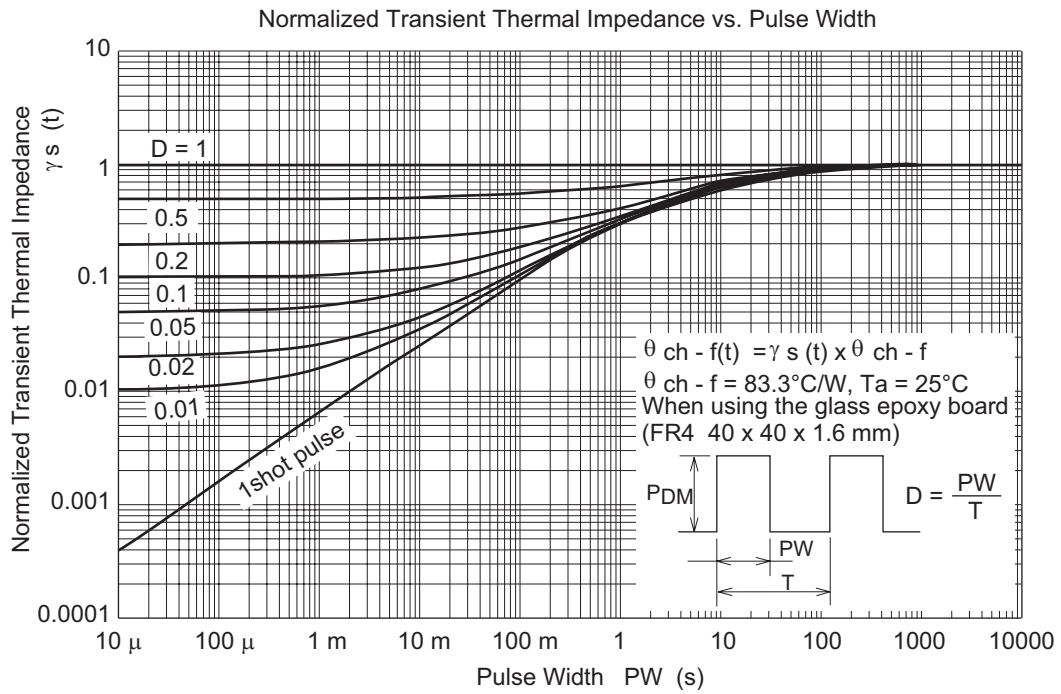
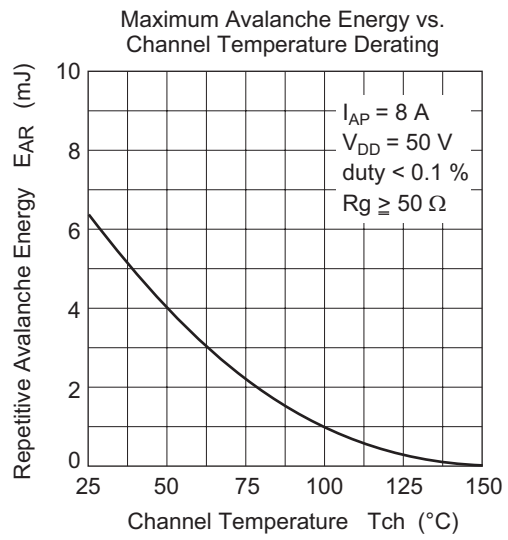
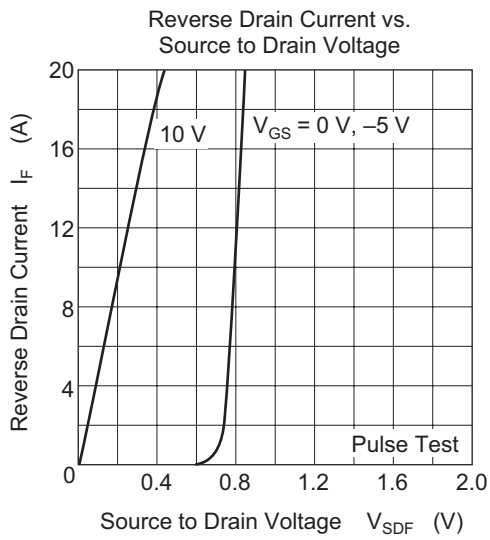
Main Characteristics



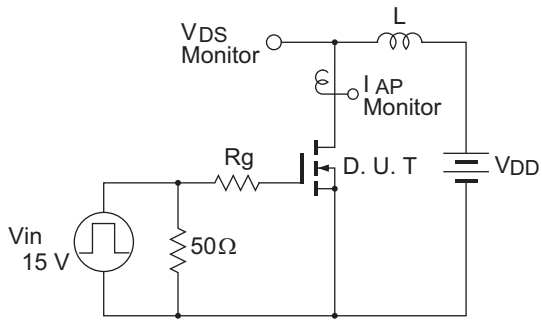
Note 5 :  
When using the glass epoxy board  
(FR4 40x40x1.6 mm)





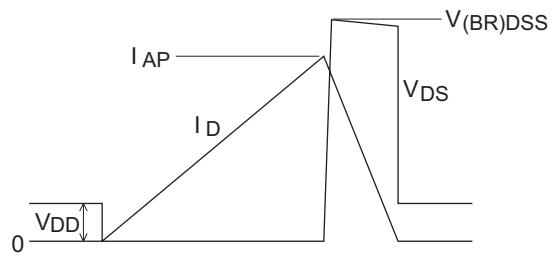


Avalanche Test Circuit

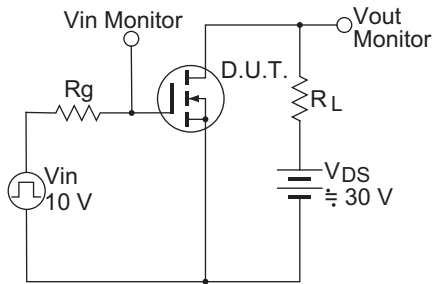


Avalanche Waveform

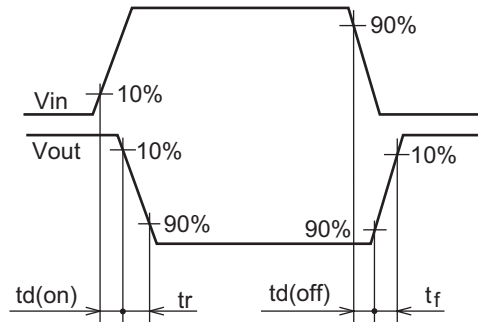
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

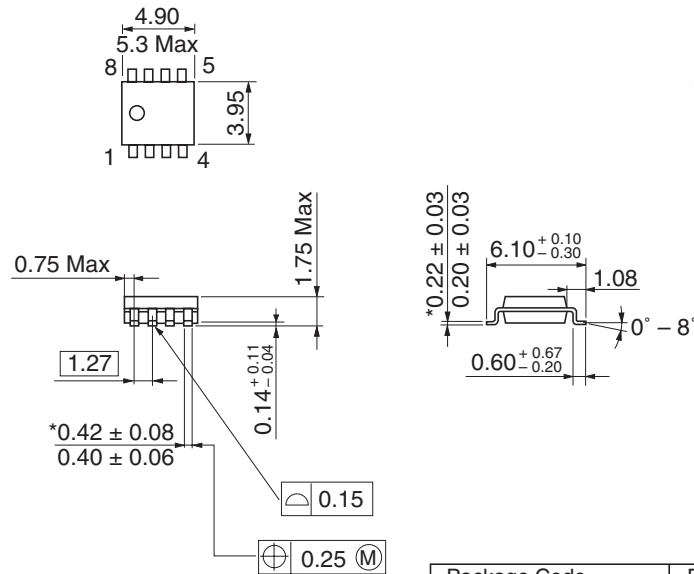


Switching Time Waveform



Package Dimensions

As of January, 2003  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT2200R-EL-E	2500pcs	Taping

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