TOPAZ SEMICONDUCTOR

SD217, SD219

N-CHANNEL ENHANCEMENT-MODE D-MOS POWER FET

ORDERING INFORMATION

TO-206AF (TO-72) Package	SD217DE	SD219DE
Shorting Ring	SD217DE/R	SD219DE/R
Sorted Chips In Waffle Pack	SD217CHP	SD219CHP
Description	6.0 ohm, 25V V_{SB} = 15V min	6.0 ohm, 25V V_{SB} = 20V min

FEATURES

- CMOS Compatible Input
- Small Package, Standard Pin-Out
- TTL and CMOS Compatible Input
- Low Capacitance
- Peak Pulsed Current, 1 Amp min

APPLICATIONS

- ±10V Analog Switch, SD219DE
- ±7.5 Analog Switch, SD217DE
- High Speed, Medium Power, Switch Drivers
- Sample and Hold and Track and Hold
- A-to-D and D-to-A Converters

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise specified)

V_{DS} Drain-Source Voltage ..... +25V

V_{DB} Drain-Body Voltage
- SD217 ..... +22.5V
- SD219 ..... +25V

V_{SD} Source-Drain Voltage
- SD217 ..... +15V
- SD219 ..... +20V

V_{SB} Source-Body Voltage
- SD217 ..... +22.5V
- SD219 ..... +25V

V_{GB} Gate-Body Voltage ..... +30V

V_{GS} Gate-Source Voltage ..... ±22.5V

V_{GD} Gate-Drain Voltage ..... ±22.5V

I_D Peak Pulsed Drain Current ..... +1.0A

I_D Continuous Drain Current (Note 1) 160mA

P_D Continuous Power Dissipation (Note 1)
- T_A = +25°C (Free Air) 300mW
- T_C = +25°C (Infinite Heat Sink) 1.2W

Power Derating Factors (Note 1)
- Free Air ..... 3.0mW/°C
- Infinite Heat Sink ..... 12mW/°C

Thermal Resistance (Note 1)

O_{ja} Junction to Ambient ..... 333°C/W

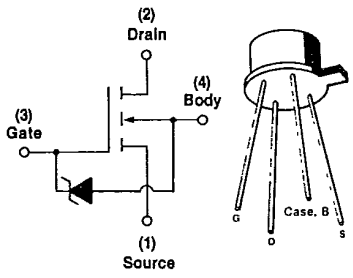
O_{jc} Junction to Case ..... 83°C/W

T_{op} Operating Junction Temperature Range ..... -55 to +125°C

T_{stg} Storage Temperature Range ..... -55 to +150°C

Note 1: Not applicable to chips. Final value depends on mounting.

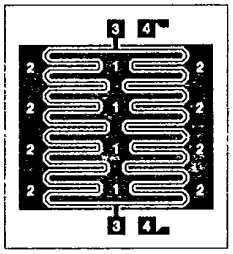
SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



1—Drain 2—Source 3—Gate 4—Diode
Minimum bonding required. One Drain, One Source (left), One Source (right), One Gate. Bond Gate and Adjacent Diode to Common Point to Connect Protective Diode.

Size: .040 x .044 x .013 inch.
Body (Substrate) is backside contact.

TOPAZ SEMICONDUCTOR

SD217, SD219

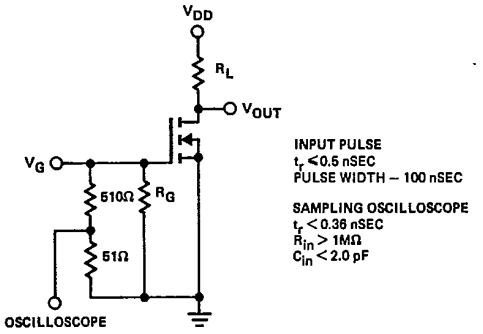
T-35-25

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)

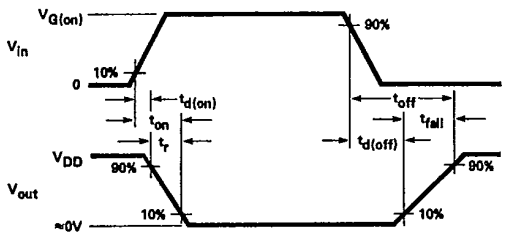
#		CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage		25	30		V	I_D = 10μA, V_{GS} = V_{BS} = 0
2				15	20			I_D = 100nA, V_{GS} = V_{BS} = -5V
3		BV_{SD} Source-Drain Breakdown Voltage	SD217	15			V	I_S = 100nA, V_{GD} = V_{BD} = -5V
4			SD219	20				
5		BV_{DB} Drain-Body Breakdown Voltage	SD217	22.5			V	I_D = 100nA, V_{GB} = 0, Source Open
6			SD219	25				
7		BV_{SB} Source-Body Breakdown Voltage	SD217	22.5			V	I_S = 100nA, V_{GB} = 0, Drain Open
8			SD219	25				
9		$I_{D(off)}$ Drain-Source OFF Leakage Current				100	nA	V_{DS} = 15V, V_{GS} = V_{BS} = -5V
10		$I_{S(off)}$ Source-Drain OFF Leakage Current				100		V_{SD} = 15V, V_{GD} = V_{BD} = -5V
11		I_{GB} Gate-Body ON Leakage Current				10	μA	V_{GB} = 30V, V_{GS} = V_{GD} = 22.5V
12		$V_{GS(th)}$ Gate-Source Threshold Voltage		0.1		2.0	V	V_{DS} = V_{GS}, I_D = 10μA, V_{SB} = 0
13		$I_{D(on)}$ Drain-Source ON Current (Note 1)		1.0			A	V_{DS} = V_{GS} = 10V, V_{SB} = 0
14		$r_{DS(on)}$ Drain-Source ON Resistance (Note 1)				8.0	ohms	V_{GS} = 5.0V, I_D = 50mA, V_{SB} = 0
15						6.0		
16						6.0		V_{GS} = 10V, I_D = 500mA, V_{SB} = 0
17	DYNAMIC	g_{fs} Common-Source (Note 1) Forward Transconductance		100			mmhos	V_{DS} = 15V, I_D = 200mA, V_{SB} = 0, F = 1KHz
18		$C_{(gs+gd+gb)}$ Gate Node Capacitance				30	pF	V_{DS} = 10V, $V_{GS}V_{BS}$ = -15V, f = 1MHz
19		$C_{(gd+db)}$ Drain-Node Capacitance				15		
20		$C_{(gs+sb)}$ Source Node Capacitance				40		
21		$C_{(dg)}$ Reverse Transfer Capacitance				5.0		
22		t_{on} Turn ON Time			2.0	4.0	nS	V_{DD} = 10V, $V_{G(on)}$ = 10V, R_L = 133Ω, R_G = 51Ω
23		t_{off} Turn OFF Time			3.0	5.0		

Note 1: Pulse Test 80μSec, 1% Duty Cycle

SWITCHING TIMES TEST CIRCUIT

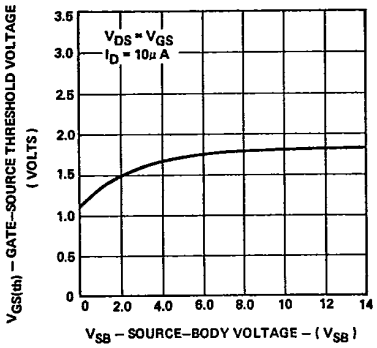


TEST WAVEFORMS

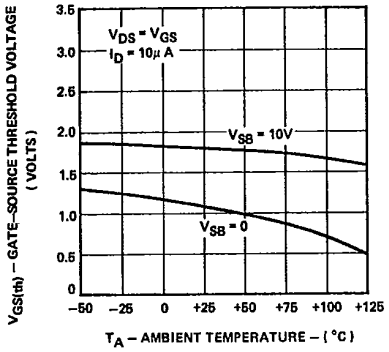


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = +25°C unless otherwise specified)

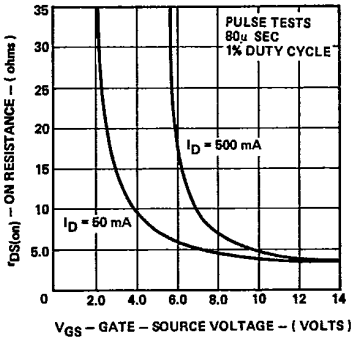
GATE-SOURCE THRESHOLD VOLTAGE —VS— SOURCE-BODY VOLTAGE



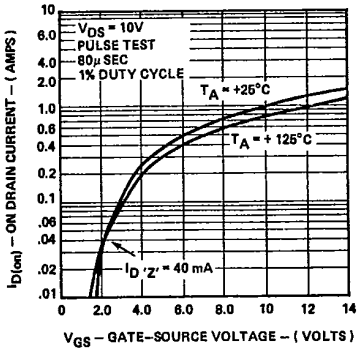
GATE-SOURCE THRESHOLD VOLTAGE —VS— TEMPERATURE



DRAIN-SOURCE ON RESISTANCE —VS— GATE-SOURCE VOLTAGE



ON DRAIN CURRENT —VS— GATE-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE —VS— ON DRAIN CURRENT