MOTOROLA

MC4316 • MC4016
MC4317 • MC4017
MC4318 • MC4018
MC4319 • MC4019

PROGRAMMABLE MODULO-N COUNTERS

The monolithic devices are programmable, cascadable, modulo-N-counters. The MC4316/4016 can be programmed to divide by any number (N) from 0 thru 9, the MC4318/4018 from 0 thru 15. The MC4317/4017 consists of a modulo 2 counter which can be programmed to divide by 0 or 1 and a modulo 5 counter which can be programmed to divide by any number from 0 to 4. The MC4319/4019 contains two modulo 4 counters which can be programmed to divide by any number from 0 to 3.

The parallel enable ($\overline{PE}$) input enables the parallel data inputs D0 thru D3. All zeros are entered into the counter by applying a logic "0" level to the master reset ($\overline{MR}$) and $\overline{PE}$ inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

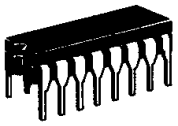
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

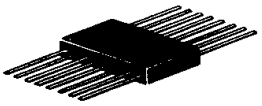
Input Loading Factor:
Clock, $\overline{PE}$ = 2
D0, D1, D2, D3, Gate = 1
$\overline{MR}$ = 4
Output Loading Factor = 8

Total Power Dissipation = 250 mW typ/pkg
Propagation Delay Time:
Clock to Q3 = 50 ns typ
Clock to Bus = 35 ns typ

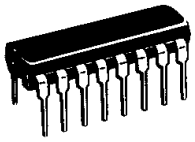
PROGRAMMABLE MODULO-N COUNTERS



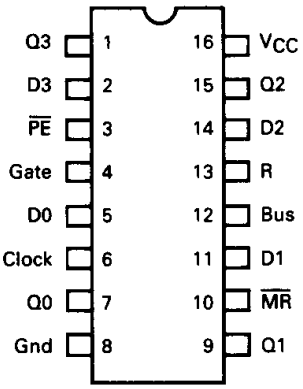
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



P SUFFIX
PLASTIC PACKAGE
CASE 648



MC4316/4016
MC4318/4018

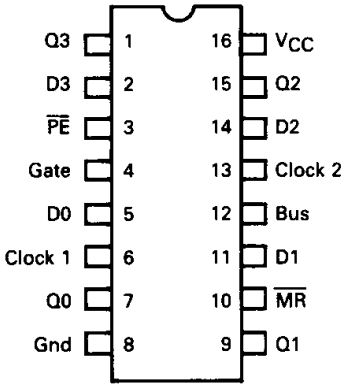
V_{CC} = Pin 16
Gnd = Pin 8

MC4316/4016

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC4318/4018

COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



MC4317/4017
MC4319/4019

V_{CC} = Pin 16
Gnd = Pin 8

MC4317/4017

COUNT	OUTPUT
	Q0
1	1
0	0

COUNT	OUTPUT		
	Q3	Q2	Q1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0

MC4319/4019

COUNT	OUTPUT	
	Q1	Q0
3	1	1
2	1	0
1	0	1
0	0	0

COUNT	OUTPUT	
	Q3	Q2
3	1	1
2	1	0
1	0	1
0	0	0

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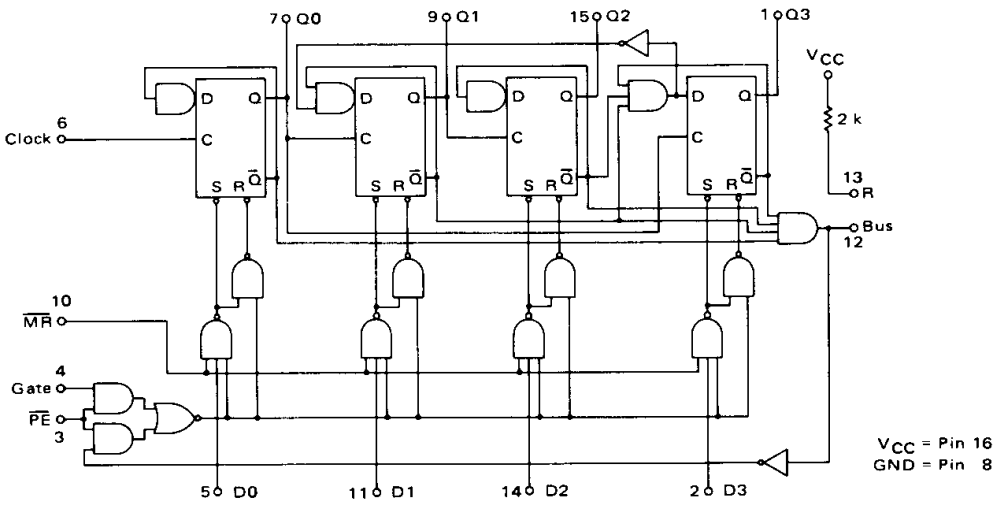
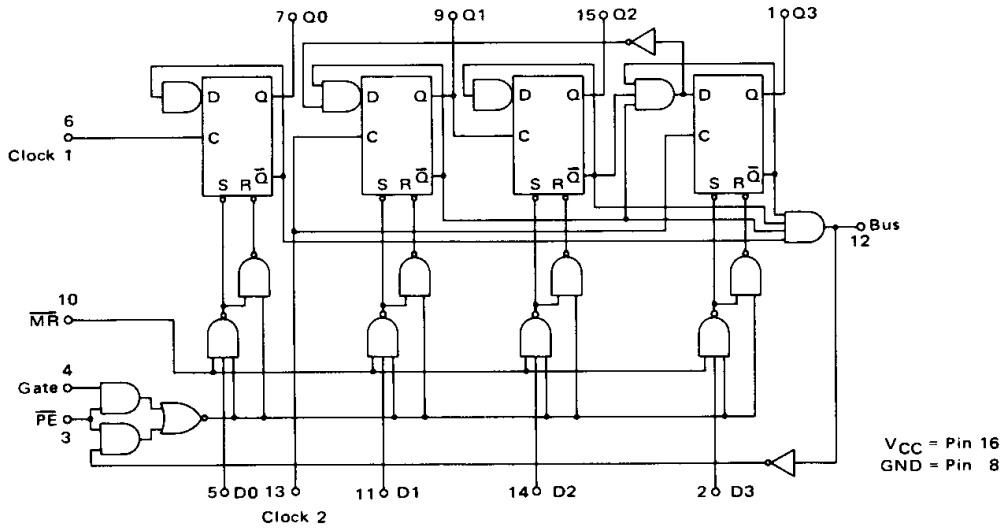
LOGIC DIAGRAMS

MC4316/4016

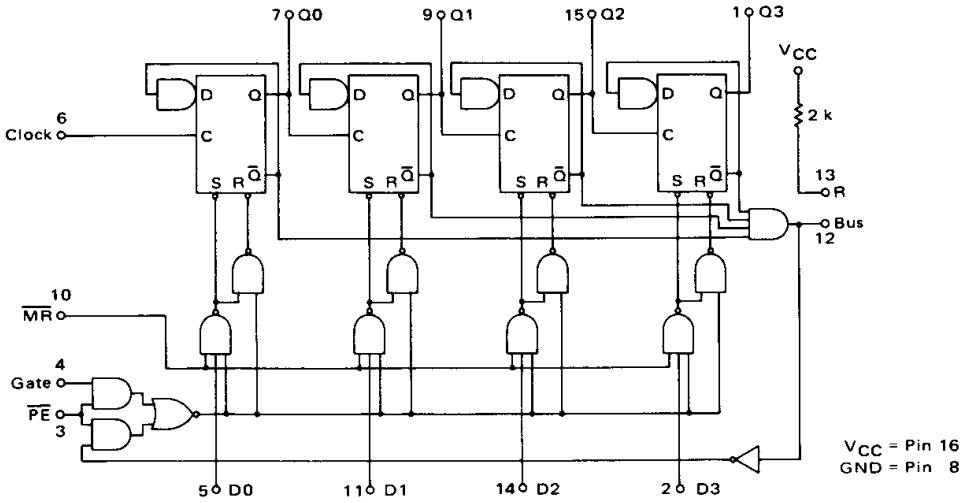


MC4317/4017

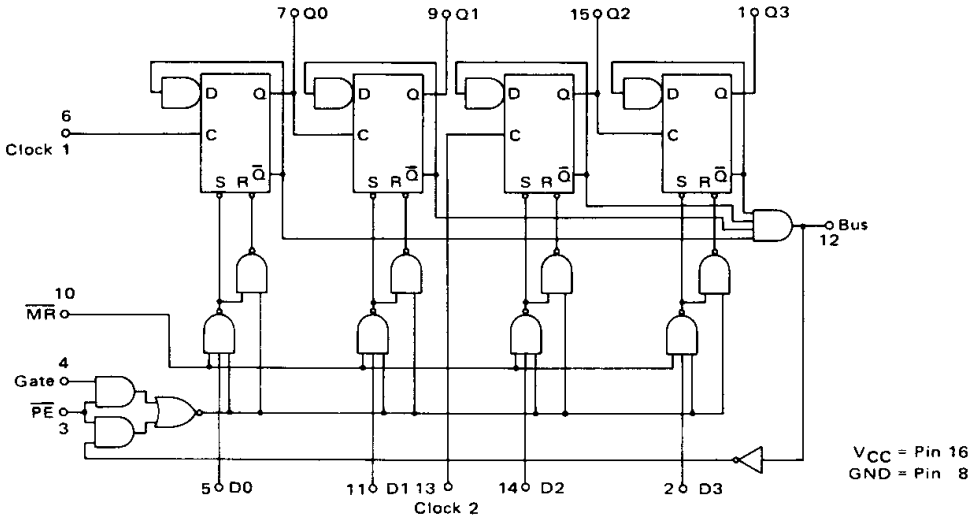


LOGIC DIAGRAMS (continued)

MC4318/4018



MC4319/4019



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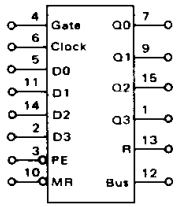
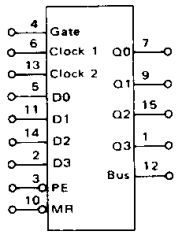
ELECTRICAL CHARACTERISTICS

Tests are shown for one output only.
Others are tested in the same manner.

MC4316/4016
MC4318/4018



MC4317/4017
MC4319/4019

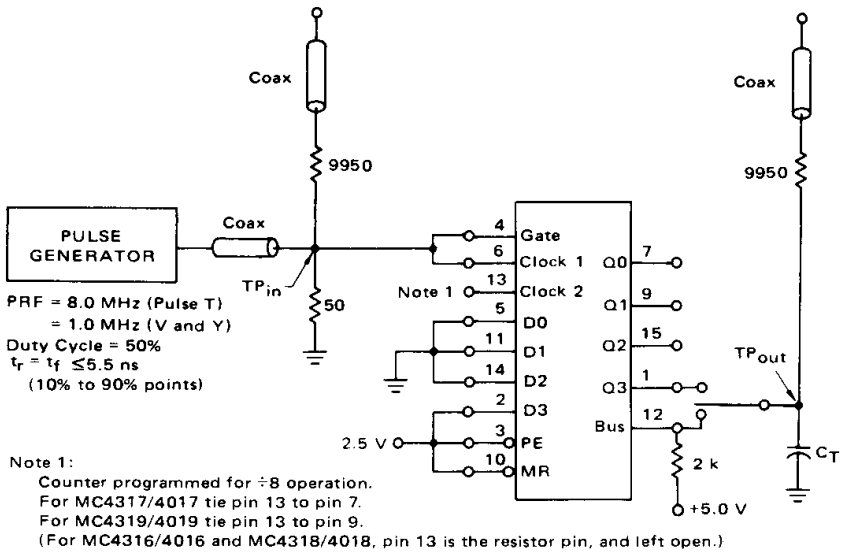


	@ Test Temperature	I_{OL1} (mA)	I_{OL2} (mA)	I_{OL3} (mA)	I_{OH} (mA)	I_{IC} (mA)	V_{IL} (Volts)	V_{IH} (Volts)	V_{IHH} (Volts)	V_{ILT} (Volts)	V_{IHT} (Volts)	V_{CC} (Volts)	V_{CCL} (Volts)	V_{CCH} (Volts)
MC4316–4019	-55°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
	+125°C	12.8	13.8	9.6	-1.6	–	0.4	2.4	5.5	0.8	2.0	5.0	4.5	5.5
MC4016–4019	0°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+25°C	12.8	13.8	9.6	-1.6	-10	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25
	+75°C	12.8	13.8	9.6	-1.6	–	0.4	2.5	5.5	0.8	2.0	5.0	4.75	5.25

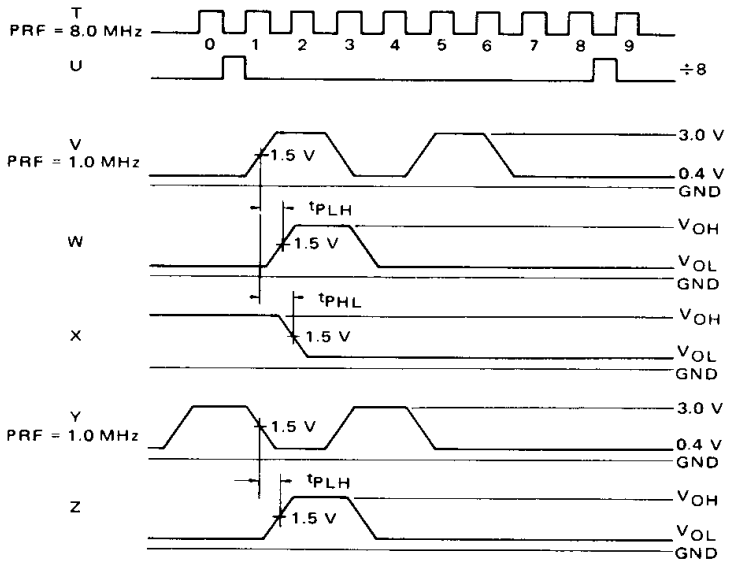
Characteristic	Symbol	Pin Under Test	MC4316–4319 Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Max	+125°C Min	+125°C Max	MC4016–4019 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	I_{OL1}	I_{OL2}	I_{OL3}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{ILT}	V_{IHT}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:												
Forward Current	I_{IL1}	2		-1.6		-1.6		-1.6		-1.6		-1.6		-1.6	mAdc	–					2	10	–	–	–	–	–	16	3,8
		3		-3.2		-3.2		-3.2		-3.2		-3.2		-3.2							3	4	–	–	–	–	–		8,12
		4		-1.6		-1.6		-1.6		-1.6		-1.6		-1.6							4	3	–	–		–			8
		5	–	-1.6	–	-1.6		-1.6		-1.6		-1.6		-1.6							5	10	–			–			3,8
		6		-3.2		-3.2		-3.2		-3.2		-3.2		-3.2							6		–			–	–		8
		10		-6.4		-6.4		-6.4		-6.4		-6.4		-6.4			–	–	–		10	2,5,11,14	–			–	–		3,8
		11	–	-1.6	–	-1.6		-1.6		-1.6		-1.6		-1.6							11	10	–			–			
		14		-1.6		-1.6		-1.6		-1.6		-1.6		-1.6	↓						14	10	–			–	–	↓	↓
	I_{IL2}	2	–	-1.4		-1.4		-1.4		-1.4		-1.4		-1.4	mAdc						2	10	–				16		3,8
		3		-2.8		-2.8		-2.8		-2.8		-2.8		-2.8							3	4	–			–			8,12
		4		-1.4		-1.4		-1.4		-1.4		-1.4		-1.4							4	3	–						8
		5		-1.4		-1.4		-1.4		-1.4		-1.4		-1.4							5	10	–						3,8
		6*		-2.8		-2.8		-2.8		-2.8		-2.8		-2.8							6		–						8
		10	–	-5.6		-5.6		-5.6		-5.6		-5.6		-5.6					–		10	2,5,11,14	–			–			3,8
		11		-1.4		-1.4		-1.4		-1.4		-1.4		-1.4							11	10	–			–			
		14		-1.4		-1.4		-1.4		-1.4		-1.4		-1.4	↓	–					14	10	–			–	↓		↓
Leakage Current	I_{IH}	2		40		40		40		40		40		40	μAdc							2	–	–				16	8,10
		3		80		80		80		80		80		80								3	–				–		4,8
		4		40		40		40		40		40		40								4	–			–	–		3,8
		5		40		40		40		40		40		40								5	–			–	–		8,10
		6		80		80		80		80		80		80								6	–			–	–		8
		10		160	–	160		160		160		160		160								10	–			–	–		2,5,8,11,14
		11		40		40		40		40		40		40								11	–			–	–		8,10
		14		40		40		40		40		40		40	↓							14	–			–	–	↓	8,10
	I_{IHH}	2	1.0	–	1.0		1.0		1.0	–	1.0		1.0		mAdc								2				–	16	8,10
		3				–																	3				–		4,8
		4																					4				–		3,8
		5																					5				–		8,10
		6																					6				–		8
		10																					10				–		2,5,8,11,14
		11																					11				–		8,10
		14													↓								14				–	↓	8,10
Clamp Voltage	V_{IC}	2**	–	–	–	-1.5	–	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	2	–	–	–	–	–	–	16	–	8
Output																													
Output Voltage	V_{OL}	1	–	0.4	–	0.4		0.4		0.4		0.4		0.4	Vdc	1	–	–					–	2,3,5,11,14	–		16		8
		1	–	0.4	–	0.4		0.4		0.4		0.4		0.4			1						–	2,3,5,11,14	–			16	
		12	–	0.5	–	0.5		0.5		0.5	–	0.5		0.5	↓	–	–	12				–	–	3	2,5,11,14		16	–	↓
	V_{OH}	1	2.4	–	2.4		2.4	–	2.5		2.5		2.5	–	Vdc			–	1		–		–	3	2,5,11,14		16	–	8
Short-Circuit Current	I_{OS}	1	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	-20	-65	mAdc						3	2,5,11,14	–			16	–	–	1,8
		13#	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	-1.8	-3.8	mAdc	–							–			16	–	–	8,13
Power Requirements (Total Device)																													
Power Supply Drain	I_{CC}	16			–	65						65	–	–	mAdc	–	–	–	–		–	–	–	–		16	–	–	8

*For MC4317/4017 and MC4319/4019 also test pin 13 using the same procedure except V_{IL} applied to pin 13.
**Test all inputs in the same manner.
#Test applies only to MC4316/4016 and MC4318/4018.

SWITCHING TIME TEST CIRCUIT AND VOLTAGE WAVEFORMS



Note 1:
Counter programmed for ÷8 operation.
For MC4317/4017 tie pin 13 to pin 7.
For MC4319/4019 tie pin 13 to pin 9.
(For MC4316/4016 and MC4318/4018, pin 13 is the resistor pin, and left open.)



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SWITCHING TIME TEST PROCEDURES (T_A = 25°C)

(Letters shown in test columns refer to waveforms.)

TEST	SYMBOL	INPUT				OUTPUT		LIMITS		
		Clock Pin 6	Gate Pin 4	D0, D1, D2 Pins 5,11,14	D3,PE, MR Pins 2,3,10	Bus Pin 12	Q3 Pin 1	Min	Max	Unit
Toggle Frequency (Check before measuring propagation delay.)	f_{tog}	T	T	Gnd	2.5 V	–	U	8.0	–	MHz
Propagation Delay Clock to Bus	t_{PLH}	V	V	Gnd	2.5 V	W	–	–	65	ns
Propagation Delay Gate to Q3	t_{PLH}	Y	Y	Gnd	2.5 V	–	Z	–	35	ns
Propagation Delay Clock 1 to Q3 MC4316, 17/4016, 17 MC4318, 19/4018, 19	t_{PHL}	V	V	Gnd	2.5 V	–	X	– –	45 78	ns ns

OPERATING CHARACTERISTICS

MC4316/4016, MC4318/4018

Operation of both counters is essentially the same. The MC4316/4016 has a maximum modulus of ten while the MC4318/4018 is capable of dividing by up to sixteen. Minor differences in the programming procedure will be covered in the discussion of cascaded stages.

Suitable connections for operating a single stage are shown in Figure 1, as well as appropriate waveforms. The desired modulus is applied to the data inputs D0, D1, D2, and D3 in binary (MC4018) or binary coded decimal (MC4016) positive logic format. If a number greater than nine (BCD 1001) is applied to the MC4016, it treats the most significant bit position as a zero; if for example, binary fourteen (1110) were applied to an MC4016, the counter would divide by six. BCD eight is programmed in Figure 1. As $\overline{PE}$ is taken low the states on the parallel inputs are transferred to their respective outputs. Subsequent positive transitions of the input clock will decrement the counter until the all zero state is detected by the bus gate. The resulting positive transition of the bus line is internally inverted and fed back to the preset gating circuitry but does not yet preset the counter since the gateclock input is still high. As the clock returns to the low state the counter is set to the programmed state, taking the bus line low. The net result is one positive pulse on the bus line for every N clock pulses. The output pulse width is approximately equal to one clock pulse high time.

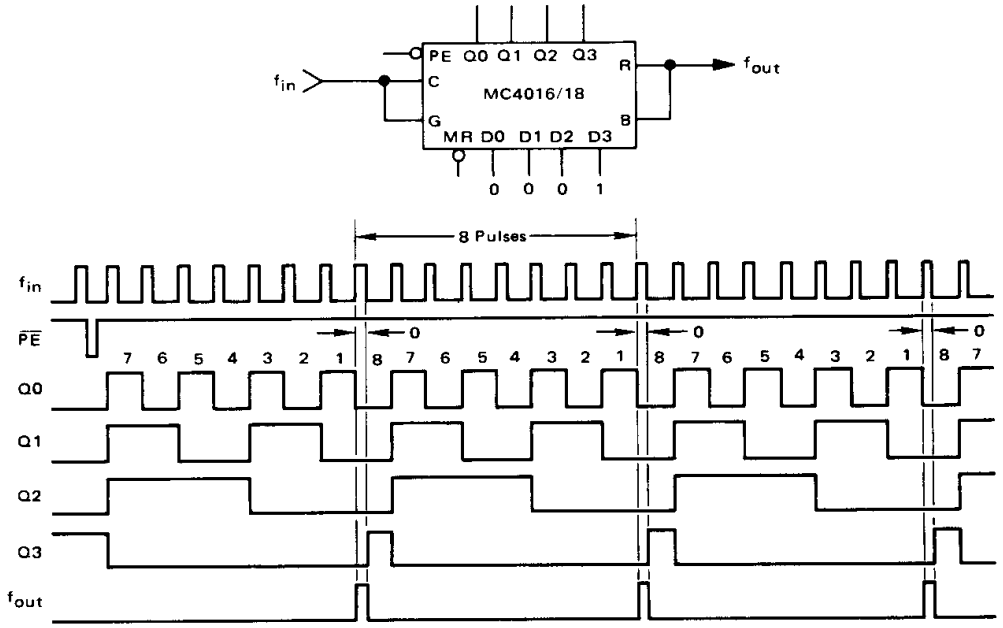
Operation will continue in this fashion until the data on the programmable inputs is changed. Since the preset circuitry is inhibited except when the counter is in the zero state, preset data may be changed while clocking is occurring. If it is necessary to enter a new number before the counter has reached zero this can be done by momentarily taking $\overline{PE}$ low. Countdown will continue from the new number on the next positive clock transition.

The counters can be made to divide by 10 (MC4016) or 16 (MC4018) by inhibiting the preset logic. This may be done by either holding the gate input high or by holding the bus line low.

The normal connections for cascading stages are indicated in Figure 2, with the appropriate waveforms. Note that the gate input of each stage is connected to the clock; all bus outputs are tied to one of the internal pullup resistors, R. The total modulus for cascaded MC4016s is determined from $N_T = N_0 + 10N_1 + 100N_2 + \ldots$; N_T for MC4018s is given by $N_T = N_0 + 16N_1 + 256N_2 + \ldots$ Stated another way, the BCD equivalent of each decimal digit is applied to respective MC4016 stages while the data inputs of the MC4018 stages are treated as part of one long binary number. The difference in programming is illustrated in Figure 2 where $N_T = 245$ is coded for both counter types.

Cascaded operation can be further clarified by referring to the timing diagram of Figure 2. For the MC4016, counting begins with the first positive clock transition after the data has been set in. After the five clock pulses, the least-significant stage has been counted down to zero. The bus line does not go high at this time since the three bus terminals are wire-ORed and the other two stages are not in the zero state. Since no reset occurs, the next positive

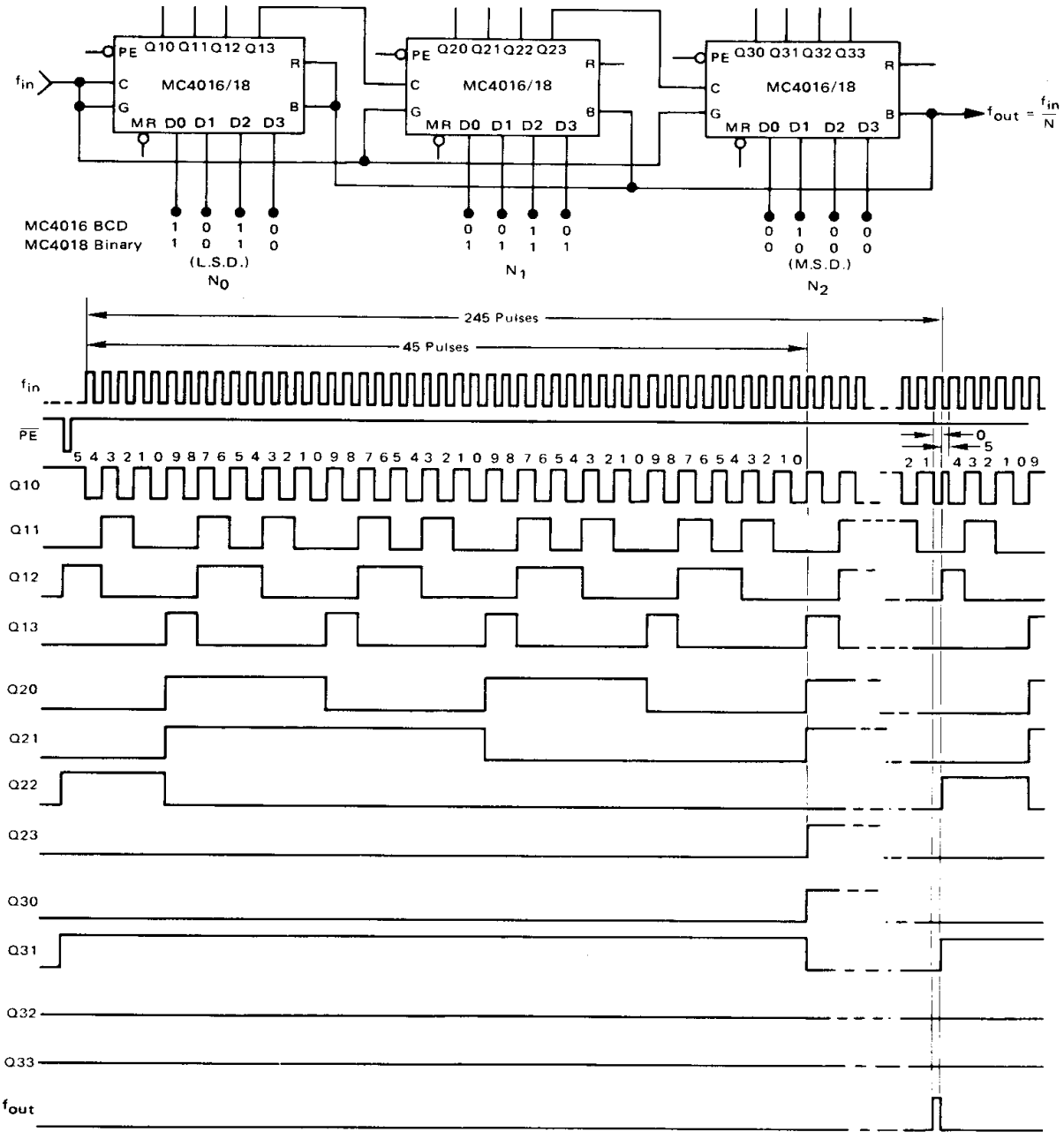
FIGURE 1 — SINGLE-STAGE OPERATION



OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

clock edge advances the least significant stage to the nine (1001) state, causing the second stage to be decremented. The process continues in this manner with the least significant stage now dividing by ten. The second stage eventually counts down to zero and also reverts to dividing by ten. Each pulse out of the second stage decrements the third until it reaches zero. At this time the bus line goes high; it remains high until the clock goes low, causing all three stages to be reset to the programmed count again.

FIGURE 2 — CASCADED OPERATION



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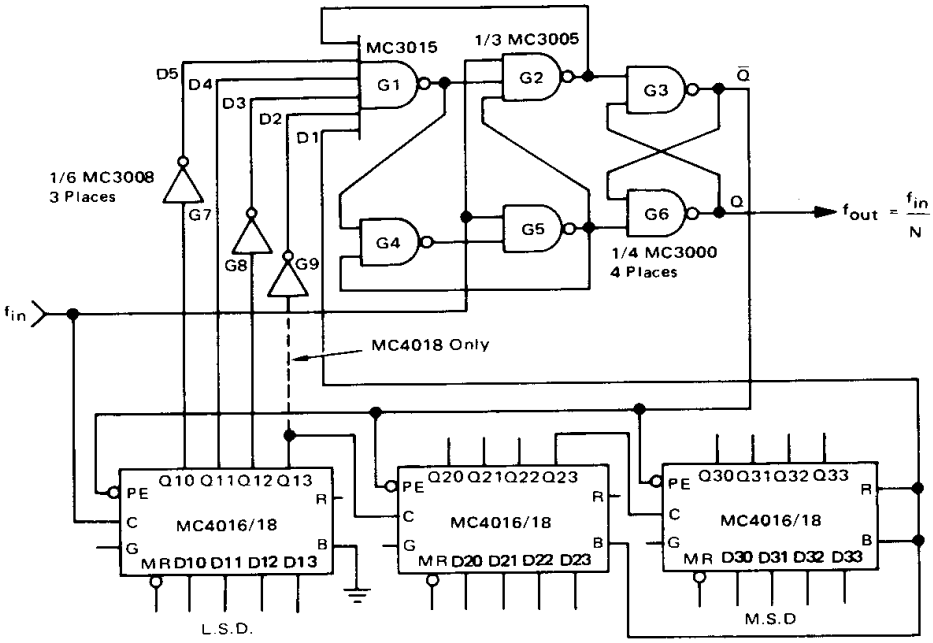
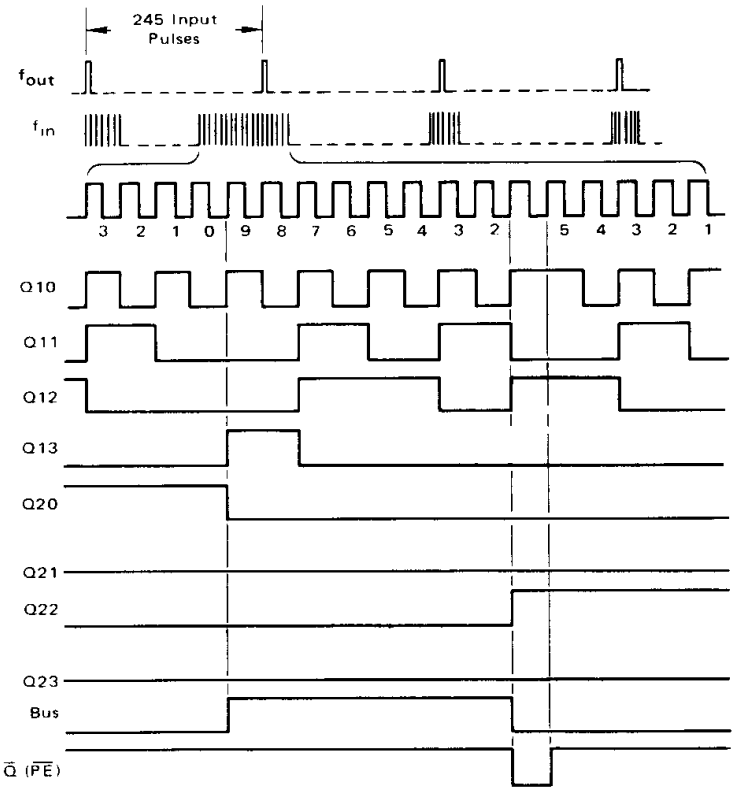
OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

FIGURE 3 – INCREASING OPERATING RANGE





OPERATING CHARACTERISTICS: MC4316/4016, MC4318/4018

Maximum operating frequency of the basic MC4016/4018 counter is limited by the time required for reprogramming at the end of each count down cycle. Operation can be extended to approximately 25 MHz by adding an "early decode" feature as shown in Figure 3. The appropriate connections for three stages are shown; however up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all Parallel Enables are connected to the $\overline{Q}$ output of a type D flip-flop formed by gates G1 through G6; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input to the flip-flop. Four additional data inputs are provided for decoding the "two" state of the least significant stage. Circuit operation is illustrated in the waveforms of Figure 3 where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 applied. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached. This condition causes the remaining D inputs to the flip-flop to be high. The next-to-last clock pulse of the cycle then triggers the flip-flop Q output high. $\overline{Q}$ simultaneously takes the parallel enable of all stages low, resetting the programmed data to the outputs. The next input pulse clocks Q (f_{out}) back to the zero state since the data inputs to the flip-flop are no longer all high. The positive output pulse is one input clock period in duration. Note that division by N equal to 1 or 2 is not available using this method.

OPERATING CHARACTERISTICS

MC4317/4017, MC4319/4019

The MC4317/4017 consists of a modulo 2 and a modulo 5 programmable counter. The MC4319/4019 contains two modulo 4 programmable counters. Both parts are implemented in the same manner as the MC4316/4016 and MC4318/4018, however in these devices the output of the appropriate flip-flop is disconnected from the input of the next flip-flop. This input is then brought out as the second clock input for the package (see logic diagrams on page 2 of this data sheet). The resistor existing on the MC4316/4016 and MC4318/4018 is eliminated on the MC4317/4017 and MC4319/4019 in order not to exceed 16 pins. Elimination of the resistor causes no problems because only one resistor is required per divider chain and these parts will normally be used with the MC4316/4016 and/or MC4318/4018. In applications where the parts are used alone, an external resistor is connected to the bus output.

To operate the MC4317/4017 as a modulo 2 programmable counter, the modulo 5 programmable counter must be disabled by programming it to zero (D1, D2, and D3 grounded). Likewise, to use the device as a modulo 5 programmable counter the modulo 2 counter must be disabled (D0 grounded). Operation of the MC4319/4019 is similar in that the modulo 4 counter not being used must be disabled by programming it to zero (D0 thru D1 grounded or D2 and D3 grounded).

When cascading packages for large divide ratios, the most significant Q output of the modulo counter being used provides the input for the next package and all bus outputs are tied together. This method of connection is the same as for the MC4316/4016 and MC4318/4018.

The MC4317/4017 and MC4319/4019 can be made to perform the same function as the MC4316/4016 and MC4318/4018, respectively, by externally connecting the last Q output of one counter to the clock input of the other counter and programming inputs in the normal manner.

APPLICATIONS INFORMATION

A typical system application for programmable counters is illustrated in the frequency synthesizer shown in Figure 4. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[1] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter.

In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 5. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where

FIGURE 4 — MTTL PHASE-LOCKED LOOP

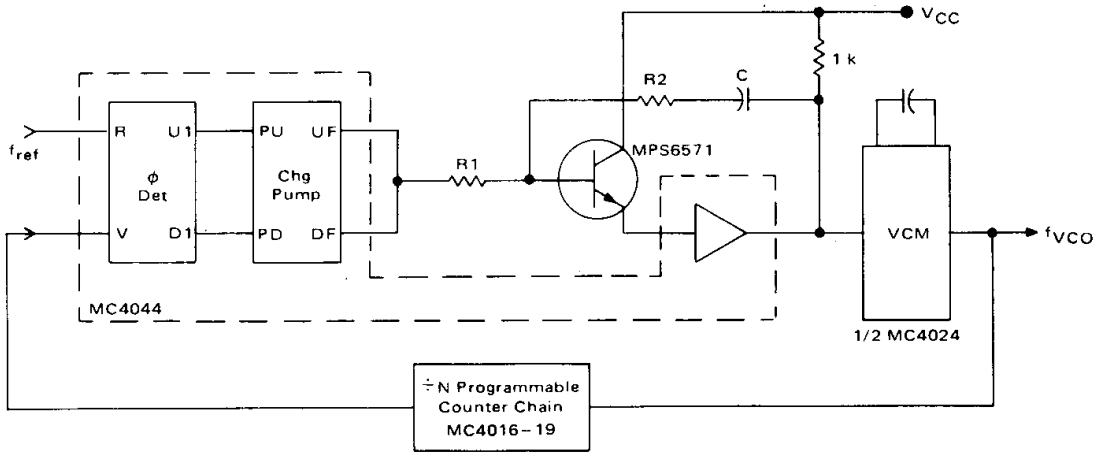
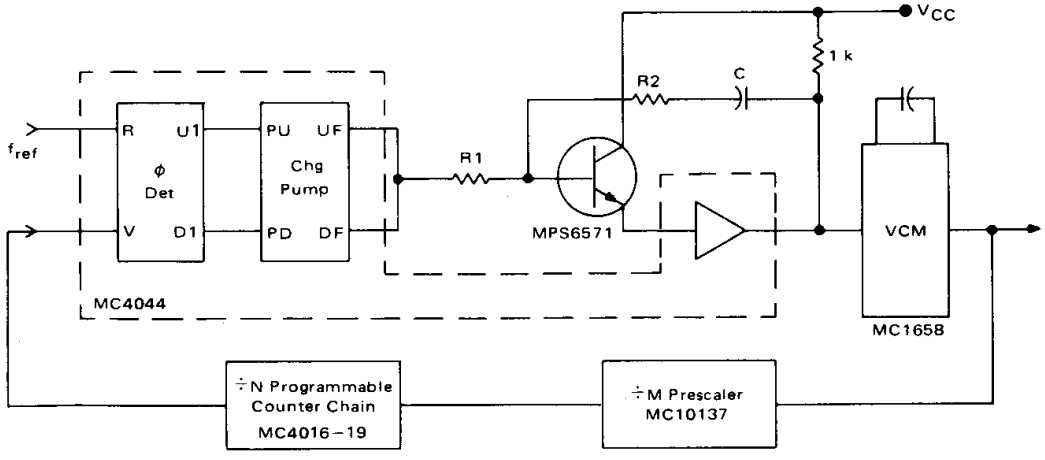
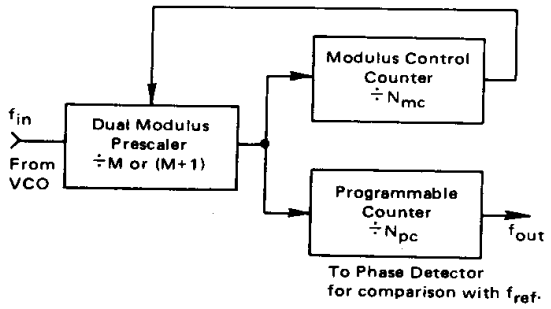


FIGURE 5 — MTTL-MECL PHASE-LOCKED LOOP



1 See Motorola Application Note AN-535 and the MC4344/4044 Data Sheet for detailed explanation of overall circuit operation.

FIGURE 6 — FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



the upper limit is established by the required channel spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 5, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 6.[2] It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M + 1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. For this configuration,

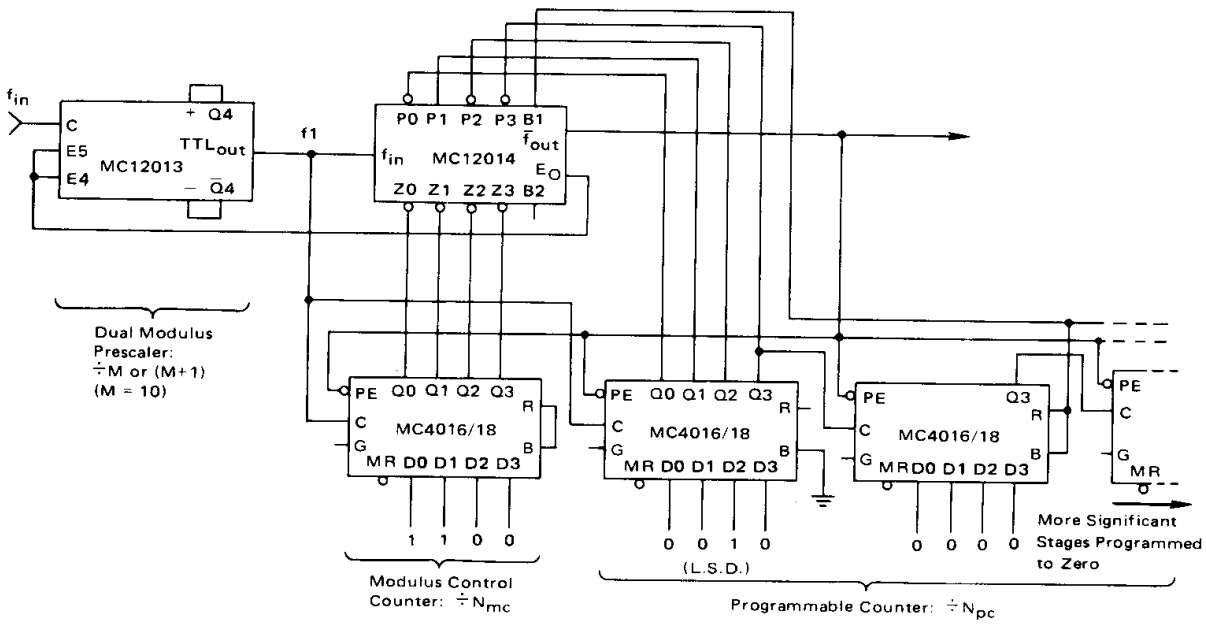
$$f_{out} = \frac{f_{in}}{MN_{pc} + N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 7. The MC12013 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 7. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain.

A specific example of this technique is shown in Figure 8. There the feedback divider circuitry required for generating frequencies between 144 MHz and 178 MHz with 30 kHz channel spacing is shown.[2]

FIGURE 7 — FREQUENCY DIVISION: $f_O = f_{in}/MN_{pc} + N_{mc}$



2. This application is discussed in greater detail in the MC12014 Counter Control Logic data sheet.

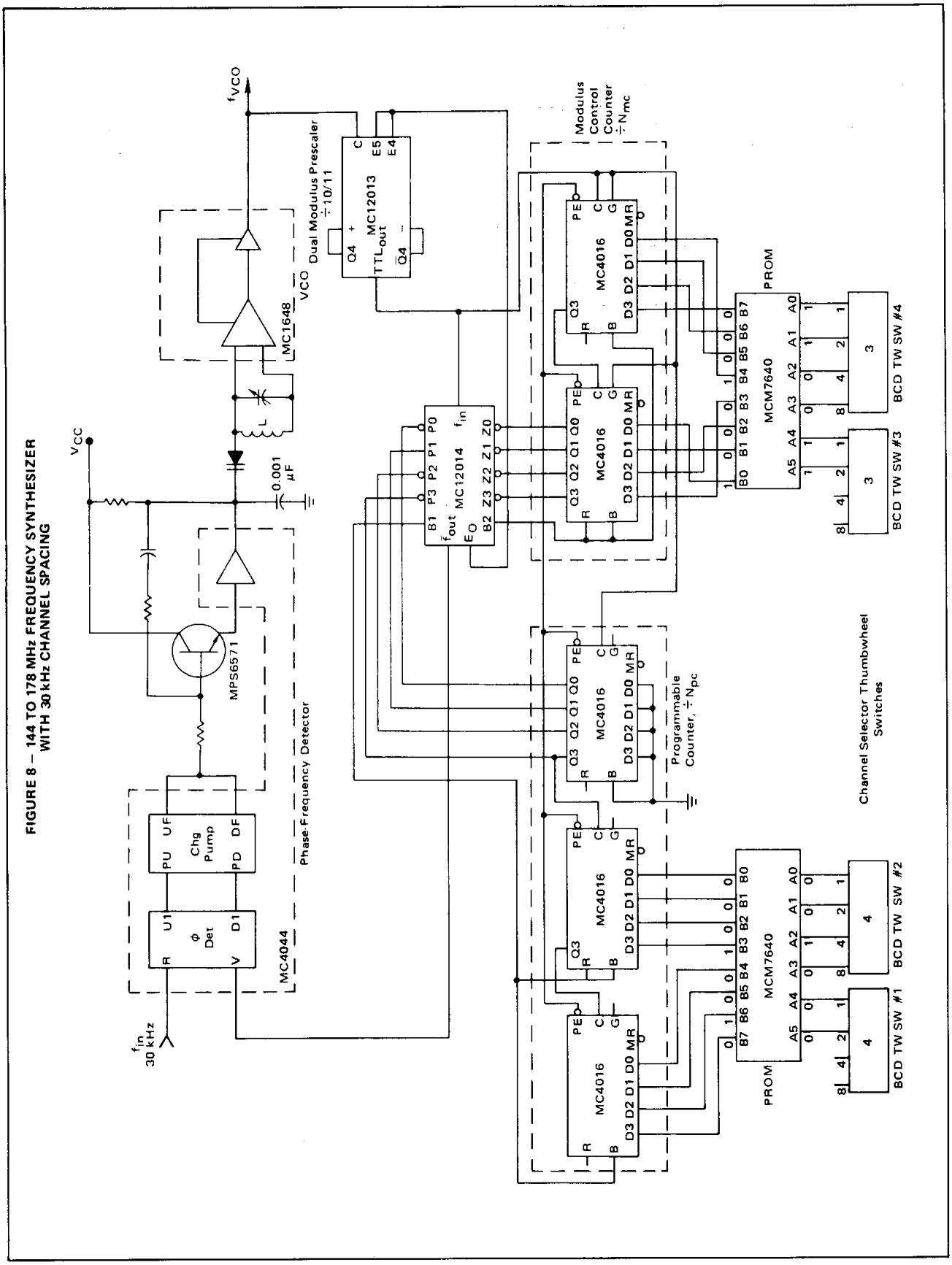


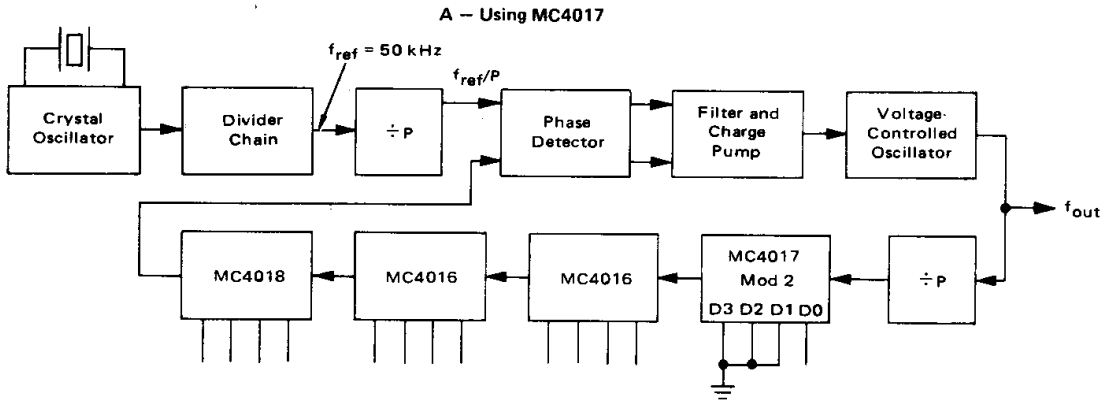
FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

Figure 9 shows a frequency synthesizer system for the aircraft band of 108 to 136 MHz with a channel spacing of 50 kHz. The use of the MC4017 as a modulo 2 programmable counter is shown in Figure 9A, while Figure 9B shows the same system implemented using the MC4016. For a system of this type it is desirable to use direct-reading thumbwheel switches for channel selection. To implement this system with these constraints, it is necessary to calculate the required reference frequency (f_{ref}). Using the equations in Figure 9A, the required reference is 50 kHz and N4 must be programmed to 0 and 1. Figure 9B requires a reference frequency of 10 kHz and N4 must be programmed to only 0 and 5.

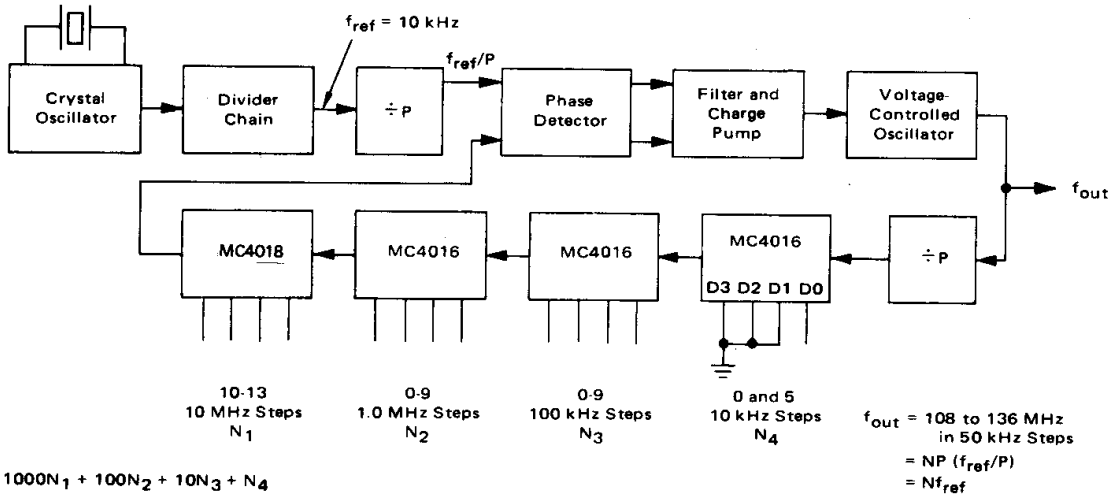
For any phase-locked loop system it is desirable to maintain as high a reference frequency as possible while meeting the system requirements. The higher the reference frequency, the higher the number of sampling pulses received by the phase detector per unit time. This results in (1) easier filtering of the control voltage, (2) faster lock-up time, and (3) less noise in the output spectrum. The higher reference frequency is also desirable because the reference frequency appears as sidebands on the output frequency and the farther the sidebands are away from the output the better the system. Another advantage of the higher reference frequency is the smaller divide ratio required in the programmable counter chain. This is advantageous when calculating realizable resistors for the filter. For these reasons, the system using the MC4017 is superior to the one using the MC4016.

FIGURE 9 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 50 kHz CHANNEL SPACING

A — Using MC4017



B — Using MC4016

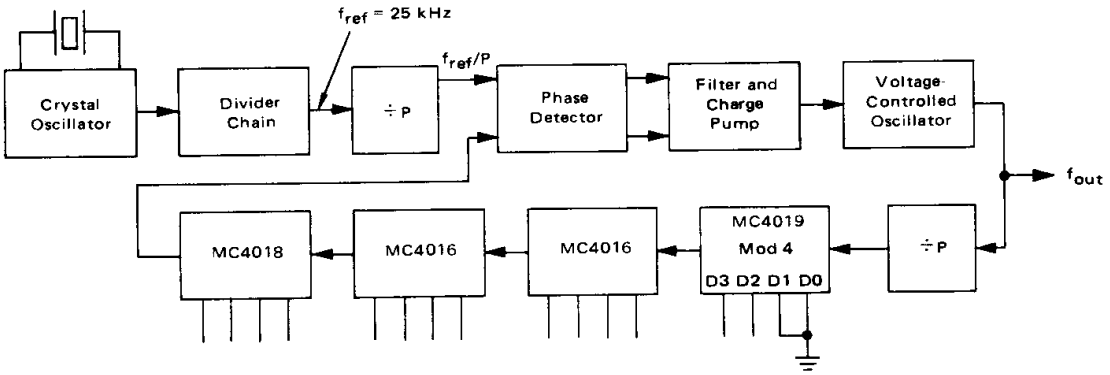


6

Figure 10 shows the implementation of the aircraft band synthesizer with 25 kHz channel spacing (the 25 kHz spacing has been proposed to the FCC). The system is implemented in Figure 10A using the MC4019, and has a reference frequency of 25 kHz. Figure 10B shows the system using an MC4018 as the first counter, and has a reference frequency of 6.25 kHz to obtain the direct programming.

FIGURE 10 — 108 TO 136 MHz FREQUENCY SYNTHESIZER WITH 25 kHz CHANNEL SPACING

A — Using MC4019



10-13
10 MHz Steps
N_1

0-9
1.0 MHz Steps
N_2

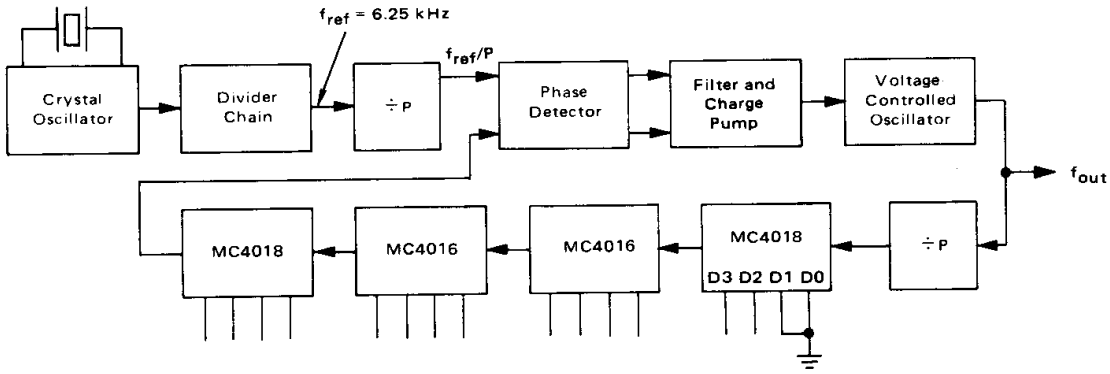
0-9
100 kHz Steps
N_3

0-4
25 kHz Steps
N_4

f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

$N = 400N_1 + 40N_2 + 4N_3 + N_4$

B — Using MC4018



10 13
6.25 MHz Steps
N_1

0 9
625 kHz Steps
N_2

0 9
62.5 kHz Steps
N_3

0,4,8,12
6.25 kHz Steps
N_4

f_{out} = 108 to 136 MHz in 25 kHz Steps
= NP (f_{ref}/P)
= Nf_{ref}

$N = 1600N_1 + 160N_2 + 16N_3 + N_4$

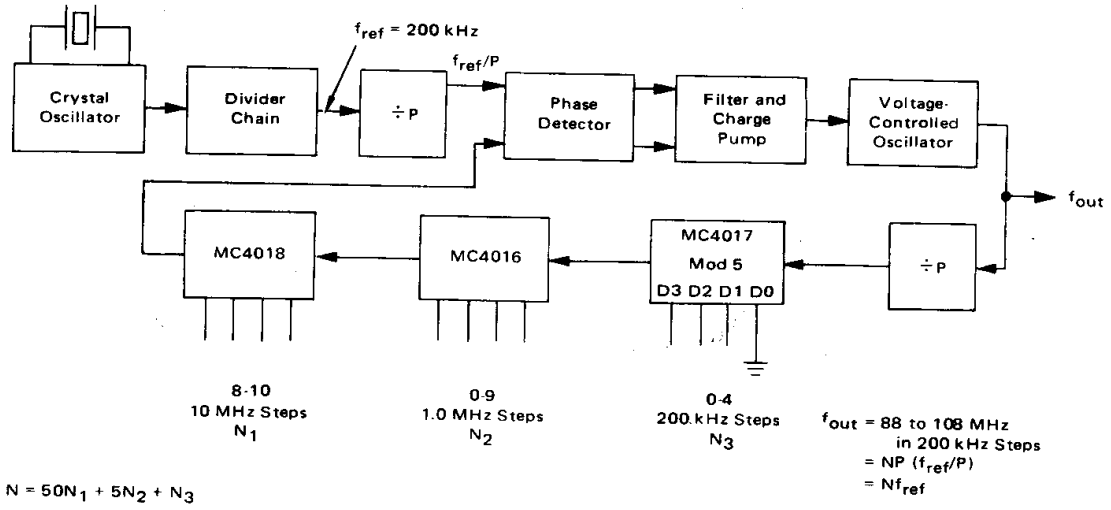
6

Figures 11A and 11B show the FM band implemented with MC4017 (used as a modulo 5 counter) and MC4016, respectively. The first system has a 200 kHz reference frequency, and the second system has a 100 kHz reference frequency. These systems using the MC4017/19 offer the same advantages over the MC4016/18 as with the aircraft band systems.

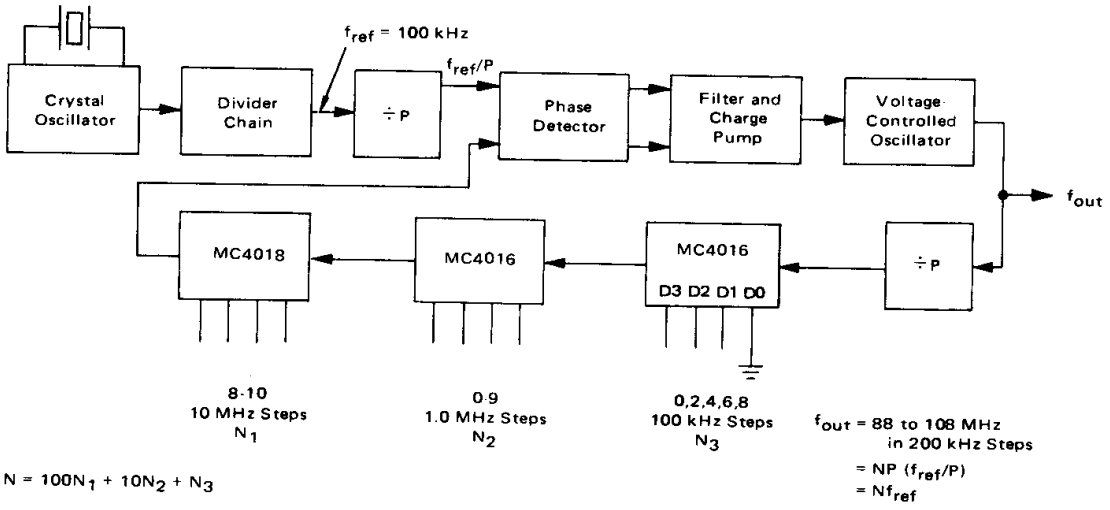
These examples illustrate the desirability of the MC4317/4017 for phase-locked loop applications where the channel spacing is 2×10^n Hz when used as a modulo 5 programmable counter, and 5×10^n Hz when used as a modulo 2 programmable counter. The MC4319/4019 is for applications with a channel spacing of 2.5×10^n Hz. The MC4316/4016 covers phase-locked loop applications where the channel spacing is 1×10^n Hz. The MC4318/4018 is used when the most significant digit is between 9 and 15.

FIGURE 11 — 88 TO 108 MHz FREQUENCY SYNTHESIZER WITH 200 kHz CHANNEL SPACING

A — Using MC4017



B — Using MC4016

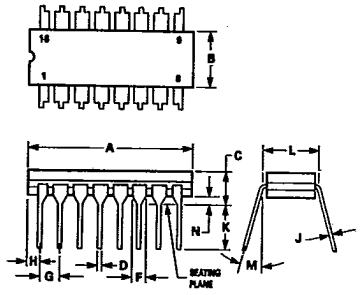


6

PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

L SUFFIX
CERAMIC PACKAGE
CASE 620-09

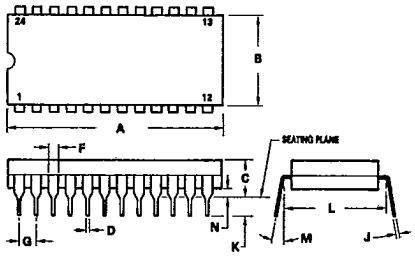


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

L SUFFIX
CERAMIC PACKAGE
CASE 623-05

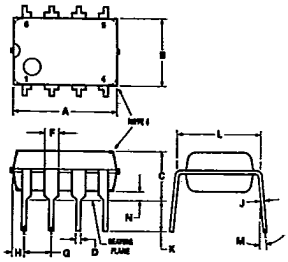
(LW SUFFIX FOR MC10H181 ONLY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

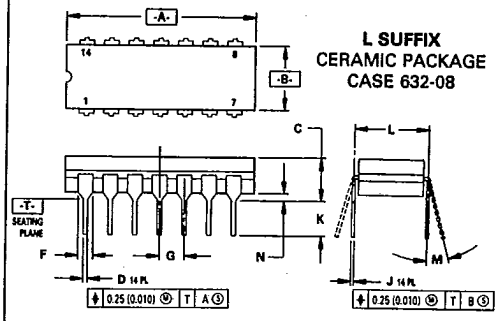
P SUFFIX
PLASTIC PACKAGE
CASE 626-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE: ⌖ 0.13 (0.005) M T A S B S
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

L SUFFIX
CERAMIC PACKAGE
CASE 632-08

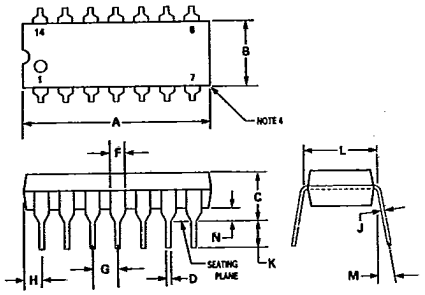


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.173
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

PACKAGE OUTLINE DIMENSIONS (continued)

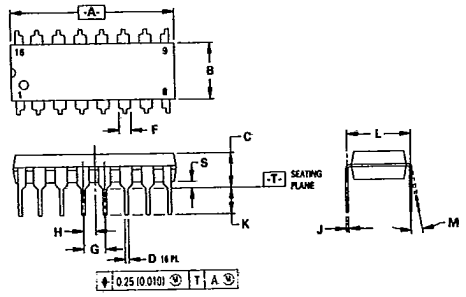
P SUFFIX
PLASTIC PACKAGE
CASE 646-06



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

P SUFFIX
PLASTIC PACKAGE
CASE 648-08

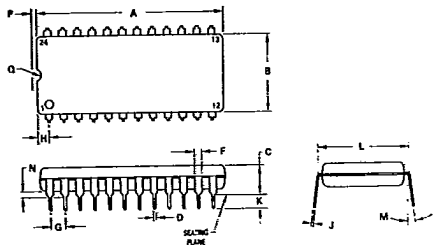


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

P SUFFIX
PLASTIC PACKAGE
CASE 649-03

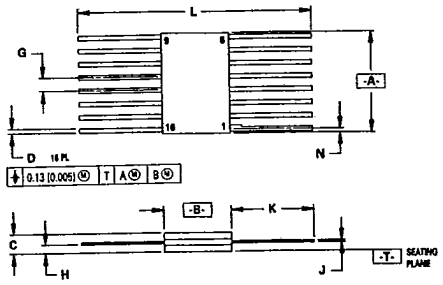
(PW SUFFIX
FOR MC10H181
ONLY)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

F SUFFIX
CERAMIC PACKAGE
CASE 650-05

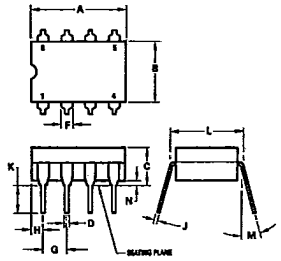


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MENISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

PACKAGE OUTLINE DIMENSIONS (continued)

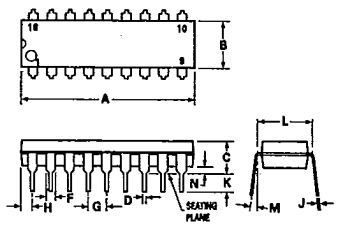
L SUFFIX
CERAMIC PACKAGE
CASE 693-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

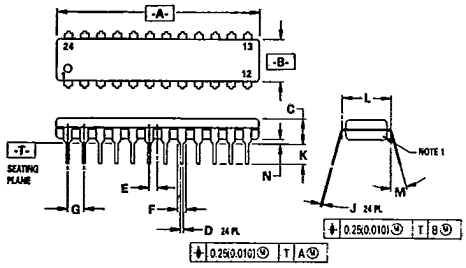
P SUFFIX
PLASTIC PACKAGE
CASE 707-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

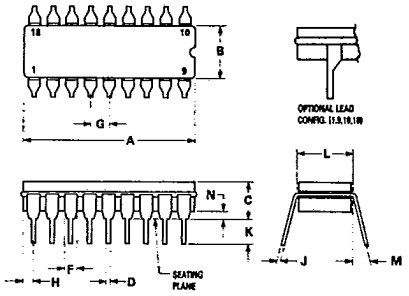
P SUFFIX
PLASTIC PACKAGE
CASE 724-03



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

L SUFFIX
CERAMIC PACKAGE
CASE 726-04

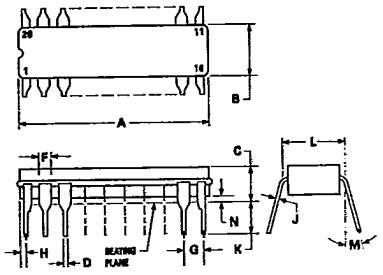


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

PACKAGE OUTLINE DIMENSIONS (continued)

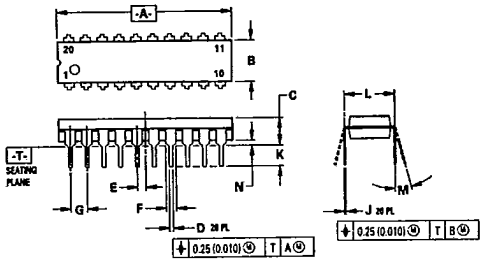
L SUFFIX
CERAMIC PACKAGE
CASE 732-03



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

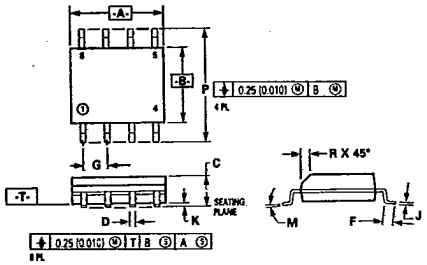
P SUFFIX
PLASTIC PACKAGE
CASE 738-03



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

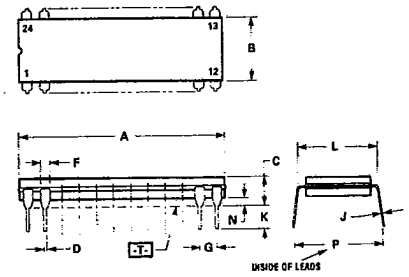
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-03



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

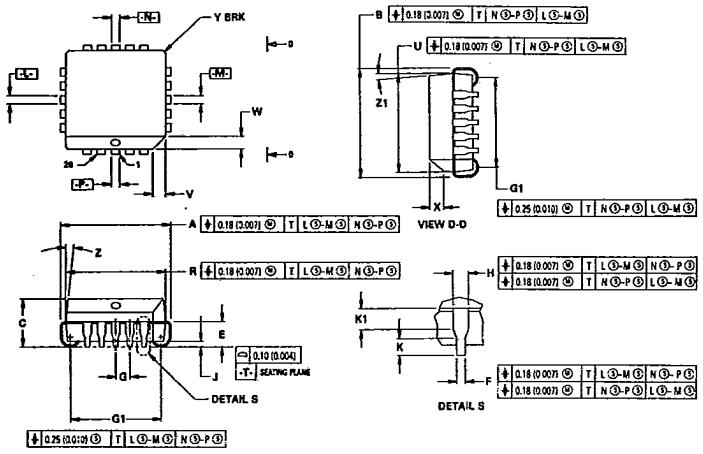
NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

L SUFFIX
CERAMIC PACKAGE
CASE 758-01



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
P	9.14	10.16	0.360	0.400

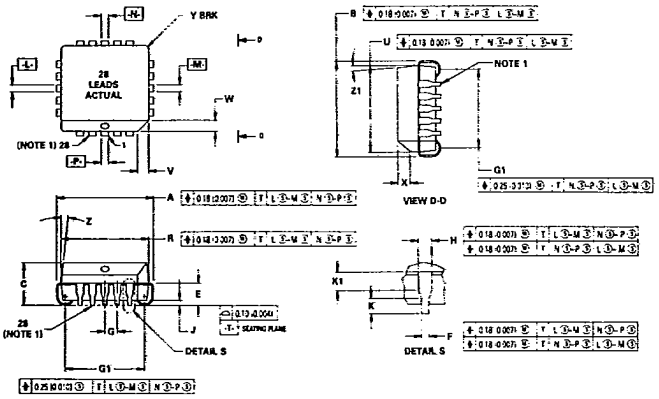
NOTES:
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: 24 PLACES
3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
PLASTIC PACKAGE
CASE 775-02



NOTES:
1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

MECL Logic Surface Mount

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

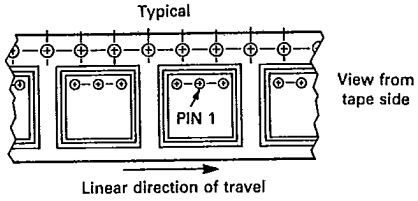
TAPE AND REEL

Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

ORDERING CODE	SHIPMENT METHOD
MC10100FN	Magazines (Rails)
MC10100FNR2	13 inch Tape and Reel
MC10H100FN	Magazines (Rails)
MC10H100FNR2	13 inch Tape and Reel
MC12015D	Magazines (Rails)
MC12015DR2	13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28