HD14017B

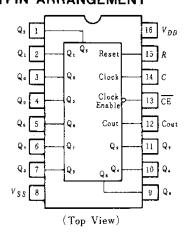
Decade Counter/Divider

The HD14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

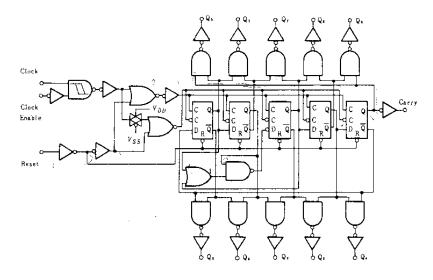
FEATURES

- Carry Output for Cascading 12MHz (typ) Operation @10V
- Divide-by-N Counting
- Ouiescent Current = 5nA/pkg typ. @5V
- Supply Voltage Range = 3 to 18V
- Capable of Driving One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B and MC14017B

■ PIN ARRANGEMENT



BLOGIC DIAGRAM



TRUTH TABLE

С	CE	R	Decode Output=n
0	×	0	n
×	1	0	n
×	×	1	Q_0
	0	0	n + 1
	×	0	n
×		0	n
1		0	n + 1

Notes) 1. × : Don't Care.

^{2.} If n<5 Carry="1", Otherwise~"0"

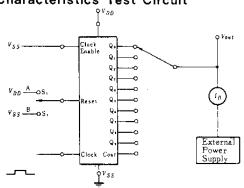
ELECTRICAL CHARACTERISTICS

Characteristic S			Test Conditions		-40°C		25°C			85°C	
Olas acteristic	J,	$V_{DD}(\mathbf{V})$	o(V)		max	min	typ	max	min	max	Unit
		5.0	$V_{in} = V_{DB}$ or 0	-	0.05	_	0	0.05	_	0.05	V V
	Vol	10		_	0.05	_	0	0.05		0.05	
Output Voltage		15			0.05	-	0	0.05		0.05	
Output voltage		5.0		4.95	_	4.95	5.0		4.95	-	
	Voн	10	$V_{in} = 0$ or V_{DD}	9.95	_	9.95	10	_	9.95	+	V
		15		14.95	_	14.95	15		14.95		
12		5.0	$V_{out} = 4.5 \text{ or } 0.5 \text{V}$	-	1.5	_	2.25	1.5	_	1.5	
	VIL	10	Vout = 9.0 or 1.0V	i	3.0	-	4.50	3.0		3.0	v
Input Voltage		15	Vout = 13.5 or 1.5V	-	4.0	_	6.75	4.0		4.0	
input voitage		5.0	$V_{out} = 0.5 \text{ or } 4.5 \text{V}$	3.5	_	3.5	2.75	_	3.5	_	v
	VIH	10	$V_{out} = 1.0 \text{ or } 9.0 \text{V}$	7.0	_	7.0	5.50	-	7.0		
		• 15	$V_{out} = 1.5 \text{ or } 13.5 \text{V}^{-1}$	11.0		11.0	8.25		11.0	_	
		5.0	$V_{OH} = 2.5 \mathrm{V}$	-1.0	_	-0.8	-1.7		-0.6	-	
	Іон	5.0	$V_{OH} = 4.6 \mathrm{V}$	-0.2		-0.16	-0.36	-	-0.12	_	mA
	10н	10	$V_{OH} = 9.5 \text{ V}$	-0.5	_	-0.4	-0.9		-0.3	_	
Output Drive Current		15	$V_{OH} = 13.5 \text{ V}$	-1.4	-	-1.2	-3.5	_	-1.0	_	
		5.0	$V_{OL} = 0.4 \text{ V}$	0.52		0.44	0.88	-	0.36	-	m A
	IoL	10	$V_{OL} = 0.5 \mathrm{V}$	1.3		1.1	2.25		0.9	_	
		15	$V_{OL} = 1.5 \mathrm{V}$	3.6	_	3.0	8.8	_	2.4		
Input Current	Ii.	15			±0.3	_	±0,00001	±0.3	_	±1.0	μΑ
Input Capacitance	Cin	-	$V_{in} = 0$			_	5.0	7.5	_		pF
Quiescent Current		5.0	7. (1.)	_	20	_	0.005	20		150	μА
	I_{DD}	10	Zero Signal, per Package		40	_	0.010	40	-	300	
		15		_	80	_	0.015	80	_	600	
		5.0	Dynamie $+I_{DD}$,	-	-		0.27	-			μΑ
Total Supply Current*	$I\tau$	10	$C_{\iota} = 50 \mathrm{pF}, f = 1 \mathrm{kHz},$	_			0.55	_	_		
		15	per Gate	_	_		0.83	_	_		

^{*} To calculate total supply current at frequency other than 1kHz. $@V_{DD} = 5.0V \quad I_T = (0.27\mu\text{A}/k\text{Hz})f + I_{DD} \qquad @V_{DD} = 10 V \quad I_T = (0.55\mu\text{A}/k\text{Hz})f + I_{DD} \qquad @V_{DD} = 15 V \quad I_T = (0.83\mu\text{A}/k\text{Hz})f + I_{DD}$

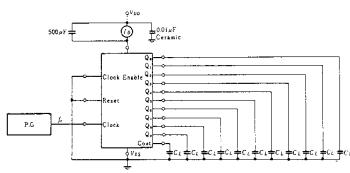
IDC CHARACTERISTIC TEST CIRCUIT

 Typical Output Source and Output Sink Characteristics Test Circuit



	lot	Іон
DECODE OUTPUTS	(S1- A)	Clock to desired outputs (S1 to B)
Cerry	Clock5~9(S1~B)	S 1 - A
Vcs=	Vaa	- Voo
Vas ==	Vout	$V_{res} - V_{DD}$

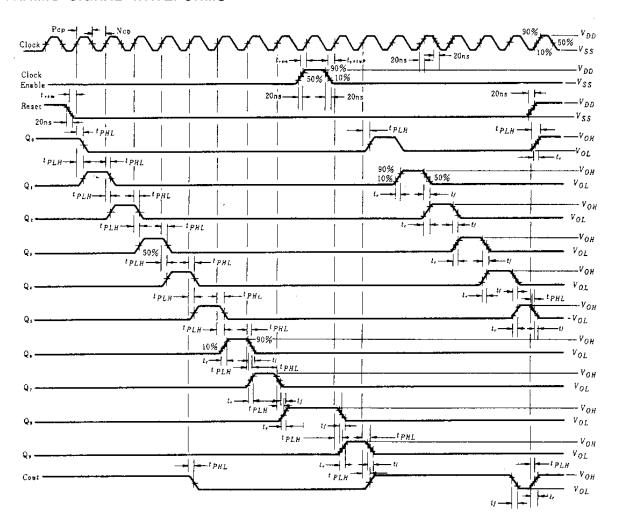
POWER DISSIPATION TEST CIRCUIT



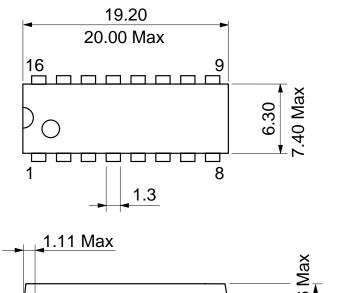
ESWITCHING CHARACTERISTICS $(C_L = 50 \text{pF}, Ta = 25^{\circ}\text{C})$

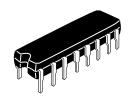
Characteris	tic	Symbol	$V_{DD}(V)$	min	typ	max	Unit
Output Rise Time			5.0	_	180	400	
		tr	10	_	90	200	ns
			15	_	65	160	
		•	5.0		100	200	
Output Fall Time		t_f	10		50	100	ns
			. 15	_	37	80	
			- 5.0	_	500	1000	
·*	Reset-to-		10	_	230	460	
	Decode		15	-	140	350	
			5.0		400	800	
	Clock-to-	t_{PLH} ,	10	_	150	350	ns
	Cout	tphl	15	_	100	250	
Propagation Delay Time			5.0		500	1000	
• }	Clock-to-		10	_	230	460	
; ;	Decode		15	_	140	350	
		tPLH	5.0	<u>-</u>	400	800	
	Reset-to-		10	_	150	350	ns
)			15		100	250	
	-	PWc	5.0	250	100		
Clock Pulse Width			10	100	42		ns
	ļ		15	75	30	_	
		PRF	5.0	_	5.0	2.0	
Clock Pulse Frequency			10	_	12	5.0	MHz
Civen 1 disc 1 requestoy			15	<u> </u>	16	6.7	
Reset Pulse Width			5.0	500	200		
		PW_R	10	250	100		ns
			15	190	75	_	
Reset Removal Time		trem	5.0	750	300	_	•
			10	275	100		ns
			15	210	80	_	
Clock Pulse Rise and Fall Time			5.0			<u>:</u>	
		tr, tf	10				
			15				
		· · · · · · · · · · · · · · · · · · ·	5.0	700	175		······································
lock Enable Setup Time		tsetup	10	300	75		ns
I I I I I I I I I I I I I I I I I I I		626.00	15	225	52	 	114
			5.0	700	260		
lock Enable Removal Ti	me	ŧ rem	10	300	100		n e
Sider Limite Ivellova, 1 mo		L rem	15	225	70		ns

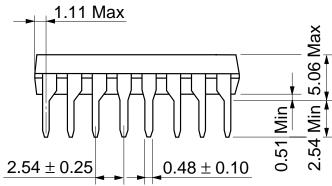
■ DYNAMIC SIGNAL WAVEFORMS

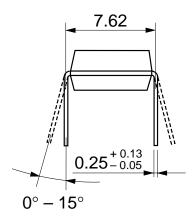


Unit: mm



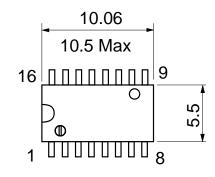


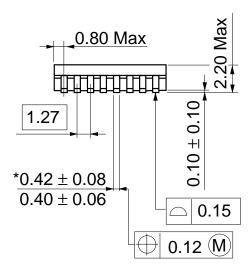




Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

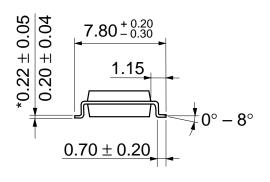
Unit: mm





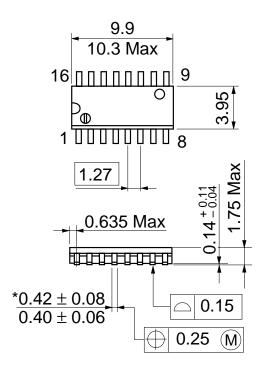
*Dimension including the plating thickness
Base material dimension



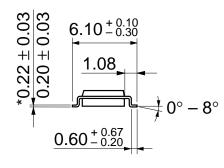


Hitachi Code	FP-16DA
JEDEC	
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm







*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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