OKI semiconductor

MSM5299B

DOT MATRIX LCD 80 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5299BGS is a dot matrix LCD's segment driver LSI which is fabricated by CMOS low power metal gate technology. This LSI consists of 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.

It receives the display data, which consists of 4-bit parallel, from the LCD controller LSI, then output the LCD driving waveform to the LCD'.

The MSM5299BGS has the power down function which enables the MSM5299BGS's power consumption low.

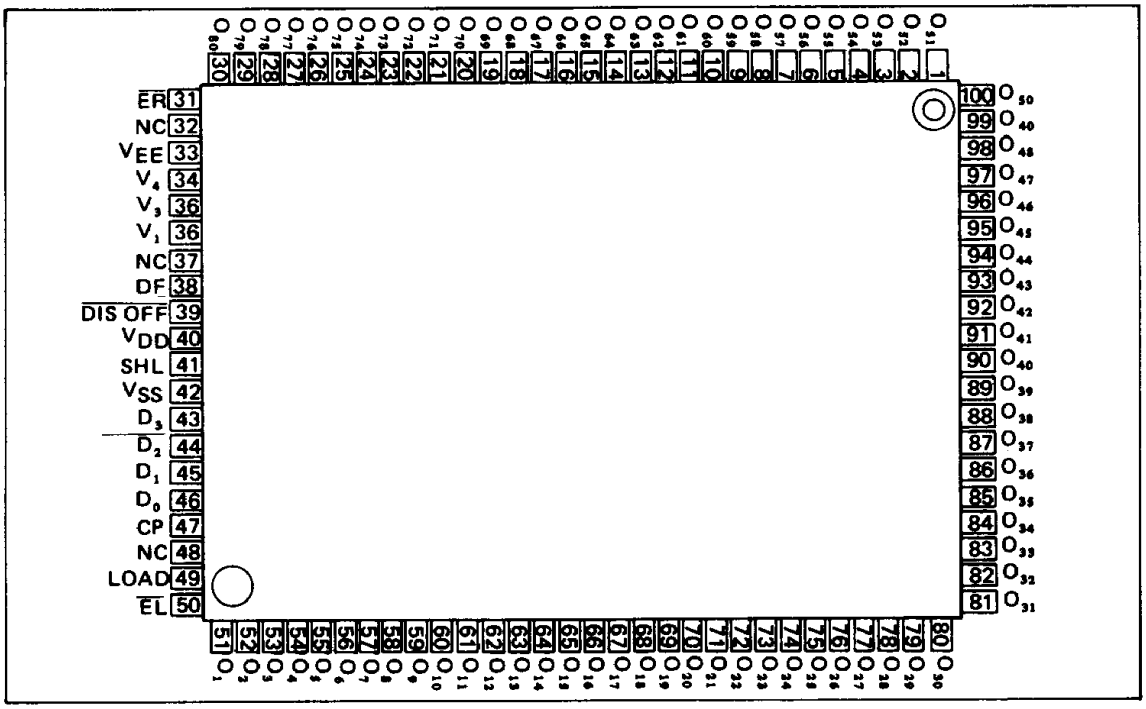
The MSM5299BGS can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

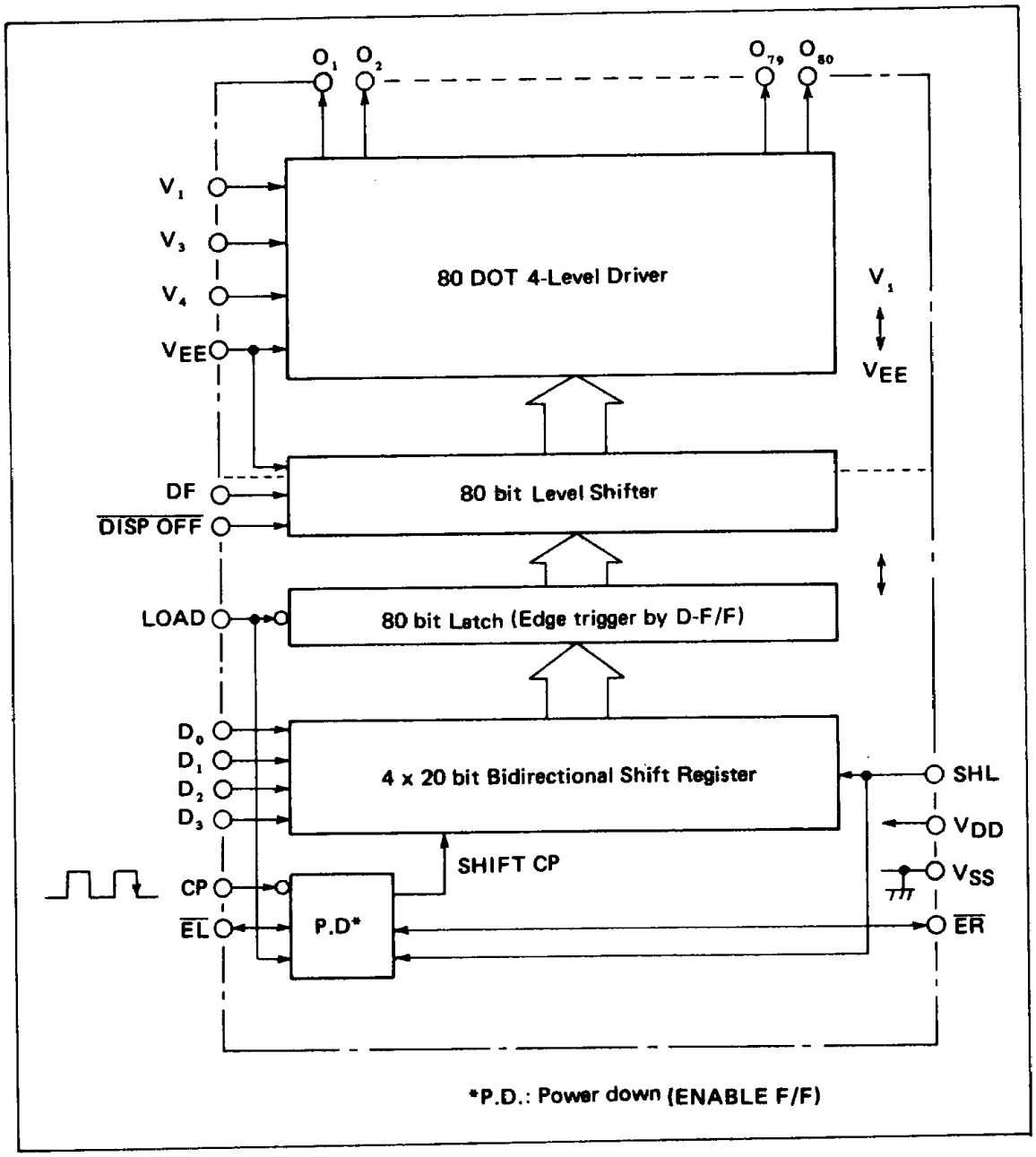
- Supply voltage: 4.5 ~ 5.5 V
- LCD driving voltage: 8 ~ 26 V
- Applicable LCD duty: 1/64 ~ 1/256
- LCD Output : 80
- Bias voltage can be supplied externally
- Power down function
- 4-bit parallel data processing
- Can be interfaced with the LCD controller LSI MSM6255GS
- 100 pin plastic QFP (QFP100-P-1420-K)
- 100 pin -VI plastic QFP (QFP100-P-1420-VIK)

PIN CONFIGURATION (TOP VIEW)

(Top view) 80 pin plastic QFP



BLOCK DIAGRAM



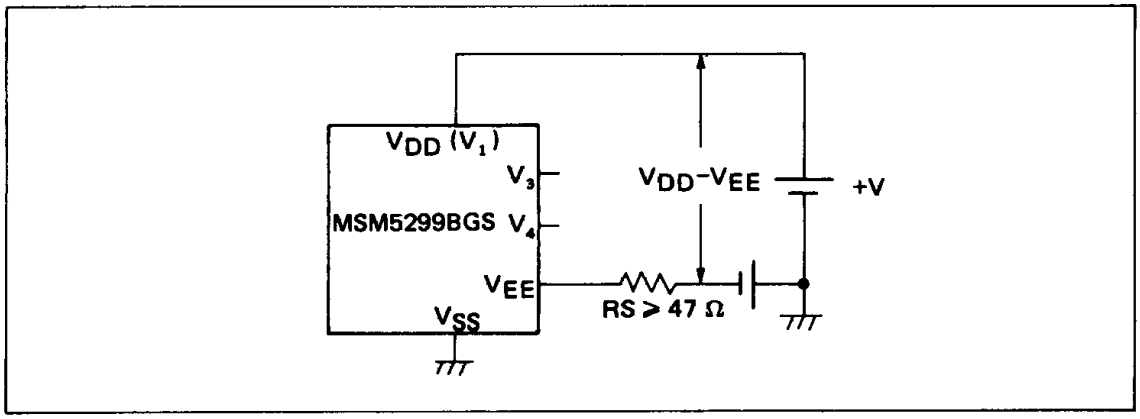
TRUTH TABLE

DF	Latched data	$\overline{\text{disp off}}$	Display data output level ($O_1 \sim O_{80}$)
L	L	H	V_3
L	H	H	V_1
H	L	H	V_4
H	H	H	V_{EE}
X	X	L	V_1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage (1)	V_{DD}	Ta = 25 °C	–0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$ *1	Ta = 25 °C	0 ~ 27	V
	$V_{DD} - V_{EE}$ *1 *2	Ta = 25 °C	0 ~ 30	V
Input voltage	V_I	Ta = 25 °C	–0.3 ~ V_{DD} + 0.3	V
Storage temperature	Tstg	–	–55 ~ + 150	°C

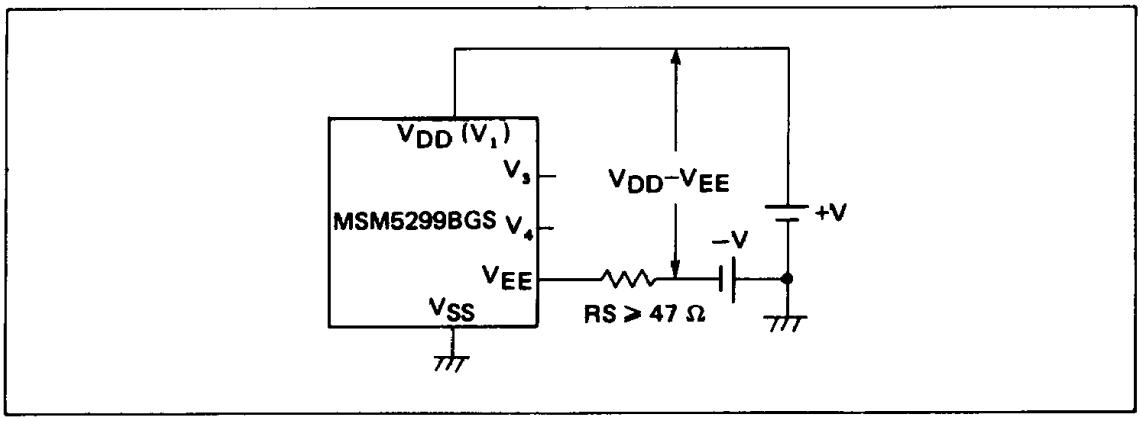
*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_I \leq V_{DD}$
*2 In case of connecting Resister (RS ≥ 47 Ω) at V_{EE} pin



OPERATING RANGE

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage (1)	V_{DD}	–	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$ *1	–	8 ~ 26	V
	$V_{DD} - V_{EE}$ *1 *2	–	8 ~ 28	V
Operating temperature	T_{OP}	–	–20 ~ +85	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_I \leq V_{DD}$
*2 In case of connecting resister (PS ≥ 47 Ω) at V_{EE} pin



DC CHARACTERISTICS

(V_{DD} = 5 V ± 10%, Ta = −20 ~ +85 °C)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}*1	—	0.8 V_{DD}	—	—	V
"L" Input voltage	V_{IL}*1	—	—	—	0.2 V_{DD}	V
"H" Input current	I_{IH}*1	$V_{IH} = V_{DD}$ V_{DD} = 5.5 V	—	—	1	μA
"L" Input current	I_{IL}*1	V_{IL} = 0 V V_{DD} = 5.5 V	—	—	−1	μA
"H" Output voltage	V_{OH}*2	I_O = −0.2 mA V_{DD} = 4.5 V	V_{DD}− 0.4	—	—	V
"L" Output voltage	V_{OL}*2	I_O = 0.2 mA V_{DD} = 4.5 V	—	—	0.4	V
ON resistance	R_{ON}*4	$V_{DD} - V_{EE}$ = 23 V *3 $\lvert V_N - V_O \rvert$ = 0.25 V V_{DD} = 4.5 V	—	1	2	kΩ
Stand-by current consumption	I_{DDSBY}	CP = 1 MHz V_{DD} = 5.5 V $V_{DD} - V_{EE}$ = 26 V, No load*5	—	—	200	μA
Current consumption (1)	I_{DD1}	CP = 1 MHz V_{DD} = 5.5 V $V_{DD} - V_{EE}$ = 26 V, No load*6	—	—	4	mA
Current consumption (2)	I_V	CP = 1 MHz V_{DD} = 5.5 V $V_{DD} - V_{EE}$ = 26 V, No load*7	—	—	±100	μA
Input capacitance	C_I	f = 1 MHz	—	5	—	pF

*1 Applicable to LOAD, CP, D_0 ~ D_3, $\overline{EL}$, $\overline{ER}$, SHL, DF, $\overline{DISP\ OFF}$, terminals

*2 Applicable to $\overline{EL}$, $\overline{ER}$ terminals.

*3 $VN = V_{DD} \sim V_{EE}$ $V_3 = \frac{13}{15}(V_{DD} - V_{EE})$, $V_2 = \frac{2}{15}(V_{DD} - V_{EE})$, $V_{DD} = V_1$

*4 Applicable to O_1 ~ O_{80} terminals.

*5 Display data 1010 — DF = 40 Hz, Current from V_{DD} to V_{SS} when the display data is not processing.

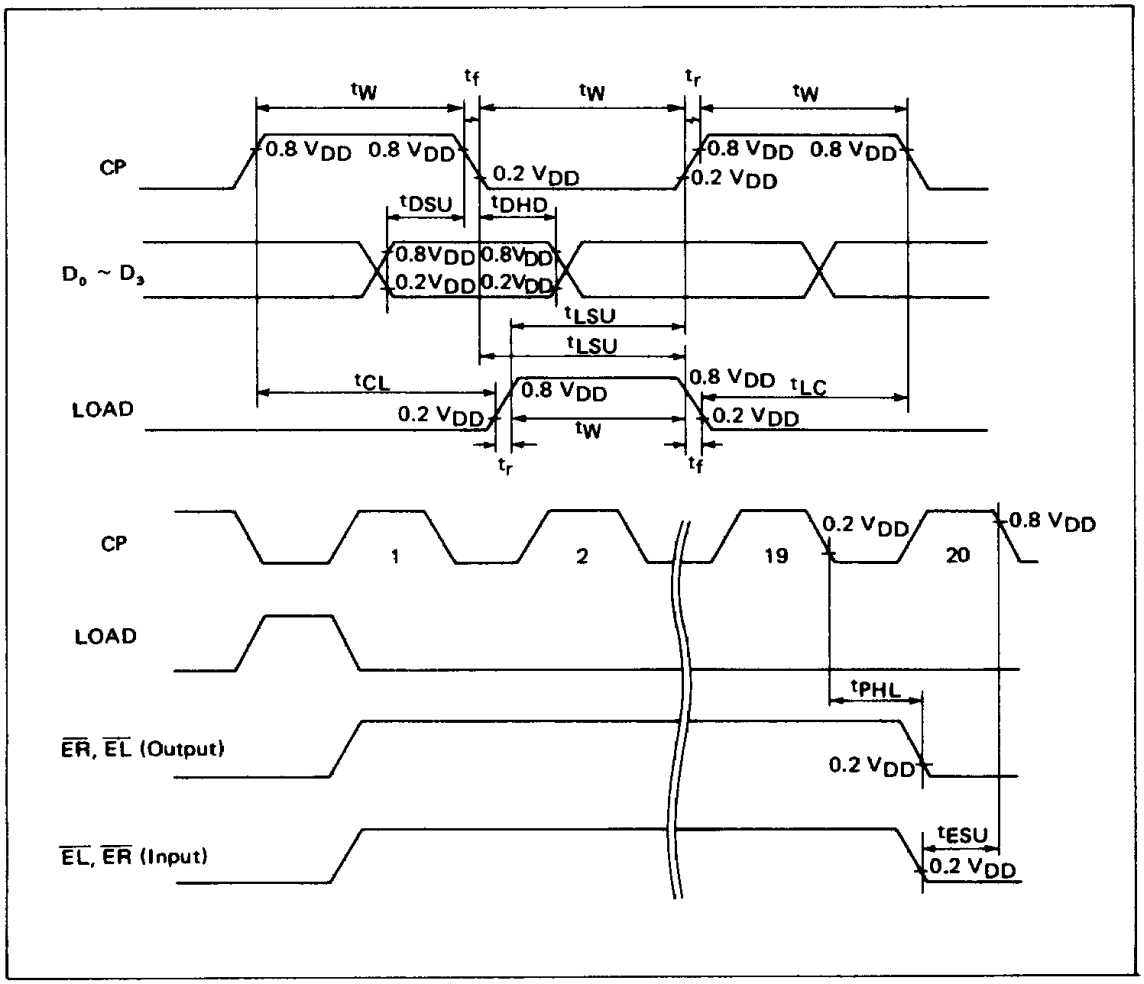
*6 Display data 1010 — DF = 40 Hz, Current from V_{DD} to V_{SS} when the display data is processing.

*7 Display data 1010 — DF = 40 Hz, Current on V_1, V_3, V_4 and V_{EE} terminals.

SWITCHING CHARACTERISTICS

(V_{DD} = 5 V ± 10% Ta = −20 ~ +85 °C CL = 15 pF)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
MAX. clock frequency	f_{CP}	DUTY = 50%	3.0	–	–	MHz
Clock Load pulse width	t_W		125	–	–	ns
Clock pulse Rising/Falling time	t_r, t_f		–	–	50	ns
Data set-up time	t_{DSU}		100	–	–	ns
Data hold time	t_{DHD}		100	–	–	ns
Clock → Load time	t_{CL}		63	–	–	ns
Load set-up time	t_{LSU}		125	–	–	ns
Load → clock time	t_{LC}		63	–	–	ns
Propagation delay time	t_{PHL}	$\overline{ER}$ Output / $\overline{EL}$ Output	–	–	270 / 230	ns
$\overline{ER}$, $\overline{EL}$ set-up time	t_{ESU}	$\overline{ER}$ Input / $\overline{EL}$ Input	100 / 60	–	–	ns



PIN DESCRIPTION

- **$\overline{ER}$, $\overline{EL}$**

Pin	Input/Output	SHL	Description
$\overline{ER}$	Input	L	Input pin to ENABLE F/F of MSM5299BGS.
$\overline{EL}$	Output		Output pin of ENABLE F/F. $\overline{EL}$ is connected to next MSM5299BGS's $\overline{ER}$ when MSM5299BGSs are connected in series (cascade connection).
$\overline{EL}$	Input	H	Input pin to ENABLE F/F of MSM5299BGS.
ER	Output		Output pin of ENABLE F/F. $\overline{ER}$ is connected to next MSM5299BGS's $\overline{EL}$ when MSM5299BGSs are connected in series (cascade connection).

- **$\overline{ER}$ and $\overline{EL}$ pins working as input pin**
  ENABLE F/F stops Display Data In at "H" level input. ENABLE F/F starts Display Data In at "L" level input.

- **$\overline{ER}$ and $\overline{EL}$ pins working as output pins**
  These pins are set to the "H" level immediately after ENABLE F/F is initialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the CP-pin, these output pins are then set to the "L" level. The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected.
  (For cascade connection, refer to the application circuit drawing.)

- **CP**
  Clock pulse input pin for the 4-bit parallel shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.

- **SHL**
  $\overline{ER}$ and $\overline{EL}$ can be used as either input pin or output pin according to the H/L condition of SHL. The shifting direction of each data, $D_0 \sim D_3$, the Input/Output condition of $\overline{ER}$ and $\overline{EL}$ and the H/L condition of SHL are described in the table below.

SHL	$\overline{ER}$	$\overline{EL}$	Shifting direction
L	Input	Output	$D_0 \rightarrow O_1 \rightarrow O_5 \cdots\cdots\rightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6 \cdots\cdots\rightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7 \cdots\cdots\rightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8 \cdots\cdots\rightarrow O_{80}$
H	Output	Input	$D_0 \rightarrow O_{80} \rightarrow O_{76} \cdots\cdots\rightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75} \cdots\cdots\rightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74} \cdots\cdots\rightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73} \cdots\cdots\rightarrow O_1$ ↑ end data ↑ start data

- **D_0, D_1, D_2, D_3**
  Display data input pins for 4-bit parallel shift register and it is input synchronized with the clock pulse. The combination of $D_0 \sim D_3$ level, DF signal, display data output level and the display on the LCD panel is described on the table below.

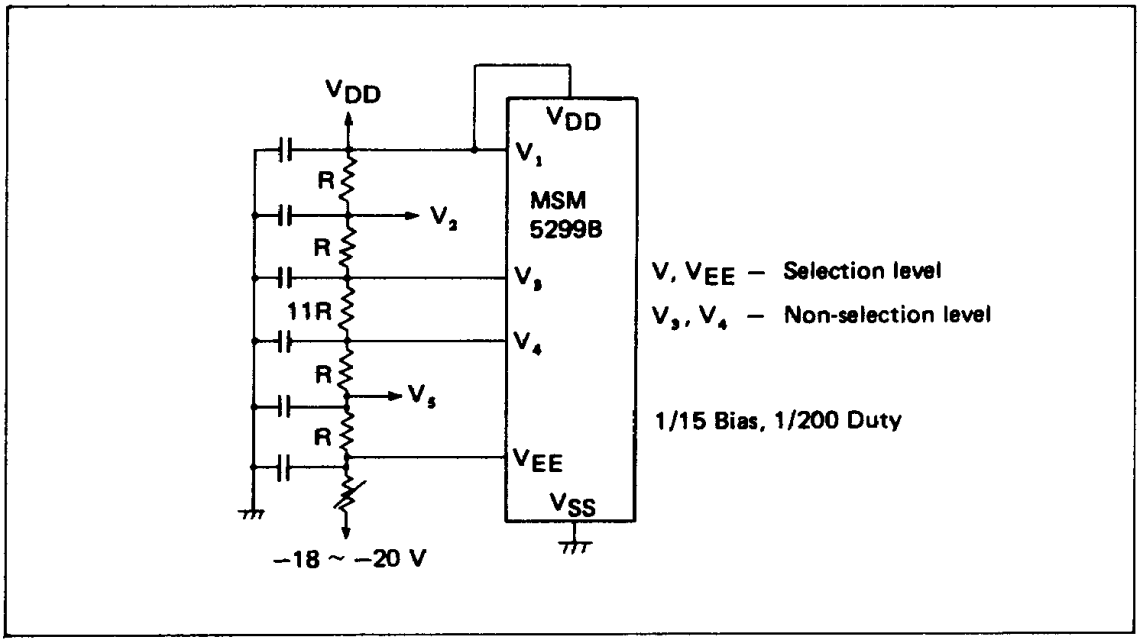
$D_0 \sim D_3$	DF	Display data output level	Display on the LCD
L	L	V_3	OFF
H	L	V_1	ON
L	H	V_4	OFF
H	H	V_{EE}	ON

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  LOAD pulse "H" level initializes ENABLE F/F.

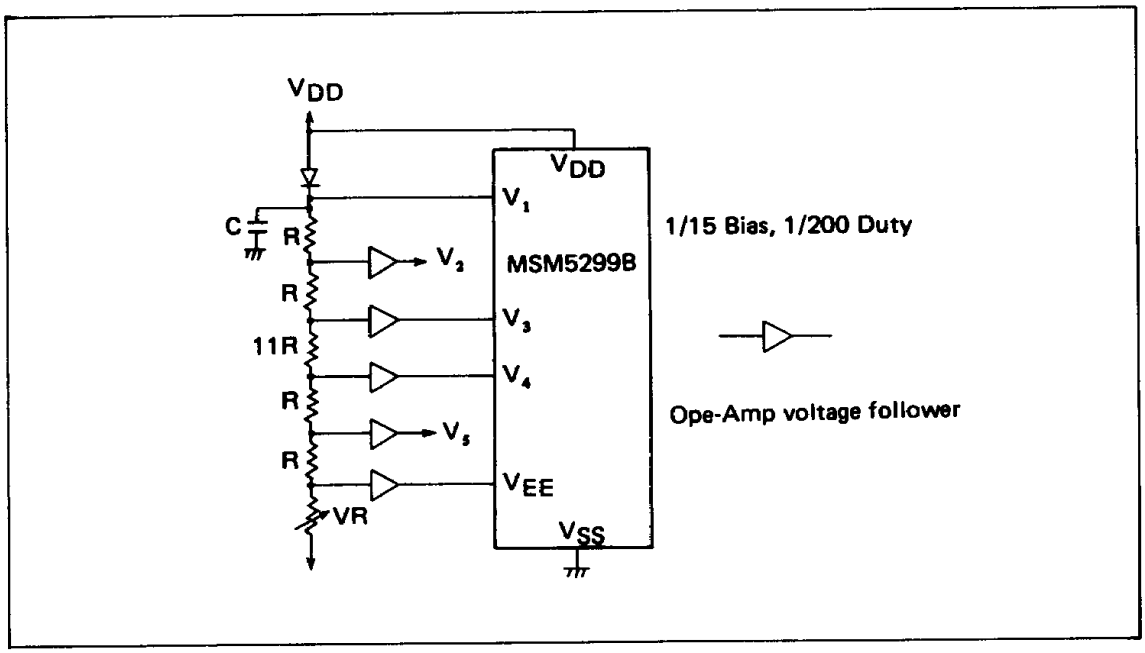
- **DF**
  Alternate signal input pin for LCD driving. Frame inversion signal is input to this terminal.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5 V. V_{SS} is a ground pin (V_{SS} = OV)

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. The figure below shows the case when bias voltage, which determines the LCD driving voltage, is supplied from the external source. V_1 is not necessarily connected with V_{DD}.



The figure below shows the case when the bias voltage is supplied by using Ope-Amps, which enables the bias source low impedance and low power consumption.

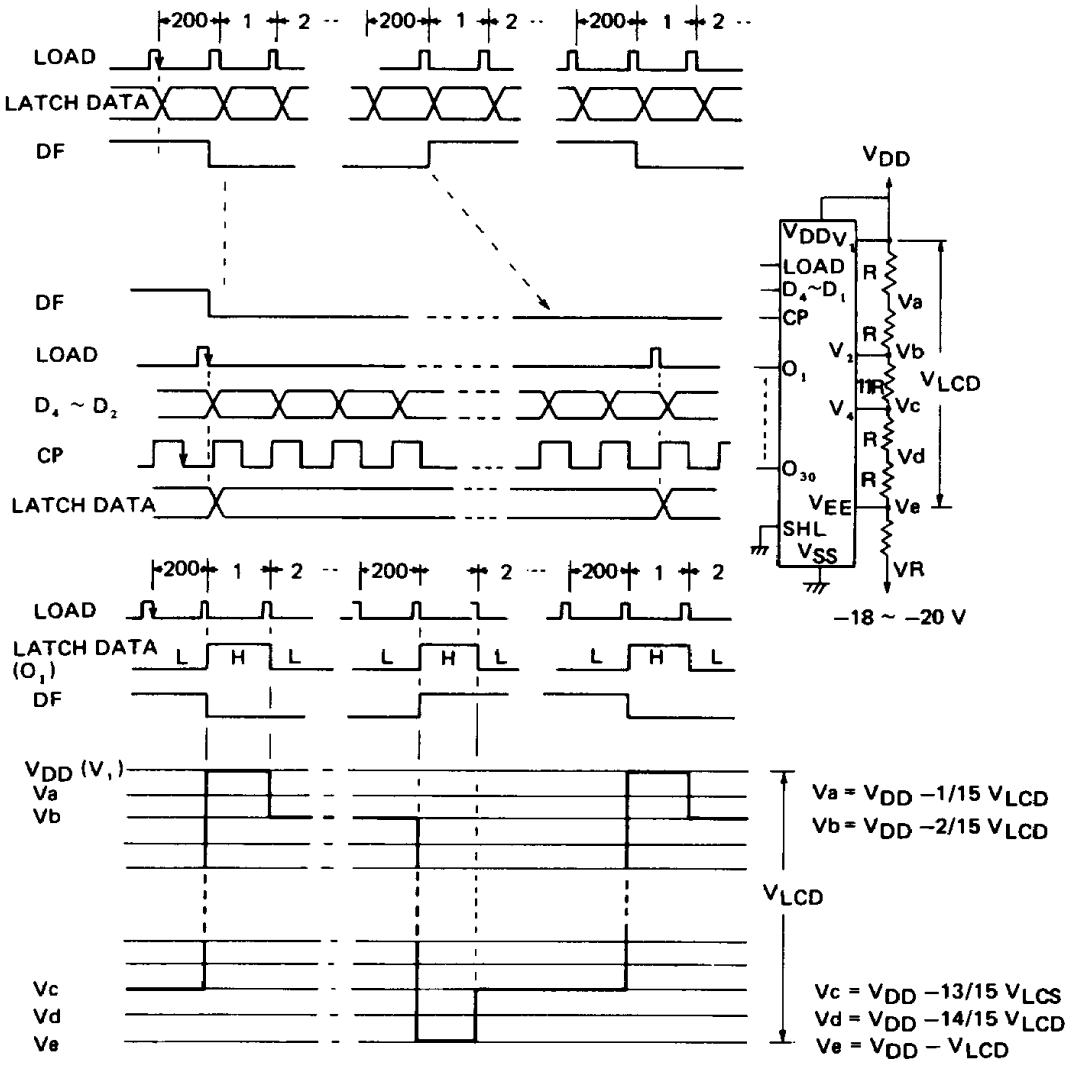


- **$O_1 \sim O_{80}$**
  Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table on the right).

- **$\overline{\text{DISP OFF}}$**
  Control input pin for display data output level ($O_1 \sim O_{80}$). V_1 level is output from $O_1 \sim O_{80}$ pin during "L" level input.
  LCD becomes non-visual by V_1 level output from every output of segment drivers and every output of common drivers.

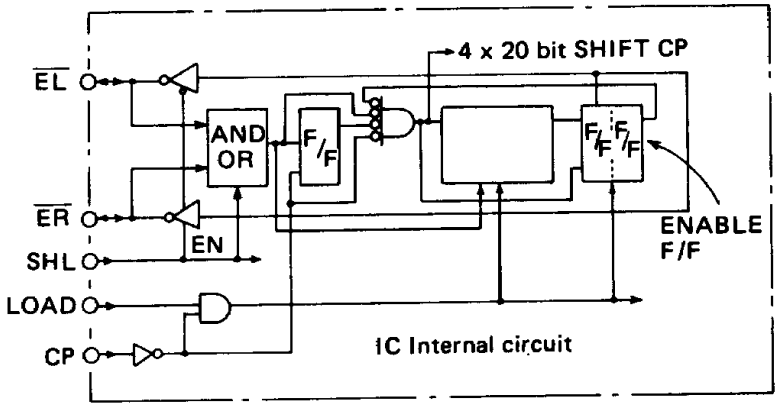
TIMING CHART

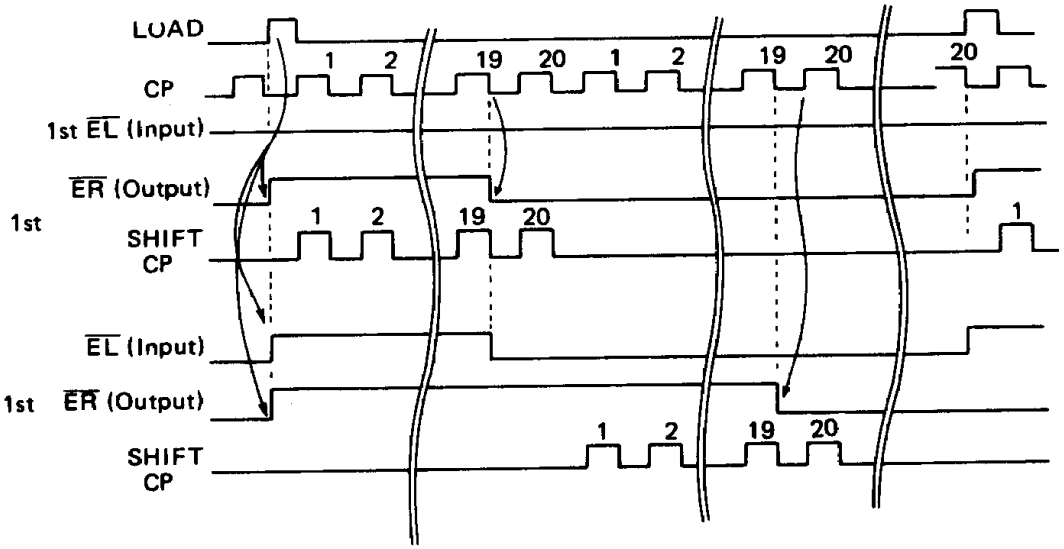
1/200 duty, 1/15 Bias



POWER DOWN FUNCTION

When more than two MSM5299BGSs are being connected in series, cascade connection, power down function of MSM5299BGS can be utilized using the ENABLE F/F (flip flop circuit) in individual MSM5299BGSs. (Regarding the internal circuit configuration of MSM5299BGS, refer to the figure below.) The display data is processed only in the MSM5299BGS, the ENABLE F/F of which is being activated by setting its $\overline{ER}$ and $\overline{EL}$ at low level, while the display data is not processed in the MSM5299BGS, the ENABLE F/F of which is not being activated and the low power consumption condition (I_{DD} SBY) is being held. The activated condition of this ENABLE F/F is being shifted to next MSM5299BGS one after another so that the ENABLE F/F of only one MSM5299BGS out of the cascade connected MSM5299BGSs should be being activated.





SHL = "H" ($\overline{EL}$ = Input $\overline{ER}$ = Output)
First MSM5299BGS's $\overline{ER}$ should be connected to second MSM5299BGS's $\overline{EL}$

Timing chart when MSM5299BGS's are connected in series (cascade connection)

APPLICATION CIRCUIT