LH5493

4K × 9 Parallel-to-Serial FIFO

FEATURES

- Fast Cycle Times: 30/35 ns
  Frequency: 33/28.5 MHz
- Parallel Data In; Serial Data and/or Parallel Data Out
- Serial Input and Serial Shift Capability in Output Register, for Long-Word-Length Parallel-to-Serial Operations
- Read Enable Input and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Reset/Reread Capability
- TTL/CMOS-Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5493 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 nine-bit words. One LH5493 FIFO can input nine-bit bytes; and it can either output nine-bit bytes in parallel, or else output a serial bitstream. Thus, a single LH5493 is capable of nine-bit-to-one-bit PISO (Parallel-In, Serial-Out) operation.

An LH5493 has one 9-bit parallel input (write) port, and one nine-bit parallel output (read) port. And there is one one-bit serial input, which supports paralleling LH5493s for greater-word-width PISO operation. This serial input also allows additional control bits to be inserted at will into the serial output bitstream. There is no serial output port as such; *any* individual bit position in the parallel output register may be chosen as the serial-output data path, according to the desired time phase of the output bitstream.

The LH5493 architecture supports a very convenient method of *paralleling* multiple FIFOs for PISO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5493 combination remains capable of performing all of the operations which a standalone LH5493 can perform. Thus, if two LH5493s are paralleled, the combination can input 18-bit halfwords; and it can either output 18-bit halfwords, or else output a serial bitstream for 18-bit-to-1-bit PISO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5493s.

The LH5493 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

Two edge-sampled enable control inputs, $\overline{WEN_1}$ and $\overline{WEN_2}$, are provided for the input port; and one such control input, REN, is provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5493 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

PIN CONNECTIONS

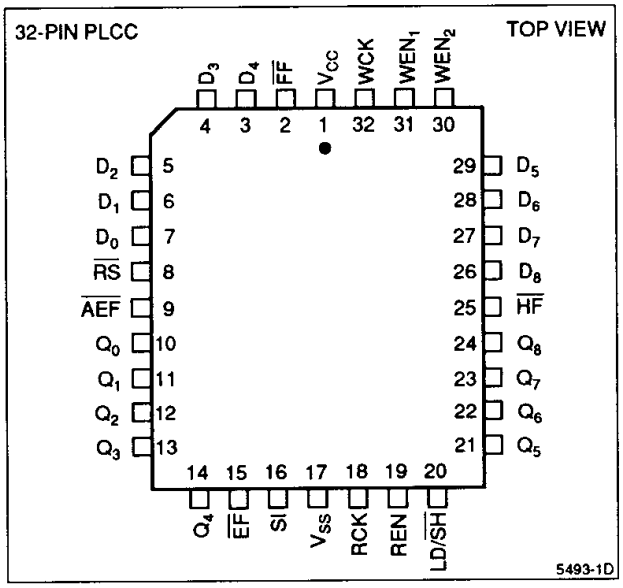


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

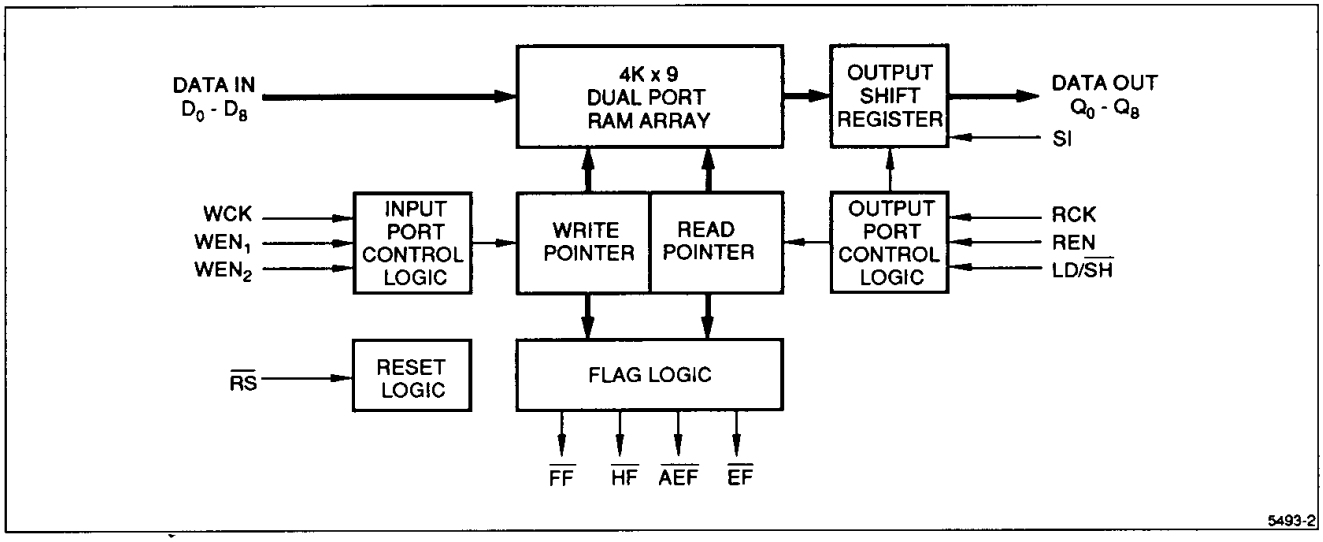


Figure 2. LH5493 Block Diagram

SIGNAL PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
SI	Serial Input. A serial data input to allow paralleled PISO operation of multiple devices.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted..
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever REN is being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN	Read Enable. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO.
LD/$\overline{SH}$	Read Load/Shift. An input signal which is sampled on the rising edge of RCK to control the loading or shifting of data in the output register.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to Vss Potential	−0.5 V to 7 V
Signal Pin Voltage to Vss Potential[3]	−0.5 V to Vcc + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	Vcc + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to Vcc	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at fc = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

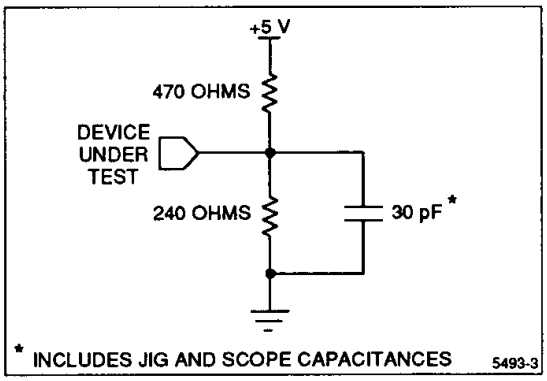


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-30		-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	30	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	12	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	12	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half-Full Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 both are being asserted, or else a rising edge of RCK occurs while REN is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful write.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation. However, failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register and seen on the output bus (Q_0 – Q_8) consists of all zeroes.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In inputs (D_0 – D_8).

When a full condition is reached, write operations should be ceased, in order to prevent overwriting unread data. The state of the status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5493 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, in order to ensure that the write operation is successful.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both the edge-sampled Read Enable input (REN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH for the prescribed setup times and hold times. Read data becomes valid at the Data Out outputs (Q_0 – Q_8) by a time t_A after the rising edge of RCK. A shift of data in the output register is performed whenever REN is held HIGH and LD/$\overline{SH}$ is held LOW on the rising edge of RCK. Data is shifted in the MSB-to-LSB direction, with data from the Serial Input (SI) replacing the contents of bit position Q_8.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. The state of the four status flags has no direct effect on read or shift operations; that is, the execution of read or shift operations is gated only by REN and LD/$\overline{SH}$, and the internal logic of the LH5493 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, shift operations may continue; but read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag will be deasserted ($\overline{EF}$ = HIGH). The first read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write to an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

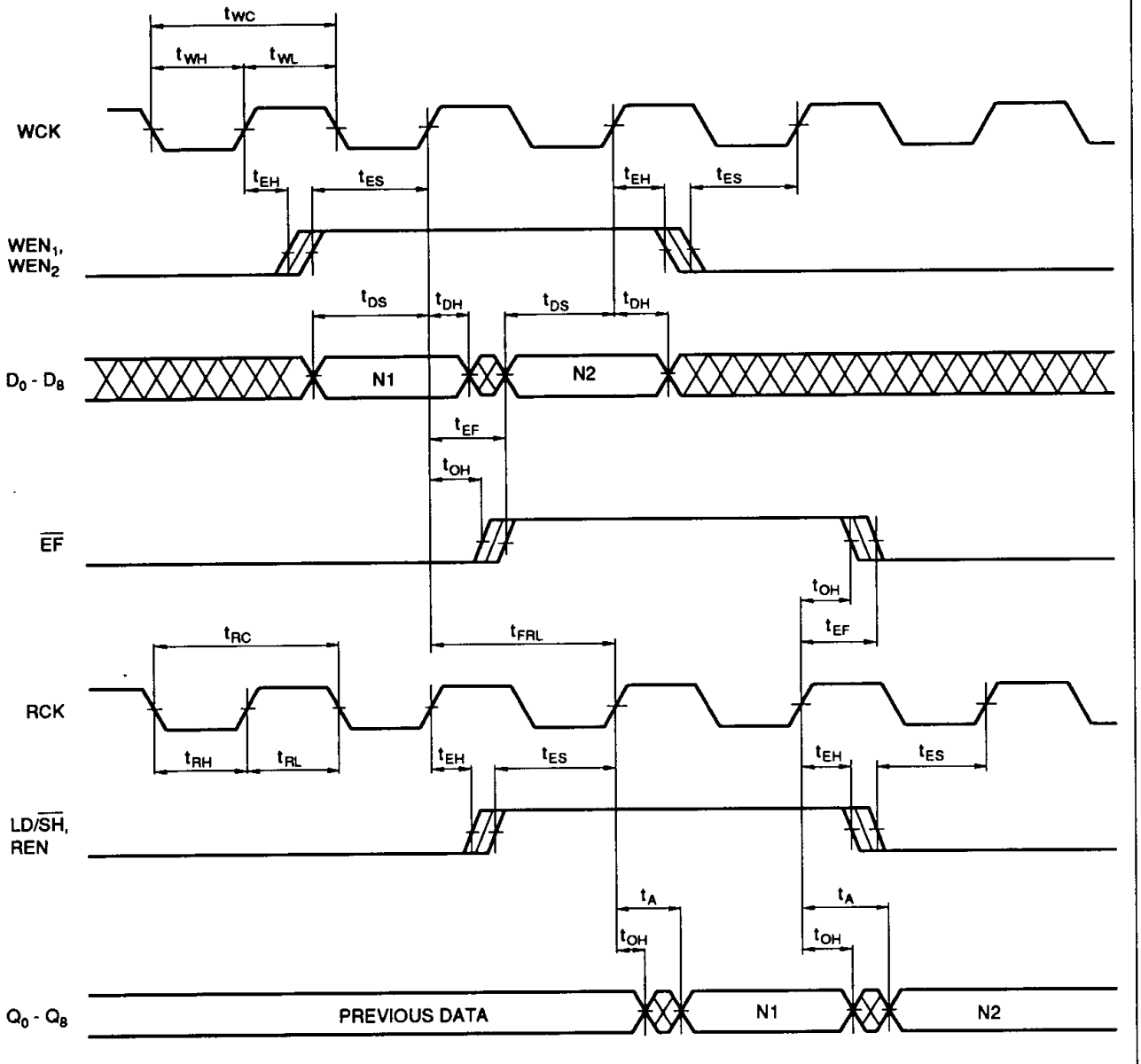
The following four status flags are included: Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1 (page 5-104). Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO may be made to reread previously-read data by means of a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still remain in the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



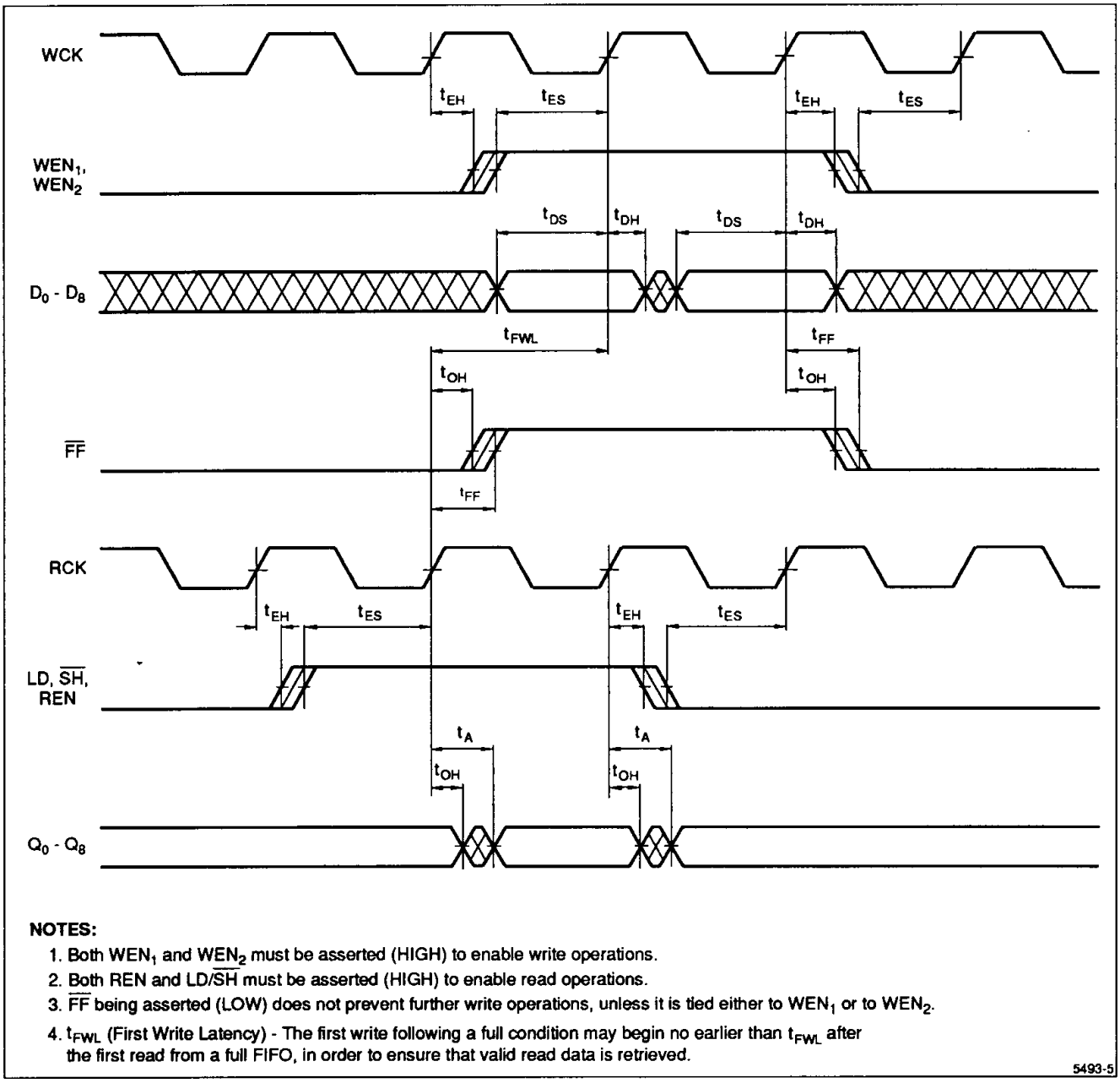
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ being asserted (LOW) does not prevent further read operations, unless it is tied to REN.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.

5493-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ being asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5493-5

Figure 5. Write and Read Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

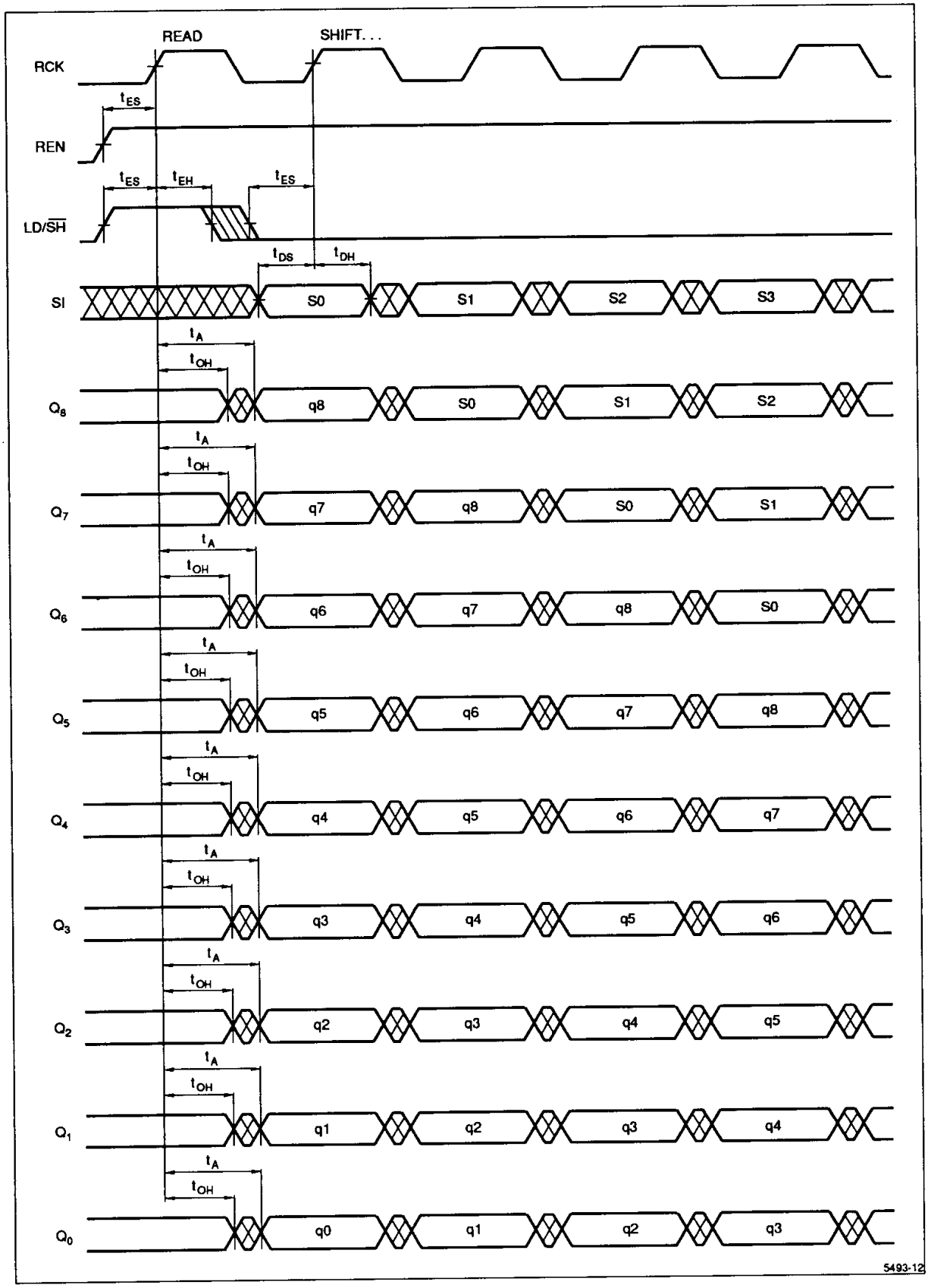


Figure 6. Serial Shift/Read Timing

TIMING DIAGRAMS (cont'd)

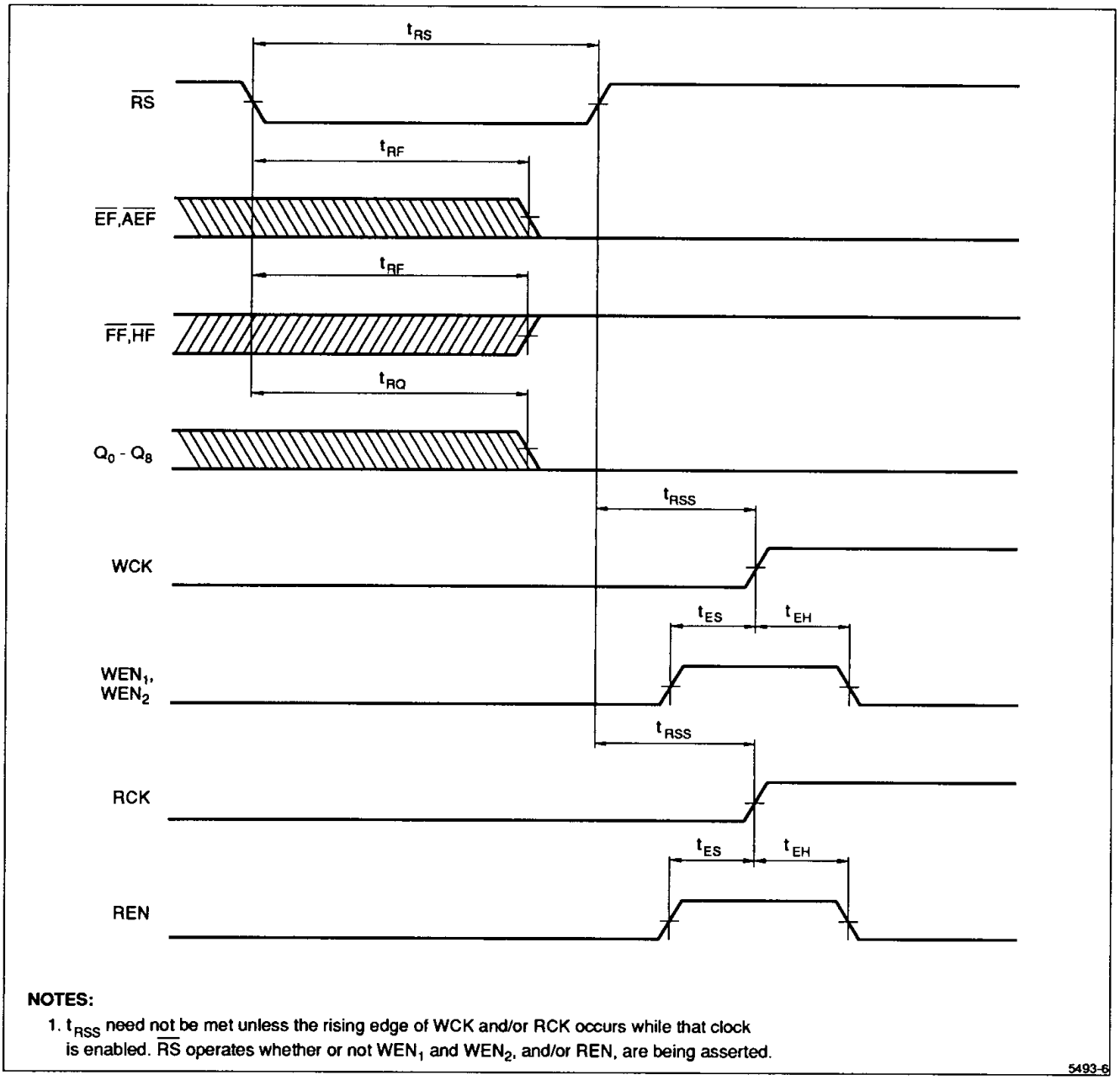
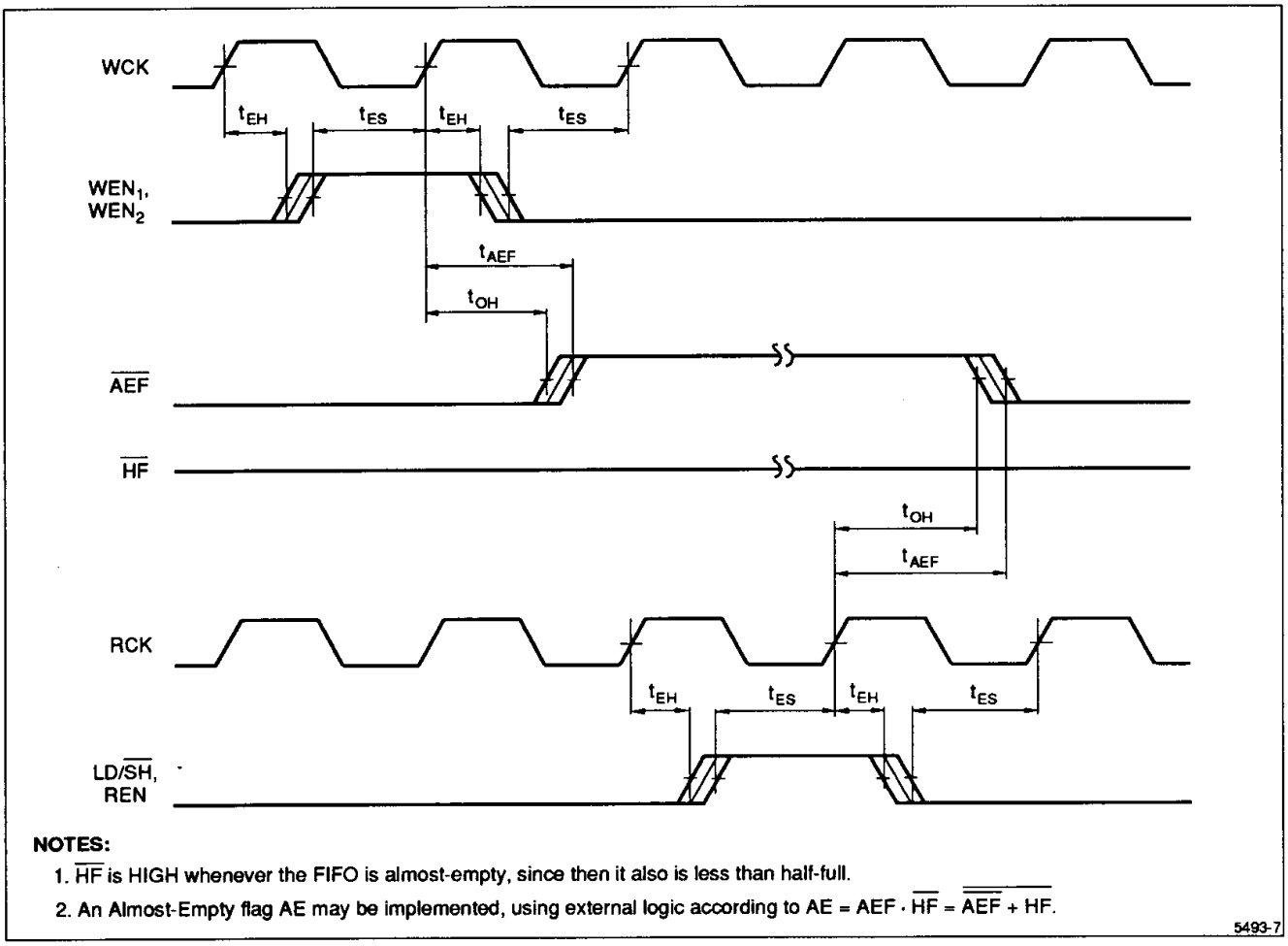


Figure 7. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5493-7

Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

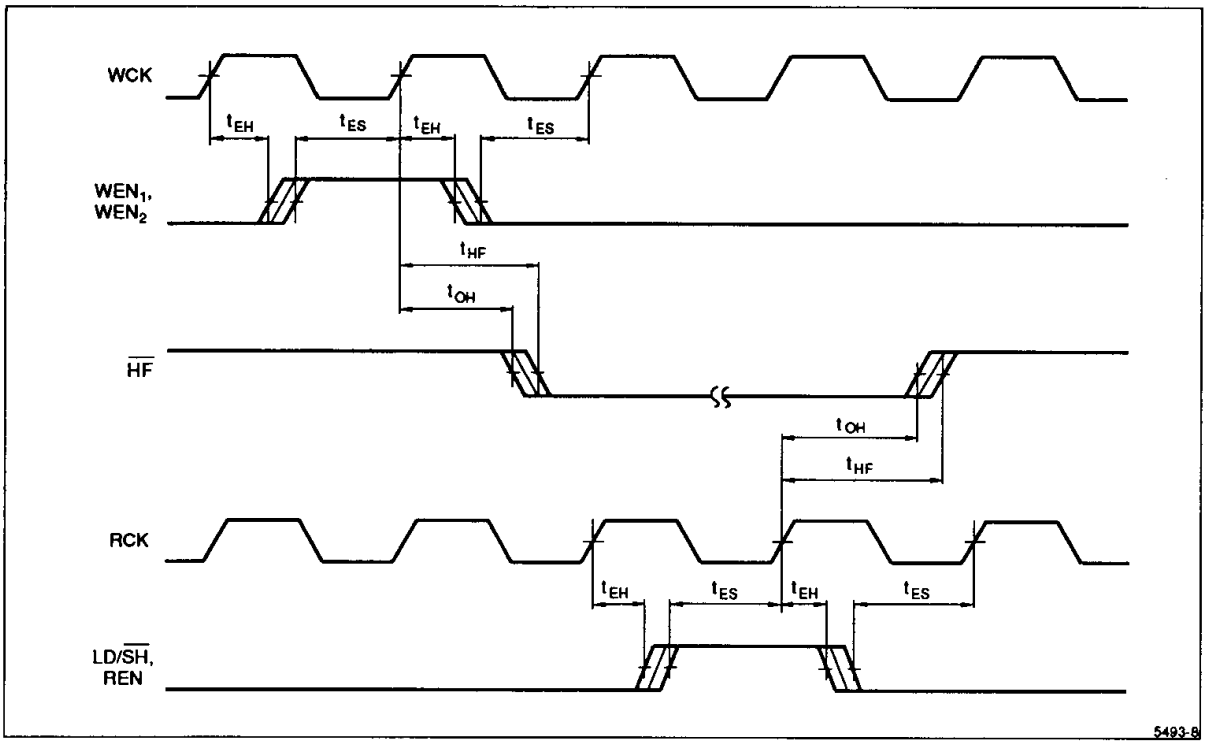
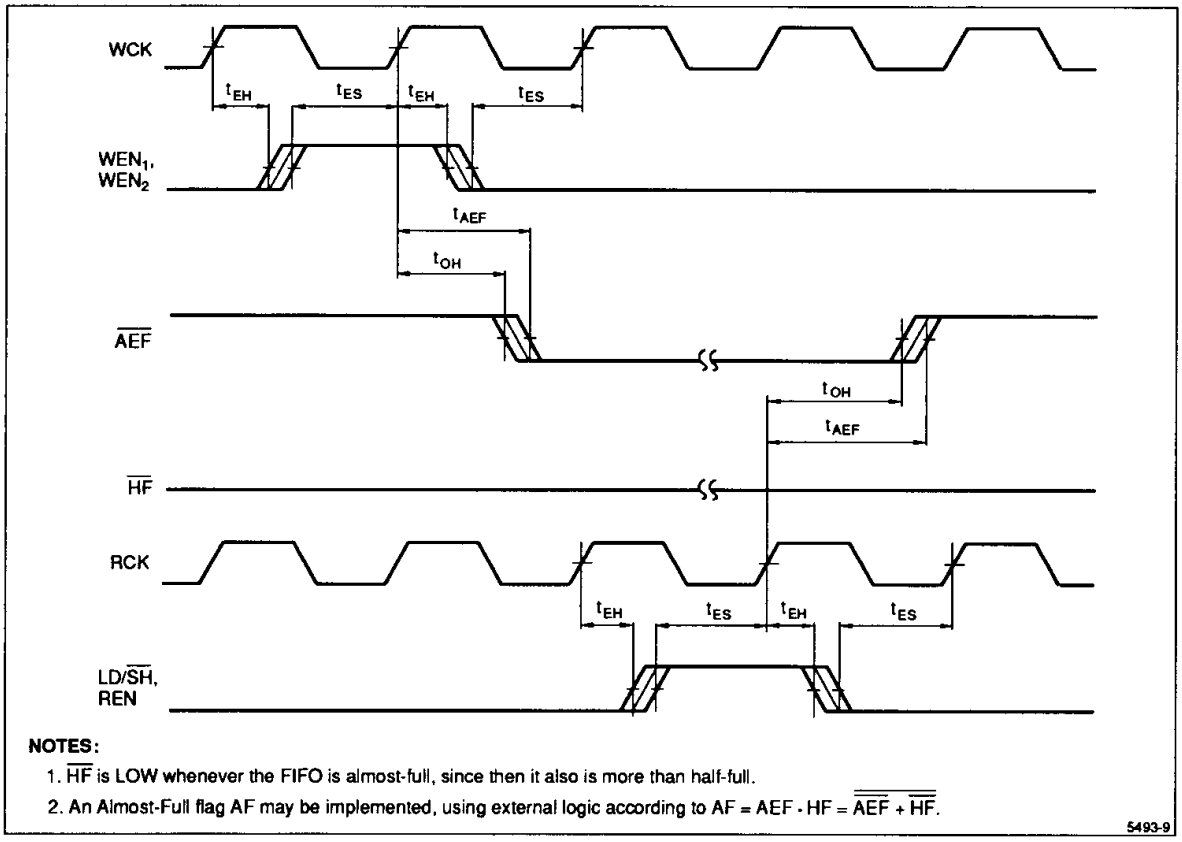


Figure 9. Half-Full Flag Timing



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to AF = AEF · HF = $\overline{\overline{AEF} + \overline{HF}}$.

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Write and Read Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2), Read Enable (REN), and Load/Shift ($LD/\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, and REN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN_1 or WEN_2, to prevent 'overrun' write operations after the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN, to prevent 'underrun' read operations after the empty condition is reached.

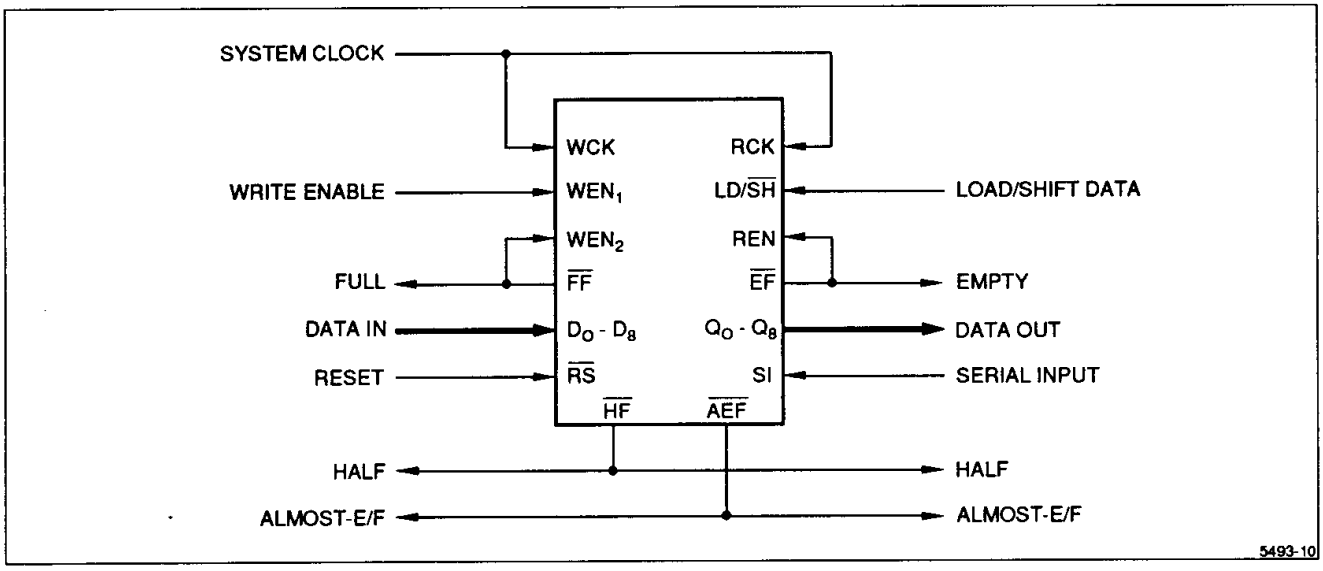


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Write and Read Operations

Write operations and read operations may be performed completely asynchronously with respect to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Write Enable or Read Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

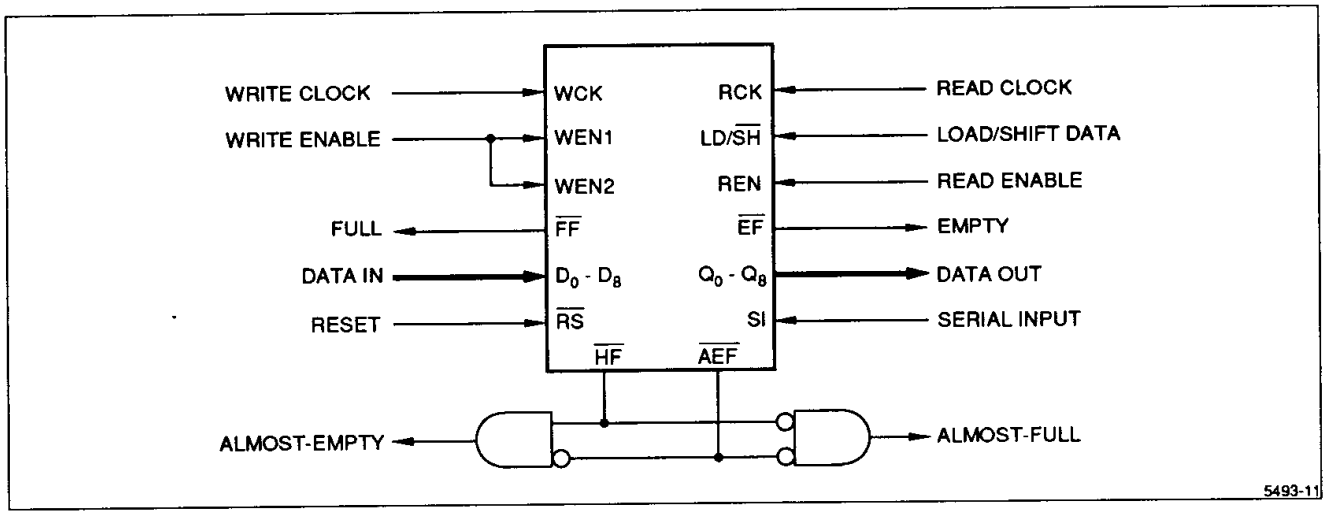


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Paralleled Operation

In paralleled operation, two or more LH5493 FIFOs are chained together into a wider 'effective FIFO.' The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. This 'effective-FIFO' serial input may be used to insert additional control bits into the serial data stream, or may be tied to a permanent logic LOW or HIGH signal if unused. The SI input of each subsequent device is connected to one of the Data Out outputs ($Q_8 - Q_0$) of the preceding device in the chain. The final 'effective-FIFO' serial output bitstream is taken from one of the Data Out outputs of the last device in the chain. By choosing different Data Out pins, an additional one to nine bits of width can be added per device.

In 'paralleled' operation, the write enable inputs WEN_1 and WEN_2, and the read enable input REN, may be made common for all devices. Since there are multiple write enable inputs, one of them on each FIFO device may be crosscoupled to the Full Flag on another FIFO device, or to the logic AND of several such Full Flags, in order to prevent any individual FIFO device from getting out of synchronization with the overall 'effective FIFO.' The approach is analogous to the method shown in Figure 11 for preventing an LH5493 from overrunning its internal FIFO boundaries. Implementing the equivalent measures during reading always requires some external logic, since each LH5493 has just one read enable input.

Word widths do not have to be a multiple of nine. For instance, making the following changes to the circuit of Figure 13 adapts it to handle 16-bit parallel data in. The D_0 input and the Q_0 output need not be used for either LH5493. The Q_1 output of the LH5493 on the left is connected to the SI input of the LH5493 on the right; and the Q_1 output of the LH5493 on the right becomes the main 'Serial Data Out' output.

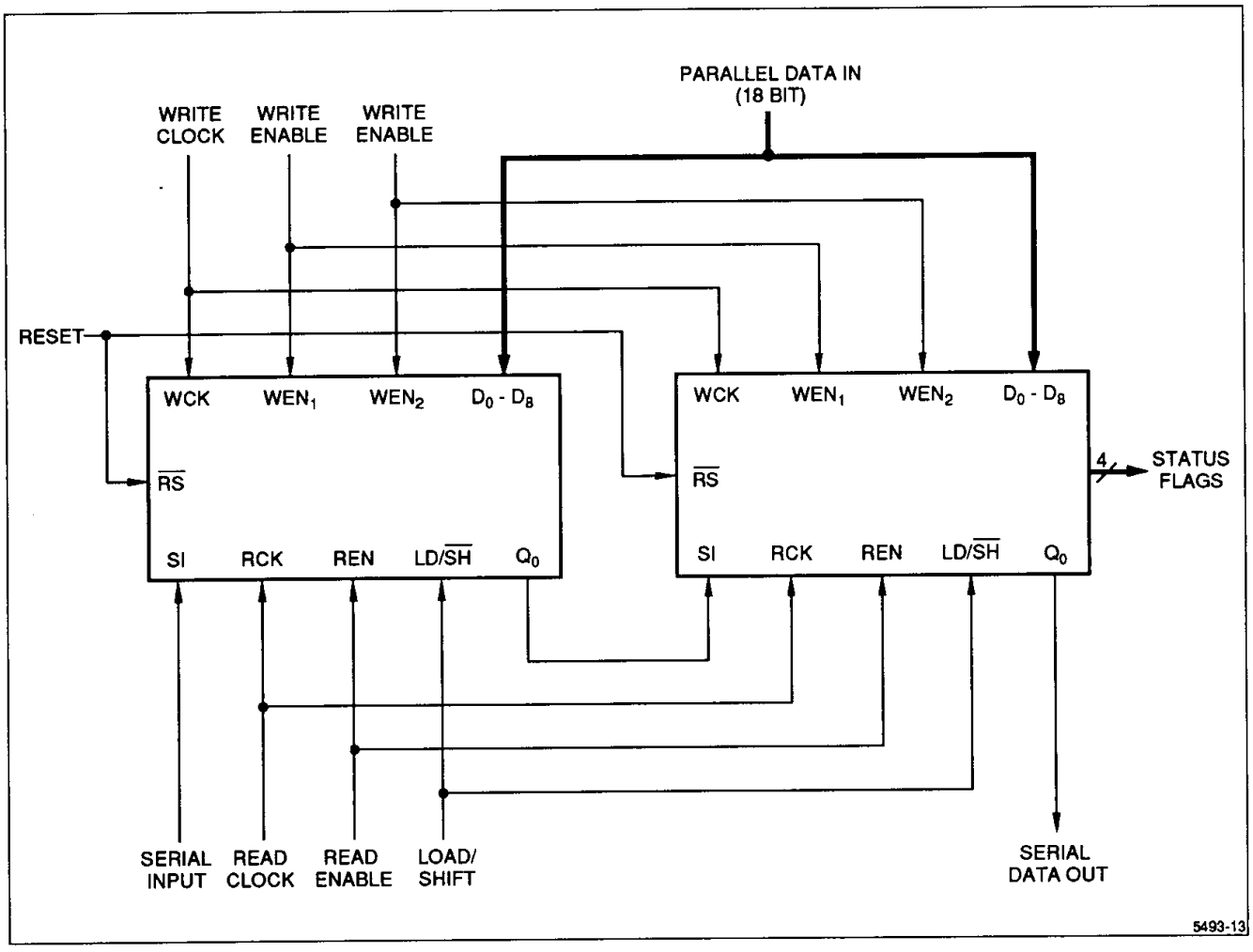


Figure 13. Paralleled Serial Operation (4096 × 18 Bit)

ORDERING INFORMATION