

LH53B16R00

CMOS 16M (1M × 16/512K × 32) MROM

FEATURES

- 1,048,576 × 16 bit organization
(Word mode: $\overline{W} = V_{IL}$)
524,288 × 32 bit organization
(Double Word mode: $\overline{W} = V_{IH}$)
- Access time: 120 ns (MAX.)
Access time in page mode: 50 ns (MAX.)
- Supply current:
 - Operating: 180 mA (MAX.)
 - Standby: 300 μ A (MAX.)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Static operation
- Package:
70-pin, 500-mil SSOP
- Others:
 - Non programmable
 - Not designed or rated as radiation
 - hardened
 - CMOS process (P type silicon substrate)

DESCRIPTION

The LH53B16R00 is a 16M-bit CMOS mask ROM (mask-programmable-read-only memory) organized as 1,048,576 × 16 bits (Word mode) or 524,288 × 32 bits (Double Word mode). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

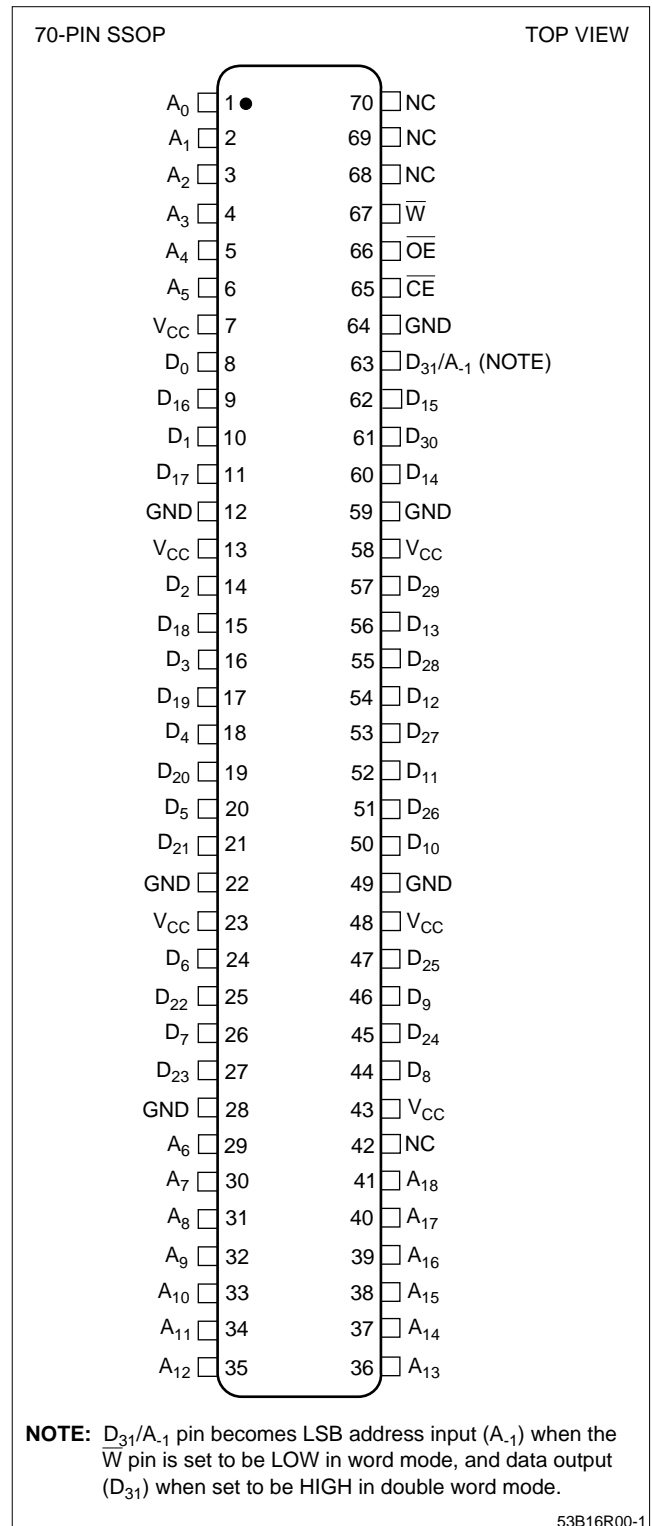
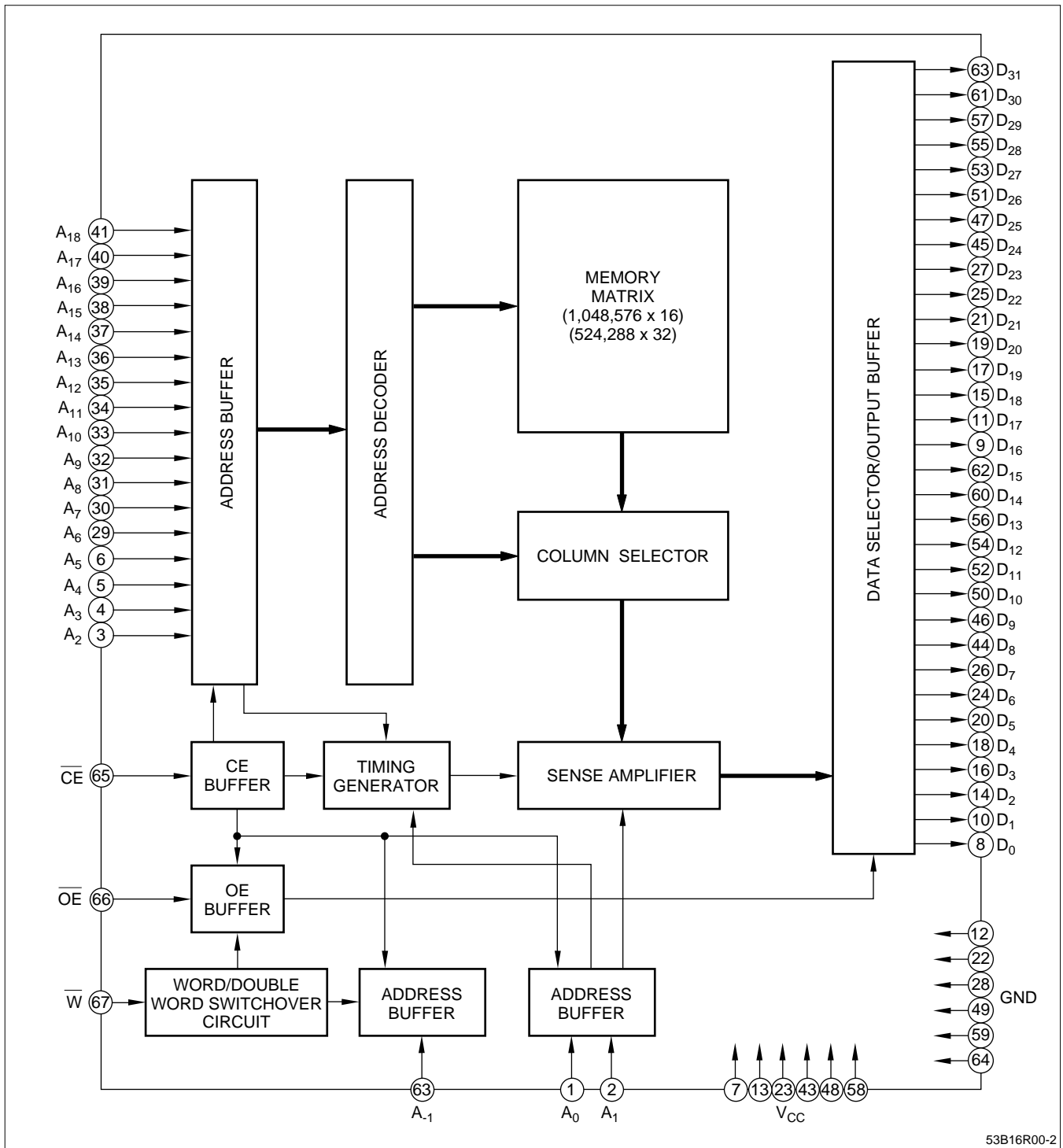


Figure 1. Pin Connections



53B16R00-2

Figure 2. LH53B16R00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₋₁ - A ₁	Address input (page mode operation)
A ₂ - A ₁₈	Address input
D ₀ - D ₃₁	Data output
\bar{W}	×16 bit / ×32 bit (word/double word) mode select input

SIGNAL	PIN NAME
CE	Chip enable input
OE	Output enable input
V _{CC}	Power pin (+5 V)
GND	Ground
NC	No connection

TRUTH TABLE

\bar{CE}	\bar{OE}	\bar{W}	A ₋₁ (D ₃₁)	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				D ₀ - D ₁₅	D ₁₆ - D ₃₁	LSB	MSB	
H	X	X	X	High-Z	High-Z	—	—	Standby (I _{SB})
L	H	X	X	High-Z	High-Z	—	—	Operating
L	L	H	—	D ₀ - D ₁₅	D ₁₆ - D ₃₁	A ₀	A ₁₈	Operating
L	L	L	L	D ₀ - D ₁₅	High-Z	A ₋₁	A ₁₈	Operating
L	L	L	H	D ₁₆ - D ₃₁	High-Z	A ₋₁	A ₁₈	Operating

NOTE:

X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _{OUT}	-0.3 to V _{CC} + 0.3	V
Operating temperature	T _{OPR}	0 to +70	°C
Storage temperature	T _{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.2	$V_{CC} + 0.3$	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4	—	V	—
Output 'Low' voltage	V_{OL}	$I_{OL} = 2.0\ \text{mA}$	—	0.4	V	—
Input leakage current	$ I_{LI} $	$V_{IN} = 0\ \text{V to } V_{CC}$	—	10	μA	—
Output leakage current	$ I_{LO} $	$V_{OUT} = 0\ \text{V to } V_{CC}$	—	10	μA	1
Operating current	I_{CC1}	$t_{RC} = 120\ \text{ns}$	—	180	mA	2
Standby current	I_{SB1}	$CE = V_{IH}$	—	2	mA	—
	I_{SB2}	$CE = V_{CC} - 0.2\ \text{V}$	—	300	μA	—
Input capacitance	C_{IN}	$f = 1\ \text{MHz}$, $T_A = 25^\circ\text{C}$	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:

- $CE = V_{IH}$, $OE = V_{IH}$, output is open
- $V_{IN} = V_{IH}$, V_{IL} , $CE = V_{IL}$, output is open

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Page address access time	t_{APA}	—	50	ns	—
Output enable delay time	t_{OE}	—	50	ns	—
Output hold time	t_{OH}	5	—	ns	—
Output floating time	t_{CHZ}	—	40	ns	1
	t_{OHZ}	—	40	ns	

NOTE:

- Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to 2.6 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

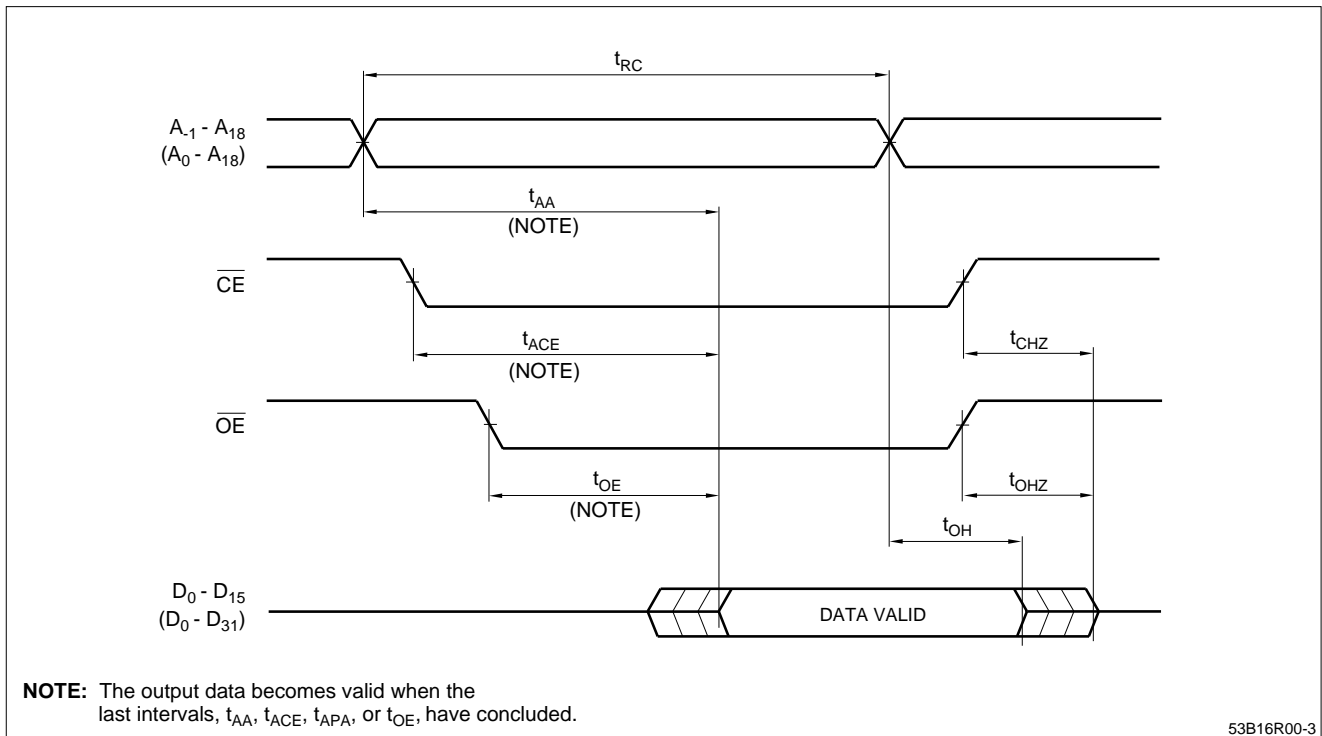


Figure 3. Read Cycle

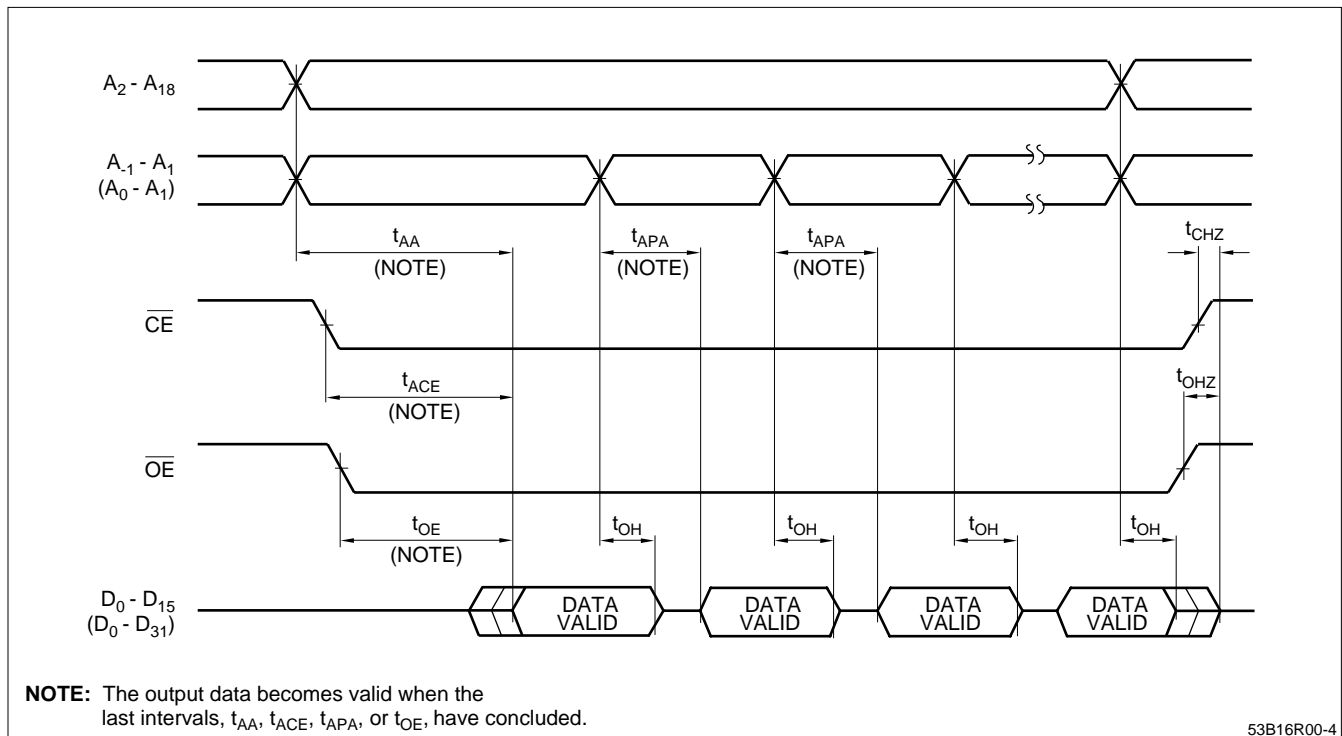
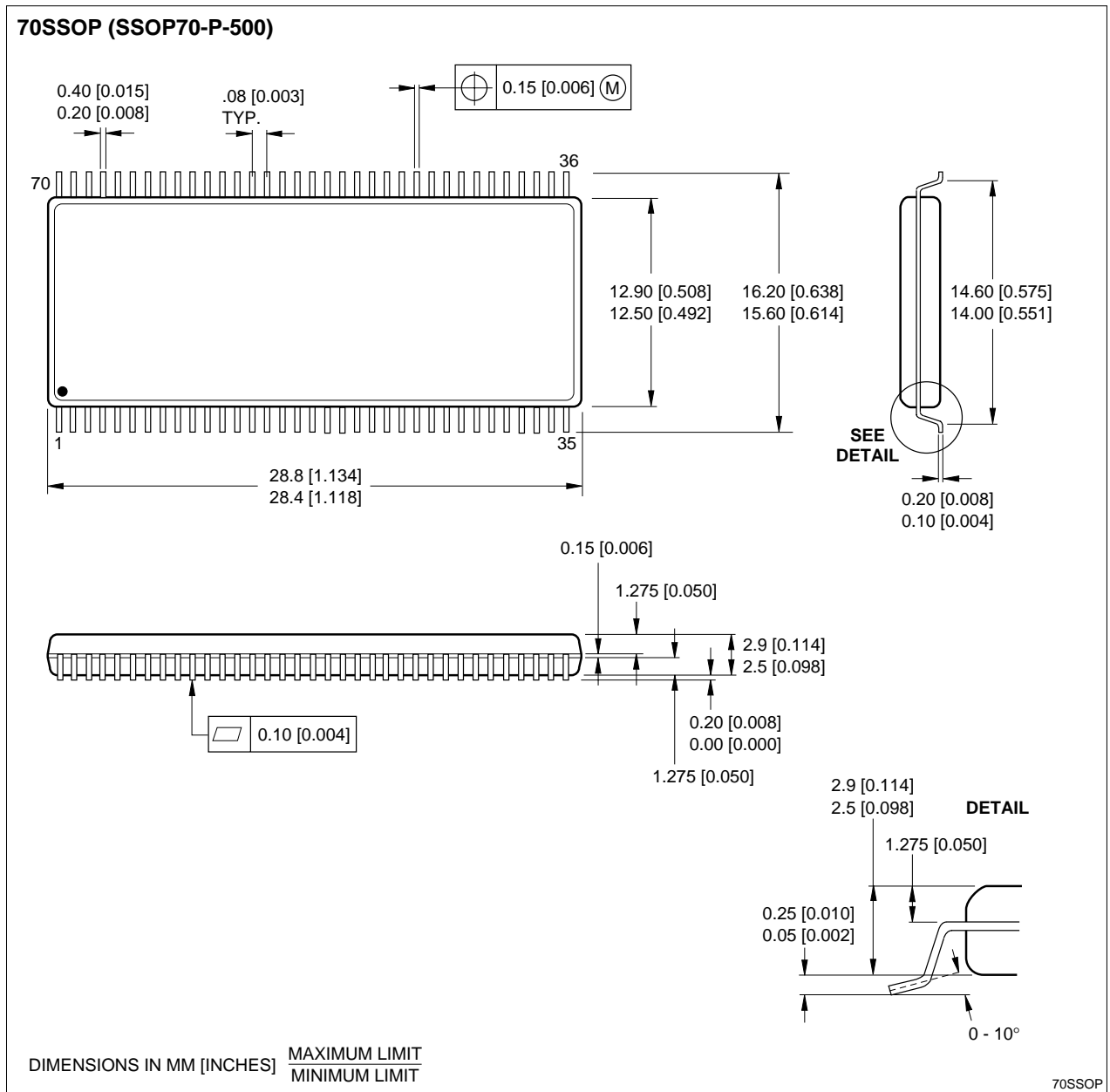


Figure 4. Page Mode Read Cycle

PACKAGE DIAGRAM



ORDERING INFORMATION

