LH5324C00

CMOS 24M (1.5M × 16) MROM

FEATURES

- 1,572,864 × 16 bit organization
- Access time: 120 ns (MAX.)
- Supply current:
  - Operating: 80 mA (MAX.)
  - Standby: 100 µA (MAX.)
- TTL compatible I/O
- Three-state output
- Single +5 V Power supply
- Static operation
- When the address input at both A_{19} and A_{20} is high level, outputs become high impedance irrespective of $\overline{CE}$ or $\overline{OE}$.
- Package:
  42-pin, 600-mil DIP
- Others:
  - Non programmable
  - Not designed or rated as radiation hardened
  - CMOS process (P type silicon substrate)

DESCRIPTION

The LH5324C00 is a 24M-bit mask-programmable ROM organized as 1,572,864 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

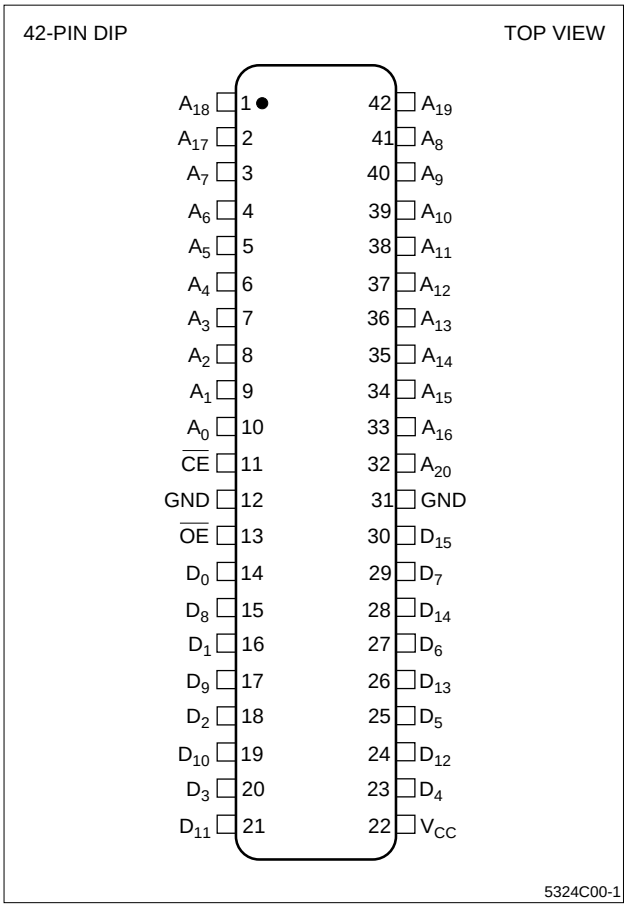


Figure 1. Pin Connections

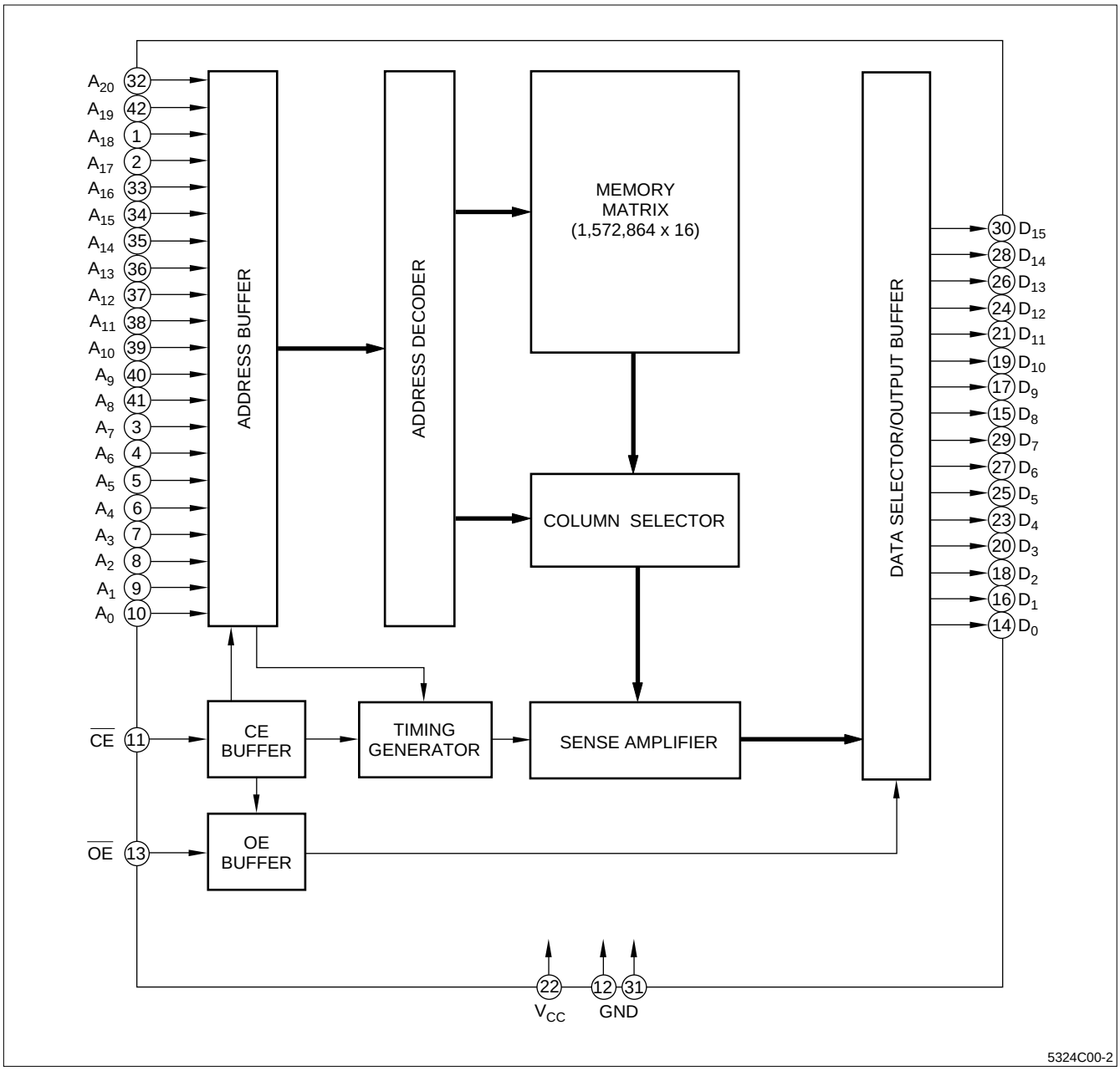


Figure 2. LH5324C00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{20}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	A_0 - A_{18}	A_{19}	A_{20}	DATA OUTPUT D_0 - D_{15}	SUPPLY CURRENT
H	X	X	X	X	High-Z	Standby (I_{SB})
L	H	X	X	X	High-Z	Operating (I_{CC})
L	L	X	L	L	Output	Operating (I_{CC})
L	L	X	L	H	Output	Operating (I_{CC})
L	L	X	H	L	Output	Operating (I_{CC})
L	L	X	H	H	High-Z	Operating (I_{CC})

NOTES:
1. X = Don't care; High-Z = High-impedance
2. When the address inputs become HIGH to both A_{19} and A_{20}, the data does not exist in this address area, the data outputs become "High Impedance".

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	T_{OPR}	0 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	2.2	V_{CC} + 0.3	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.8	V	—
Output 'High' voltage	V_{OH}	I_{OH} = -400 µA	2.4	—	V	—
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA	—	0.4	V	—
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}	—	10	µA	—
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}	—	10	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns	—	80	mA	2
	I_{CC2}	t_{RC} = 1 µs	—	70		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	2	mA	—
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V	—	100	µA	—
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, output is open

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5 V ± 10%, T_A = 0 to +70°C)

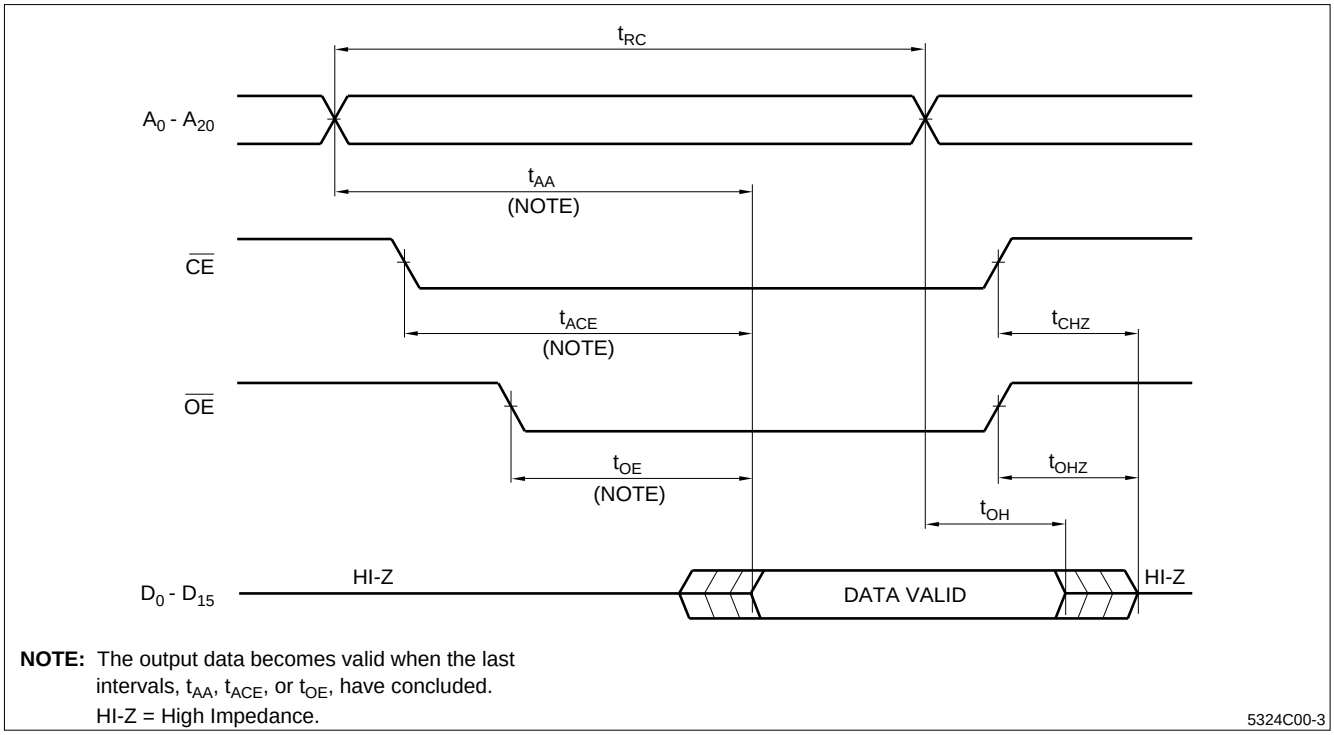
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Output enable delay time	t_{OE}	—	60	ns	—
Output hold time	t_{OH}	0	—	ns	—
Output floating time	t_{CHZ}	—	50	ns	1
	t_{OHZ}	—	50	ns	
	t_{AHZ}	—	60	ns	

NOTE:
1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

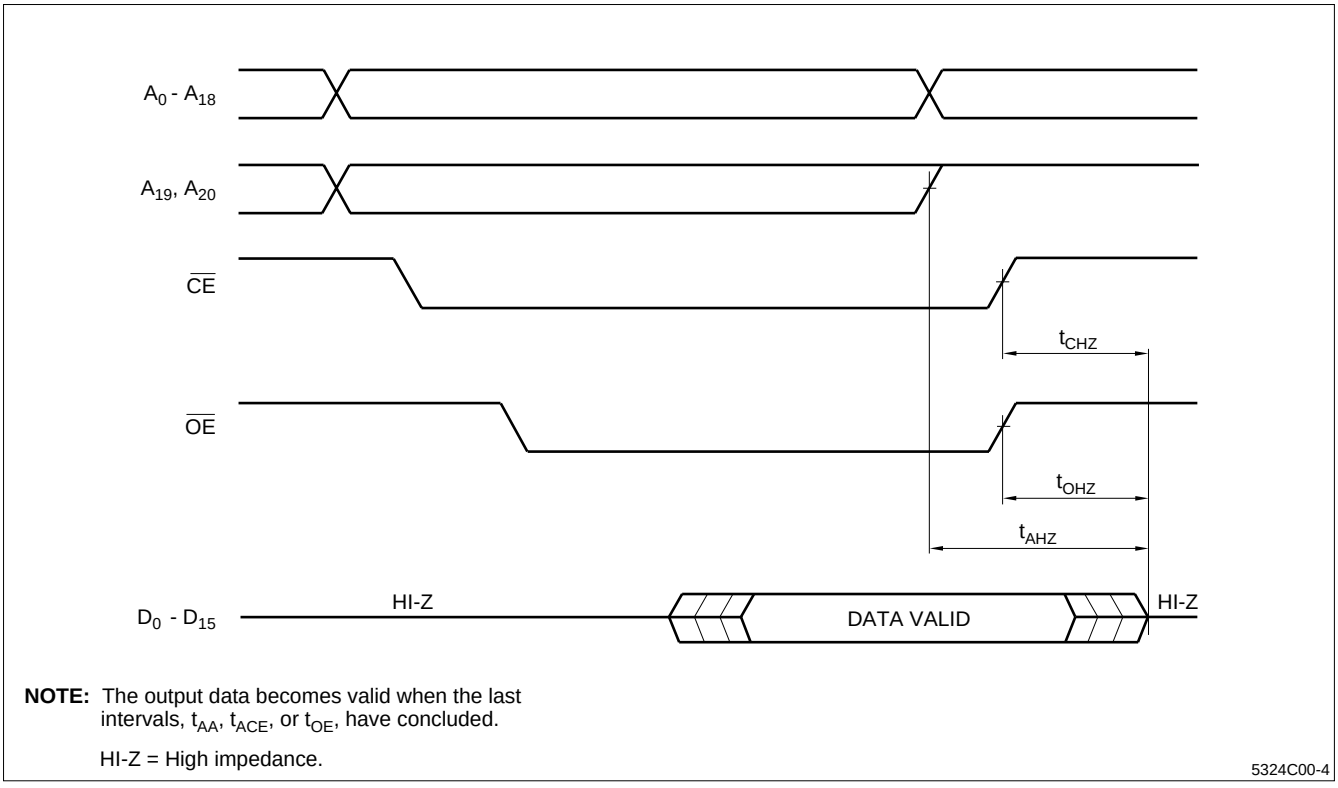
PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input signal rise time	10 ns
Input signal fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL + 100 pF

NOTE:
It is recommended that a decoupling capacitor be connected between V_{CC} and GND-Pin.



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.
HI-Z = High Impedance.

Figure 3. Byte Mode



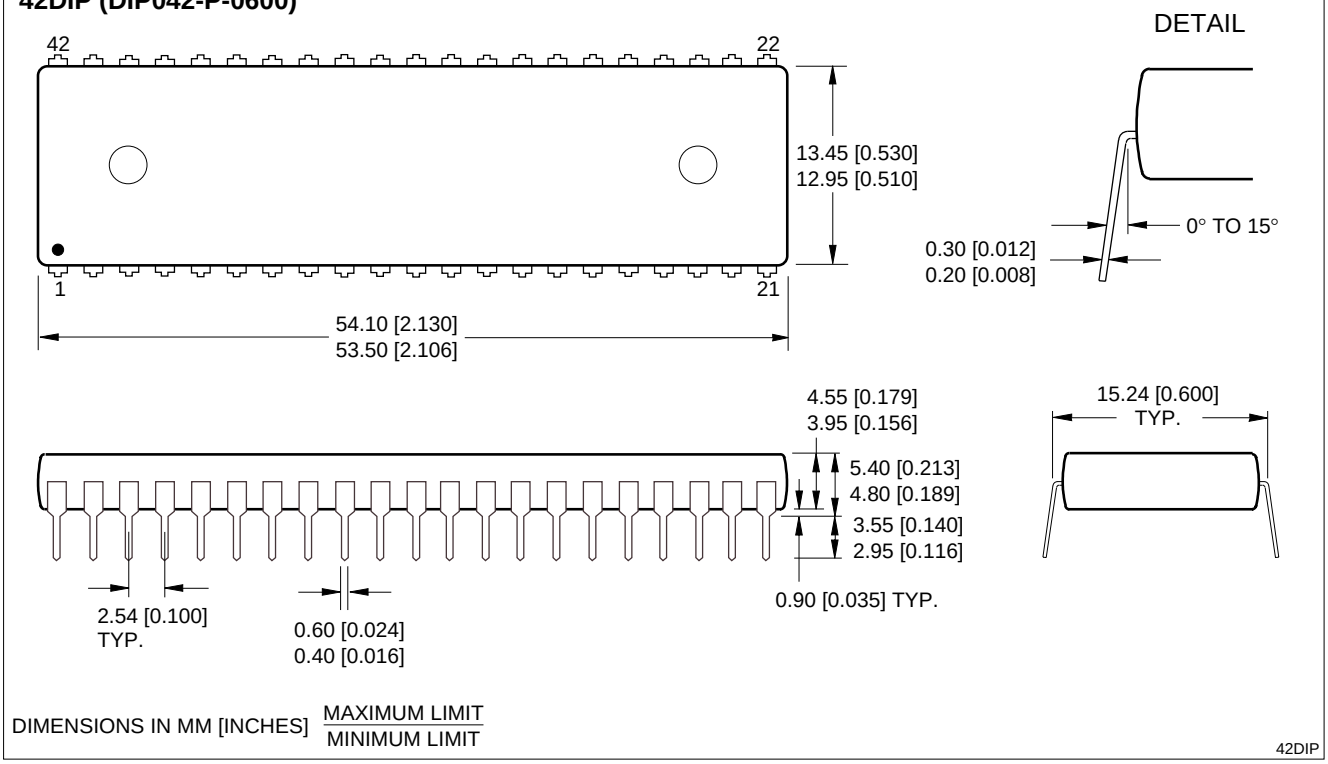
NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

HI-Z = High impedance.

Figure 4. Word Mode

PACKAGE DIAGRAM

42DIP (DIP042-P-0600)



ORDERING INFORMATION