LH530800A-Y

CMOS 1M (128K × 8) 3 V-Drive MROM

FEATURES

- 131,072 words × 8 bit organization
- Access times:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  150 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Low-power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- Three-state outputs
- Mask-programmable control pin:
  Pin 24 = OE/$\overline{OE}$
- Wide range power supply:
  2.6 V to 5.5 V
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP

DESCRIPTION

The LH530800A-Y is a 1M-bit mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

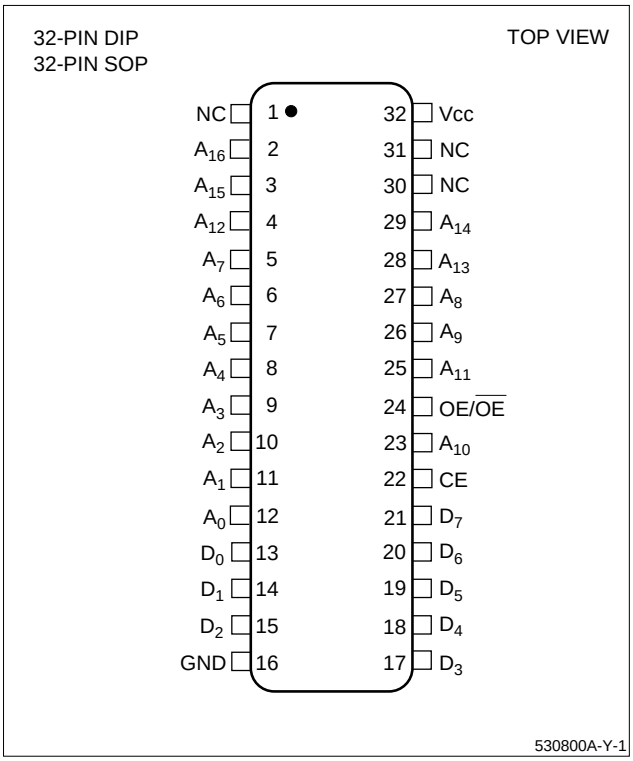


Figure 1. Pin Connections for DIP and SOP Packages

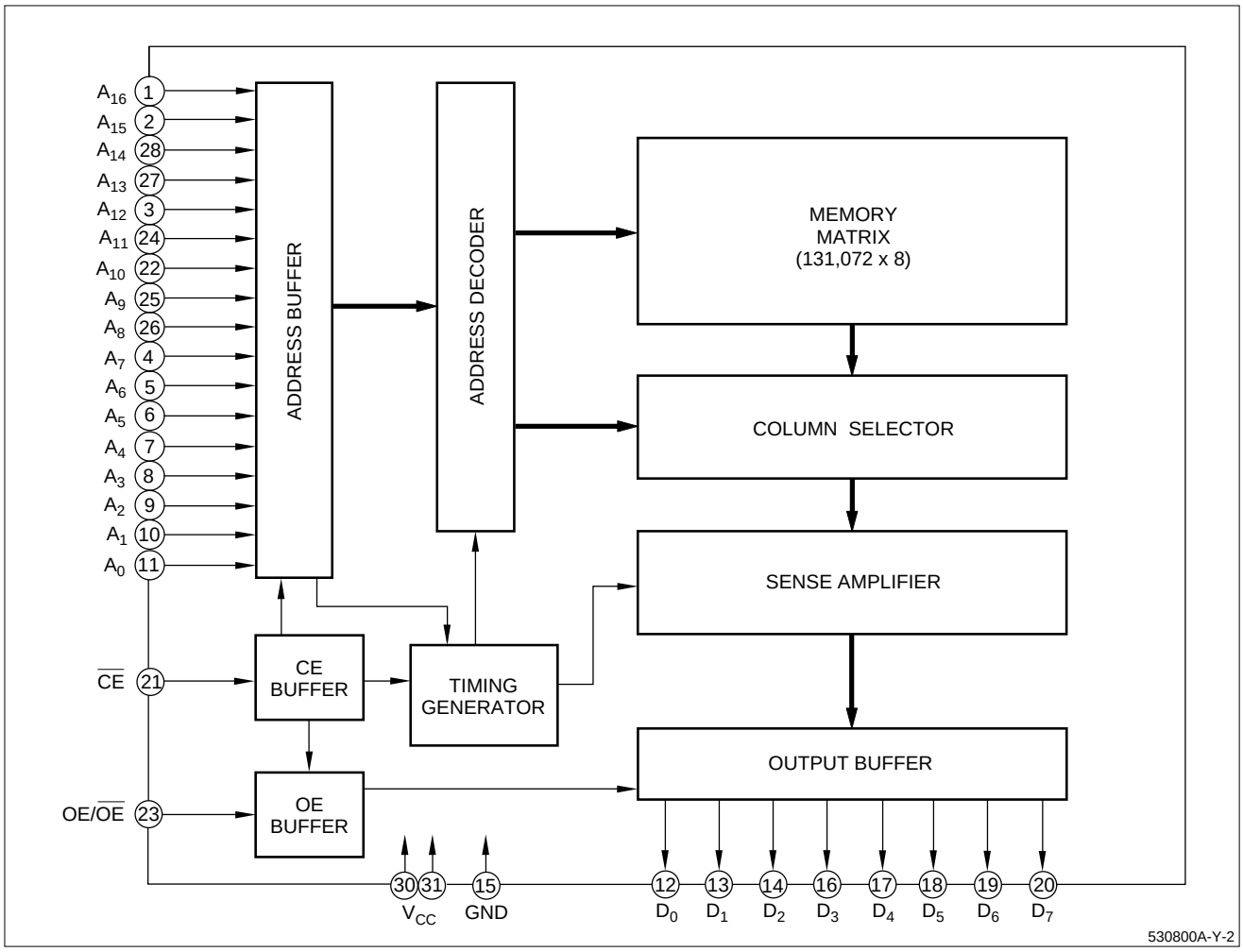


Figure 2. LH530800A-Y Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data Output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply	
GND	Ground	
NC	Non connection	

NOTE:
1. Active levels of OE/$\overline{OE}$ are mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	High-Z	Standby (I_{SB})	1
L	L/H	High-Z	Operating (I_{CC})	
L	H/L	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V

Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 V to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		-0.3		0.4	V	
Input 'High' voltage	V_{IH}		0.8 × V_{CC}		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	0.8 × V_{CC}			V	
Input leakage current	| I_{LI} |	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	| I_{LO} |	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 500 ns			18	mA	3
	I_{CC3}	t_{RC} = 500 ns			12	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}$/$\overline{OE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
2. 4.5 V ≤ V_{CC} ≤ 5.5 V, outputs open
3. 3.4 V < V_{CC} < 4.5 V, outputs open
4. 2.6 V ≤ V_{CC} ≤ 3.4 V, outputs open

AC CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 V ≤ V_{CC} < 4.5 V		4.5 V ≤ V_{CC} ≤ 5.5 V		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		150		ns	
Address access time	t_{AA}		500		150	ns	
Chip enable access time	t_{ACE}		500		150	ns	
Output enable delay time	t_{OE}		200		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

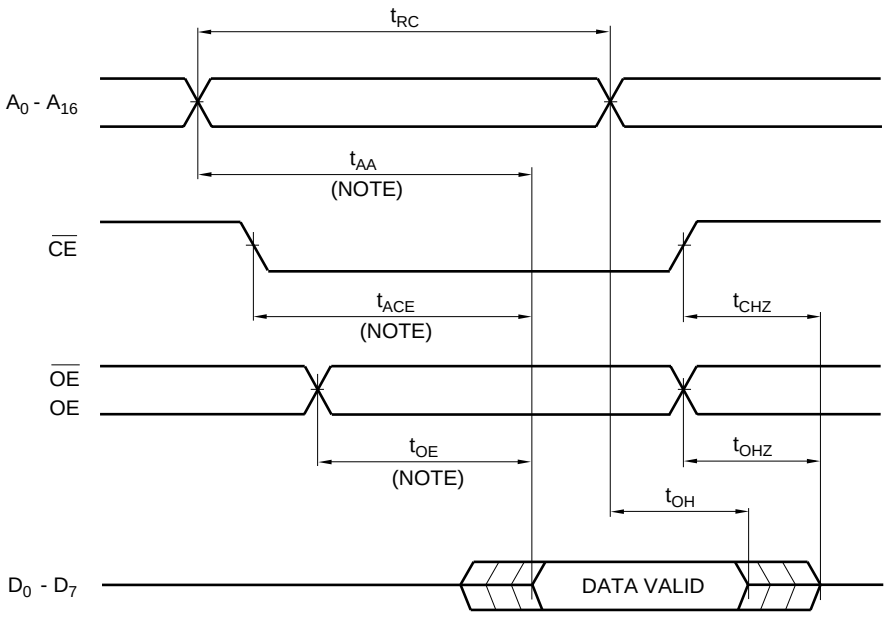
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to (0.8 × V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} and the GND pin.



NOTE: Data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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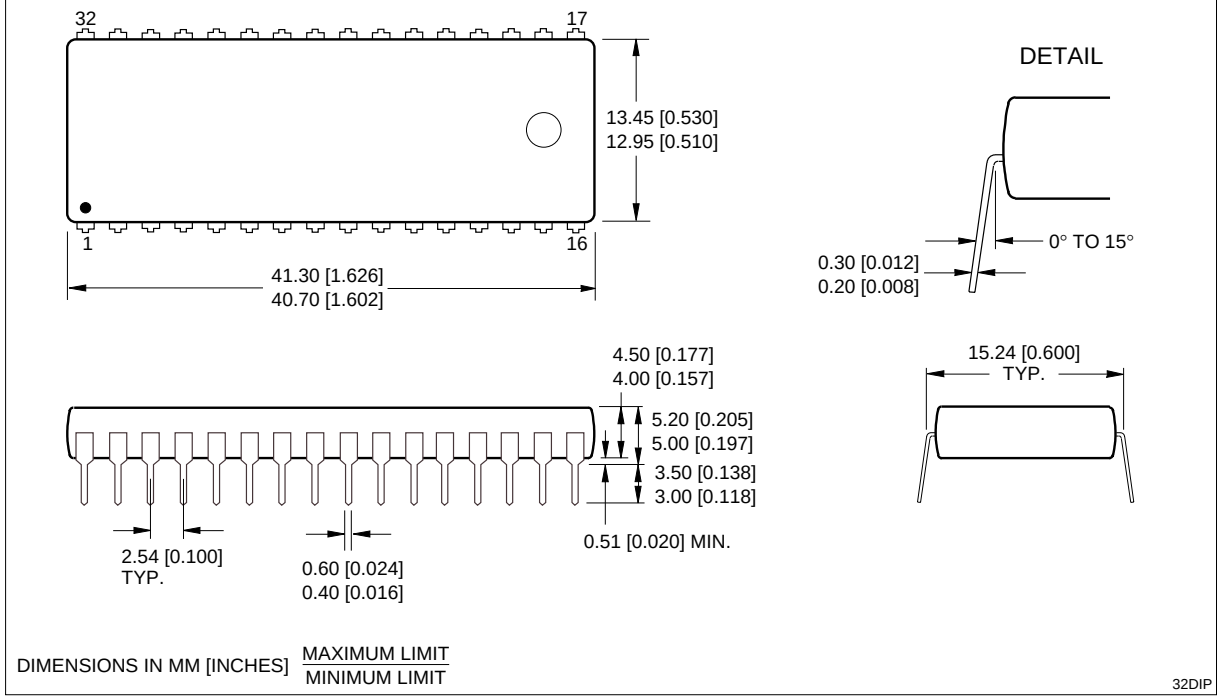
Figure 3. Timing Diagram

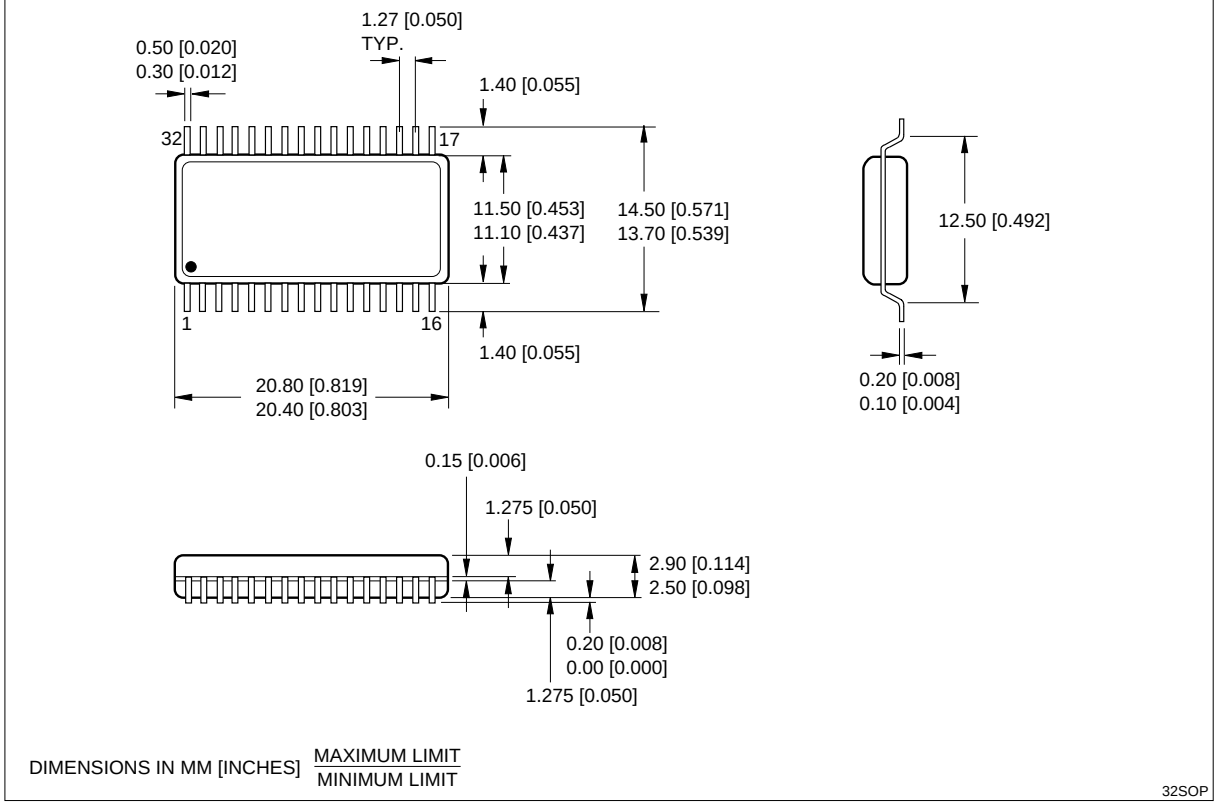
PACKAGE DIAGRAMS

32DIP (DIP032-P-0600)



32-pin, 600-mil DIP

32SOP (SOP032-P-0525)



32-pin, 525-mil SOP

ORDERING INFORMATION