CoreAHB

DirectCore

Product Summary

Intended Use

- CoreAHB Provides an AHB Bus Fabric and Is Intended for Use in an AMBA Subsystem where Multiple AHB Masters are Present

Key Features

- Supplied in SysBASIC Core Bundle
- Implements a Multi-Master AMBA AHB Bus Fabric
- Up to 3 AHB Masters Can Be Accommodated
- Up to 16 AHB Slave Devices Are Supported
- Automatic Stitching to AHB Slaves and Masters in CoreConsole
- Supports Swapping (or remapping) of Slave Slots 0 and 1 to Facilitate Processor Boot

Benefits

- Allows Easy Inter-Connection of AHB Masters and Slaves in a Subsystem
- Devices Can Be Automatically Connected to CoreAHB Using the Auto Stitch Feature in CoreConsole, which Allows for Rapid System Development
- Compatible with CoreMP7 and Cortex™-M1

Supported Device Families

- Fusion
- IGLOO™
- IGLOOe
- ProASIC®3L
- ProASIC3
- ProASIC3E

Synthesis and Simulation Support

- Synthesis: Synplicity®
- Simulation: Model*Sim*

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreAHB implements a multi-master AHB bus fabric. Up to 3 masters and 16 slaves can be connected to CoreAHB. A block diagram of CoreAHB is shown in Figure 1. Each AHB slave slot is allocated 256 megabytes of memory space and all slave slots are accessible from each master connection.

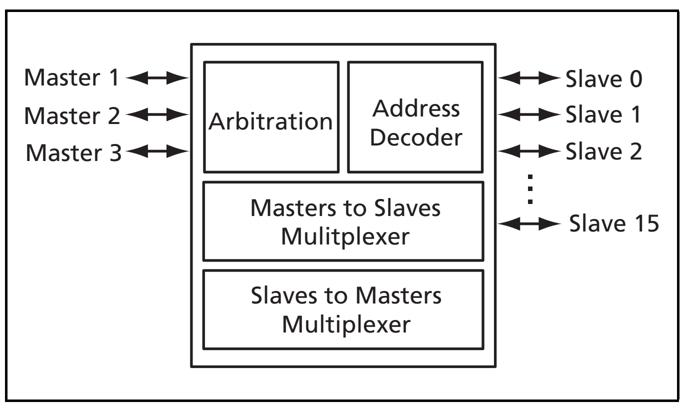

Figure 1 • **CoreAHB Block Diagram**

Arbitration Scheme

While three masters may be connected to CoreAHB, only one master can have control of the bus at any one time. An arbitration mechanism is included in CoreAHB to control access to the bus by the masters.

In addition to the 3 master connections previously mentioned, there is also a dummy master contained within CoreAHB. The dummy master never performs real transfers, but only issues IDLE transfers if granted. There is a request input (HBUSREQM0) for the dummy master that can be connected to a "pause" signal to request that no other masters are granted control of the bus.

CoreAHB contains a fixed, priority-based, arbitration scheme that supports three AHB bus masters as well as the dummy master. The priority allocation is as follows:

- Master 3 has the highest priority
- Master 0 (dummy master) has the second highest priority
- Master 2 has the middle priority
- Master 1 has the lowest priority and is the default bus master. The main subsystem processor (such as CoreMP7) is normally connected to this master connection.

Dummy Master

The master 0 slot is reserved for the dummy bus master. The dummy master does not perform real transfers. It is granted under the following conditions:

- When the previously granted master is performing a locked transfer that has received a SPLIT response
- When the default master receives a SPLIT response and no other master is requesting the bus
- When all masters have received SPLIT responses

Remapping

CoreAHB has an input named "Remap," which when asserted (high) causes slave slots 0 and 1 to be swapped from the masters' point of view. Typically, memory resources such as Flash and RAM will be connected to slots 0 and 1. The Remap input provides a means of altering the memory map. For example, it may be necessary to boot from a nonvolatile memory at power-up and then subsequently to boot from RAM.

The Remap input can be driven by CoreRemap or by an external source. When generating a subsystem containing CoreAHB in CoreConsole, the Remap input will automatically be tied low (inactive) if no connection is made to it.

Connecting CoreAHB in CoreConsole

Table 1 lists the connections present on CoreAHB and describes how to connect these in CoreConsole.

Table 1 • **CoreAHB Bus Connections**

Connection	CoreConsole Label	Description
HCLK	HCLK	AHB system clock input Connect this to the HCLK output of the bus master.
HRESETn	HRESETn	Active low AHB system reset Connect this to the HRESETn output of the bus master.
Remap	Remap	This input can be used to modify the memory map. When high, mirrored slave slots 0 and 1 are swapped. This is intended to provide a means of altering the memory map after boot-up. This input is tied low if no connection is made to it.
AHB master 0 request	HBUSREQM0	Request input for master 0 (dummy master). This input may be driven by a "pause" signal to request that no other masters are granted. This input will be tied low (inactive) if no connection is made to it.
AHB master 0 lock	HLOCKM0	Lock input for master 0 (dummy master). This input will be tied low (inactive) if no connection is made to it.
AHB master 0 grant	HGRANTM0	Grant indication output for master 0 (dummy master). When high, the dummy master is driving (IDLE) transfers on the AHB bus.

Table 1 • **CoreAHB Bus Connections (Continued)**

Connection	CoreConsole Label	Description
AHB mirrored master 1 interface	AHBmmaster1	Connection for lowest priority, default bus master
AHB mirrored master 2 interface	AHBmmaster2	Connection for middle priority bus master
AHB mirrored master 3 interface	AHBmmaster3	Connection for highest priority bus master
	AHBmslave0	AHB mirrored slave 0 interface Normally connected to AHBslave_base interface of Memory Controller
	AHBmslave1	AHB mirrored slave 1 interface
	AHBmslave2	AHB mirrored slave 2 interface
	AHBmslave3	AHB mirrored slave 3 interface
	AHBmslave4	AHB mirrored slave 4 interface
	AHBmslave5	AHB mirrored slave 5 interface
	AHBmslave6	AHB mirrored slave 6 interface
	AHBmslave7	AHB mirrored slave 7 interface
	AHBmslave8	AHB mirrored slave 8 interface
	AHBmslave9	AHB mirrored slave 9 interface
	AHBmslave10	AHB mirrored slave 10 interface
	AHBmslave11	AHB mirrored slave 11 interface
	AHBmslave12	AHB mirrored slave 12 interface
	AHBmslave13	AHB mirrored slave 13 interface
	AHBmslave14	AHB mirrored slave 14 interface
	AHBmslave15	AHB mirrored slave 15 interface

CoreAHB Port List

Table 2 on page 4 lists the ports present on the AHB Bus component. Seven groups of signals can be identified.

1. Common AHB system signals (clock and reset)
2. Remap input
3. AHB mirrored master 0 (dummy master) related connections
4. Signals common to mirrored master interfaces 1 to 3
5. AHB mirrored master signals specific to each master
6. Signals common to all 16 AHB mirrored slave interfaces
7. AHB mirrored slave (master) signals specific to each slave

Table 2 • **CoreAHB Port List**

Signal	Direction	Description
Common AHB System Signals		
HCLK	Input	Bus clock. This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Input	Reset. The bus reset signal is active low and is used to reset the system and the bus. This is the only active low AHB signal.
Remap Signal		
Remap	Input	Provides a means of altering the memory map. Slave slots 0 and 1 are swapped when this input is high.
Mirrored AHB Master 0 (dummy master) Interface		
HBUSREQM0	Input	Request input for master 0 (dummy master). This input may be driven by a "pause" signal to request that no other masters are granted. This input will be tied low (inactive) if no connection is made to it.
HLOCKM0	Input	Lock input for master 0 (dummy master). This input will be tied low (inactive) if no connection is made to it.
HGRANTM0	Output	Grant indication output for master 0 (dummy master). When high, the dummy master is driving (IDLE) transfers on the AHB bus.
Common AHB Mirrored Master Signals		
HRDATA [31:0]	Output	32-bit data to masters
HREADY	Output	Transfer done. When high, the HREADY signal indicates that a transfer has finished on the bus. This signal can be driven low to extend a transfer.
HRESP[1:0]	Input	Transfer response. This indicates an Okay Error Retry, or Split response.
Master-Specific Mirrored AHB Master Signals		
HADDRMx[31:0]	Input	32-bit master address bus (x = 1 to 3)
HTRANSMx [1:0]	Input	Transfer type (x = 1 to 3). Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITEMx	Input	Transfer direction (x = 1 to 3). When high, this signal indicates a write transfer; and when low, a read transfer.
HSIZEMx [2:0]	Input	Transfer size. This indicates the size of the transfer, which can be byte (8-bit), halfword (16-bit), or word (32-bit).
HBURSTMx [2:0]	Input	Burst type (x = 1 to 3). This indicates if the transfer forms part of a burst.
HPROTMx [3:0]	Input	Protection control (x = 1 to 3). These signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a Supervisor mode access or User mode access.
HWDATAMx [31:0]	Input	32-bit data from master (x = 1 to 3)

Table 2 • **CoreAHB Port List**

Signal	Direction	Description
Common AHB Mirrored Slave Signals		
HADDRS[31:0]	Output	This is the 32-bit system address bus.
HTRANSS[1:0]	Output	Transfer type. Indicates the type of the current transfer: 00 – Idle 01 – Busy 10 – Non-Sequential 11 – Sequential
HWRITES	Output	Transfer direction. A write transfer is indicated when this signal is high and a read transfer is indicated when this signal is low during the address phase of an AHB transfer.
HSIZES[2:0]	Output	Transfer size. Indicates the size of the transfer, which can be any of the following: 00 - byte (8-bit) 01 - halfword (16-bit) 10 - word (32-bit).
HBURSTS[2:0]	Output	Burst type. This indicates whether or not the transfer forms part of a burst.
HPROTS[3:0]	Output	Protection control. These signals indicate whether the transfer is an opcode fetch or data access, and whether the transfer is a Supervisor mode access or User mode access.
HWDATAS[31:0]	Output	32-bit data to the slave
HREADYS	Output	Transfer done. Out to the slaves (alias of HREADY)
Slave-Specific Mirrored Slave Signals		
HSELx	Output	Select of slave x (where x is a integer between 0 and 15)
HRDATASx[31:0]	Input	32-bit read data from slave x
HREADYSx	Input	Ready signal from slave x. When high, this indicates that slave has completed a transfer and is ready for another transfer.
HRESPSx[1:0]	Input	Transfer response from slave x which can be: 00 – Okay 01 – Error 10 – Retry 11 – Split

Resource Requirements

The utilization for CoreAHB in a Fusion, IGLOO, ProASIC3L, or ProASIC3/E device is 1,300 tiles.

Ordering Information

CoreAHB is included in the SysBASIC core bundle that is supplied with the Actel CoreConsole IP Deployment Platform tool. The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreAHB cannot be ordered separately from the SysBASIC core bundle.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v2.1)	Page
v2.0	The "Supported Device Families" section was updated to include ProASIC3L.	1
	The "Resource Requirements" section was updated to include ProASIC3L.	5
Advanced v0.1	The "Product Summary" section was updated to include Cortex-M1 and IGLOO/e information.	1
	Table 1 • CoreAHB Bus Connections was updated to change CoreMP7Bridge to bus master for HCLK and HRESETn.	2

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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