Austria Mikro Systeme International AG

ASCell3911

ISM 868 MHz, 433 MHz and 315 MHz FSK Transmitter

Preliminary Data Sheet

Key Features

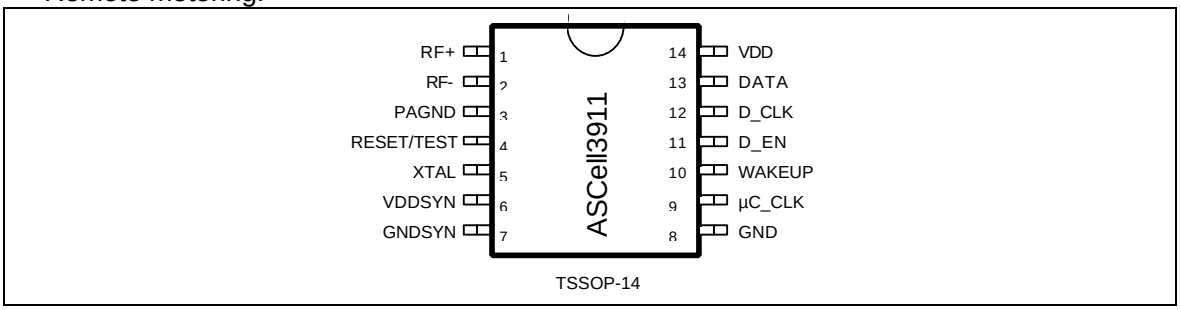
- Supports triple band operation: Europe 868 MHz and 433 MHz-, US and Japan 315 MHz ISM band.
- Designed to be conform to EN 300 220, and FCC 47 CFR Ch.1 par.15 requirements.
- Provides highly reliable packet oriented data transmission in blocks of 128 bit.
- Event oriented single message transmission and status oriented and continuous message transmission supported.
- Special transmission protocol for high reliability even in presence of burst interferer (e.g. GSM) implemented.
- Supports clock for an external µC and allows clock free total shut down of the whole system.
- Wide supply range between 2,2 to 3,5 V.
- Low TX current, typical 8,5 mA @ 2,2 V.
- Low standby current, typical 0,5 µA.
- Wide operating temperature range from –40 °C to +85 °C.
- Only a low cost XTAL for 25 ppm (868 MHz) or 50 ppm (433 and 315 MHz) reference frequency tolerance required.
- Typically only 1 XTAL, 4 capacitors and 2 inductors externally required.

General Description

The ASCell3911 is a low power, triple ISM band (868 / 433 / 315 MHz), single channel FSK transmitter designed to work in a remote control link together with the SC3912 receiver system cell.
The ASCell3911 performs packet oriented data transmission, in a single message- or continuos-message mode using a special protocol to ensure high reliability even in presence of strong pulsed interferers in close adjacent bands like e.g. GSM.
It contains a general bi-directional five line micro-controller (µC) interface to support the µC with clock- and reset- signal and to operate the highly efficient power up/down management including. This allows e.g. a clock-free total shut-down of the whole transmitter system.
As external components the ASCell3911 need only a reference XTAL, 4 capacitors and up to 2 inductors.

Applications

- Key-less car entry systems.
- Short-range packet oriented data transmission.
- Security applications and alarm systems.
- Domestic remote control systems.
- Industrial remote control systems.
- Remote metering.



TSSOP-14

This pin-out is preliminary and will change for the real implementation!

1 Functional Description

The ASCell3911 consists at the RF side of a reference XTAL oscillator, a single channel RF-synthesizer, an I/Q based direct conversion FSK modulator, a driving amplifier. On the digital side the pulse interference resistant protocol encoder and a µC interface, including microprocessor clock divider and a sophisticated power up/down circuitry are implemented.

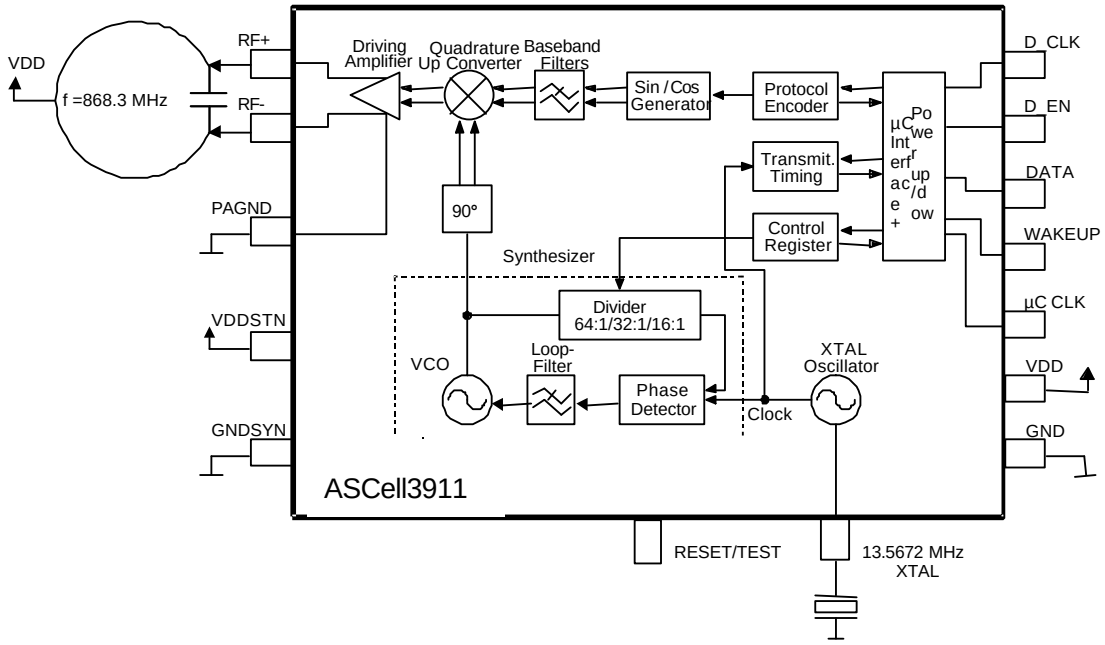


Figure 1: Block diagram of the ASCell3911.

1.1 RF Synthesizer

Frequency synthesis is performed by a single channel synthesizer, consisting of a phase detector, a charge pump, a voltage-controlled oscillator (VCO), and a feedback divider. The VCO is working at 315,000 to 868,300 MHz. The feedback divider divides by 16 (315,00 MHz), 32 (433,920 MHz) or 64 (868,300 MHz). The different ISM bands are selected by different XTAL frequency values F_{XOSC} and the CRYSTAL and RANGE control bits. A truth table for the selection of the different frequencies is given in Table 1.

F_{XOSC} / MHz	Multiplier	CRYSTAL	RANGE	F_C/ MHz
19,6875	16	H	L	315,000
13,5600	32	L	L	433,920
13,5672	64	L	H	868,300
not used		H	H	not used

Table 1: Quartz and RF output frequencies.

Note: CRYSTAL and RANGE are bits of the control information.

1.2 Microprocessor Clock

The microprocessor clock frequency F_{CLK} is generated by dividing the XTAL frequency F_{XOSC} by 4 if CRYSTAL is ´L´ and by dividing the XTAL frequency F_{XOSC} by 6 if CRYSTAL is ´H´.

Note: CRYSTAL is one bit of the control information.

1.3 Modulation

The SC3011 uses FSK modulation with a frequency deviation of ≈60 kHz at a gross data rate from 18,25 kbit/s for the 868,300 MHz ISM band.
In the transmitter, the data from the pulse interference resistant protocol encoder is first transformed into a complex base-band signal in the sin/cos block. After filtering it is shifted up to RF in an I/Q based direct conversion transmitter.

1.4 Burst interference Resistant Protocol Encoder

In order to avoid disturbance due to pulsed interferes, e.g. GSM phones, the net data block is encoded with a special protocol. Up to two simultaneous GSM disturbers can be handled by adding redundancy to the FSK data in a suitable manner.
The 128 bits of a message (net data block) are put into a transmission sequence that alternates a synchronization packet and data packet at transmission as shown in Figure 2.
To form a data packet, the 128 bit net data the information is split in 16 bytes where a bytenumber and a parity is added to generate 14 bit words. Therefore the 128 bits of net data are expanded to the 224 bit long (gross) data packet. The synchronization packet is simple 0101-sequence of 252 bit.

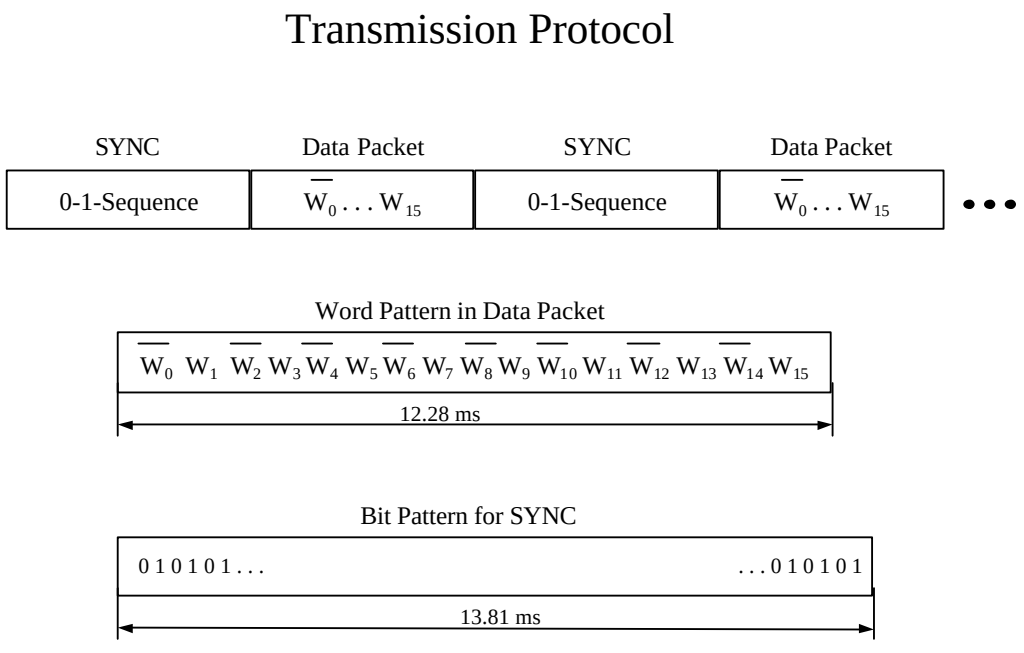


Figure 2: Transmission protocol of the ASCell3911.

1.4.1 Duty-Cycle Operation

In certain countries, it is required to reduce the average transmit power but it is allowed to keep the peak power high. Therefore a duty-cycled operation mode is implemented in the ASCell3911. By selecting this operation mode, the duty cycle of the transmit signal is set to 50%, related to an observation interval of 10 ms. This function is be implemented in the burst interference resistant protocol encoder. The duty cycle operation is set via the bit duty cycle operation (DCO).

Note: DCO is one bit of the control information.

1.4.2 Transmission Modi

The ASCell3911 supports two different transmission modii:

- The event oriented Single Message Transmission (SMT) where four times alternate synchronization and data packets are transmitted. Due to the limited transmission time this mode needs less power than CMT but supports no direct information about the duration of a transmitted command. The bit SMT/CMT is “L” for this mode.

- The status oriented Continuous Message Transmission (CMT) where alternate synchronization and data packets are transmitted as long as one button is pressed. This mode is less power efficient than SMT but the duration of a command can be directly transported by the duration of the transmission power. The bit SMT/CMT is “H” for this mode.

Note: SMT/CMT is one bit of the control information.

1.5 Driving Amplifier

The driving amplifier has a differential open collector output optimized for driving of small, symmetrical high-impedance loop antennas. The amplifier drives a nominal RF current of 1 mA_{RMS}. The maximal differential voltage swing is about 2,8 V_{PP}. Therefore, the output power is a function of the connected load impedance. With a 2 kΩ differential load a nominal peak output power (to the antenna) of ≈2 mW is obtained. Please note that the finally radiated power (from antenna) is lower and strongly dependent on the efficiency (function of the size) of the antenna to be used.

1.6 µC Interface and Power Management

The ASCell3911 contains a direct interface to a micro controller (µC). The µC interface of the ASCell3911 consists of the following five pins:

”Transmit data input” (DATA).

“Active ”H” transmit data enable” (D_EN).

”Transmit data clock input” (D_CLK).

”Active ”L” µC reset output/transmitter wakeup end input” (WAKEUP).

”µC clock output/active ”L” start-up input” (µC_CLK).

These lines support the µC with the required reset and clock signals and control the ASCell3911 internal power on/off circuit, which wakes up and shuts down the whole transmitter consisting of the ASCell3911 and the µC.

Figure 3 shows a typical interconnection of the ASCell3911 with a typical µC. Figure 4 presents a related timing for power up and down of the transmitter.

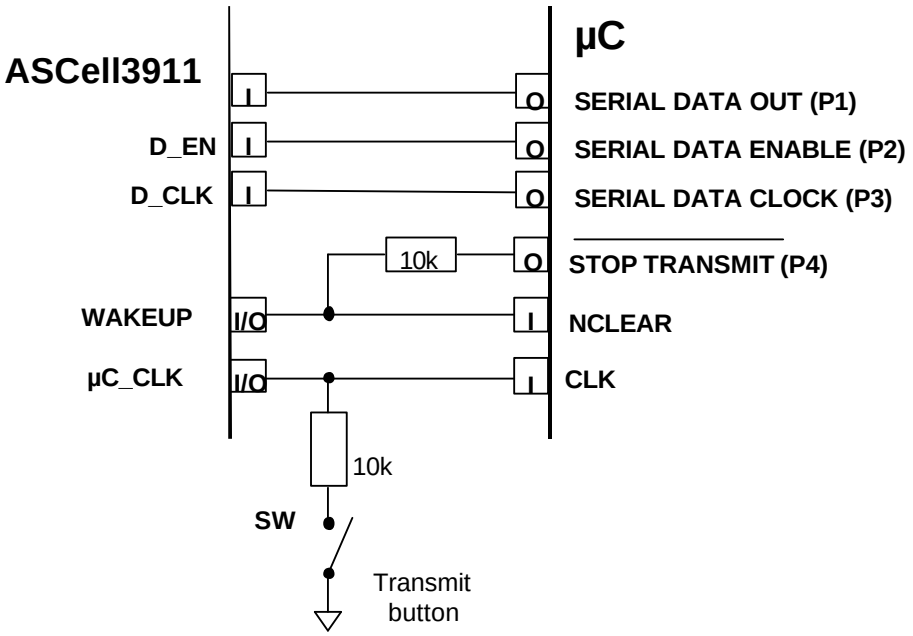


Figure 3: Interconnection of the ASCell3911 with a typical µC with one button to wake up the whole system (example).

Note: At room temperature, resistor values of ≈10 kΩ are suggested for the µC interface.

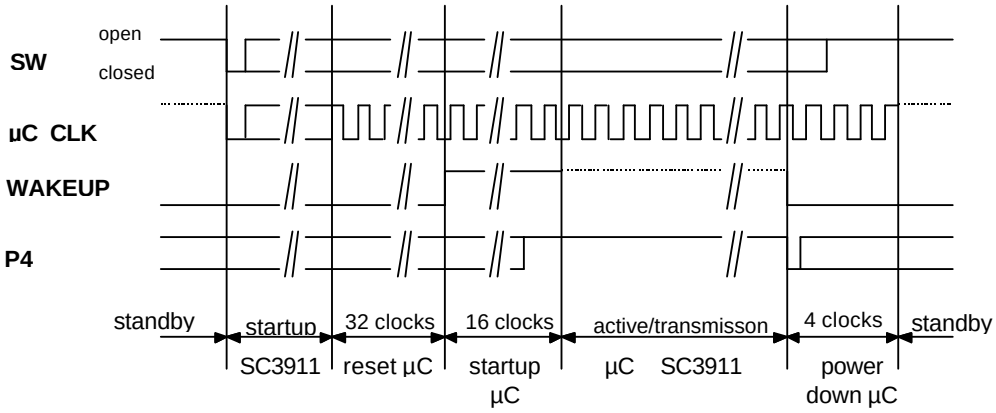


Figure 4: µC interface timing for wake-up and power down control.

Note: The dashed lines indicate weak high or low state when the µC_CLK or WAKEUP output of the ASCell3911 is disabled (in high-resistive Z state) and pulled "H" or "L" by the internal pull-up device or by the µC via a resistor. These weak states can be overridden by the ASCell3911 if the respective outputs are enabled. Whenever a line is pulled via an external resistor, however, this should override the internal pull-up devices of the ASCell3911.

1.6.1 Interface Description

It is assumed that the µC remains in low power standby mode as long as the P4 pin is kept "L" and no clock cycles are applied.

Standby: During standby (default after V_{CC}-on) the XTAL oscillator is turned off and ASCell3911 holds the µC in a reset state:

The ASCell3911 WAKEUP pin is active and set to ”L”, holding the µC in reset state. In standby mode the ASCell3911 WAKEUP internal pull-up is disabled and does not drain current from the supply.
The ASCell3911 µC_CLK output is disabled, (in high resistive ”Z” state) and internally pulled up to ”H”.
(Re)starting the transmitter: Closing the push button (giving a falling edge on µC_CLK line) starts up the ASCell3911. It turns on its XTAL oscillator and after the oscillator start up phase it turns the µC_CLK pin to active (CMOS level) mode and provides a clock to the µC.
After a delay of 32 µC clock cycles the WAKEUP pin of the ASCell3911 is set to ”H” for 16 clock cycles. The transmitter is now in active mode. The WAKEUP acts in ASCell3911 active mode as an input waiting for a ”L” to trigger the transmission of the transmitter to standby mode
During this active mode the µC sends the 132 bit data (8 bit control and 16 * 8 bit data) on the µC - P1 (Serial data out) line.
The timing of the microcontroller interface is shown in Figure 5. The microcontroller clocks a 134-bit *Data* into the ASCell3911 for data encoding. This data consists of 6 *control* bits followed by 128 transmit *data* bits. After the data bock has been completely transferred to the AS-Cell3911, it starts up transmission, during which the I/Q modulator and power amplifier are powered up in order to transmit the encoded data. Transmission is done with respect to the control bits. Table 2 shows the control bits set different operation modes of the chip.

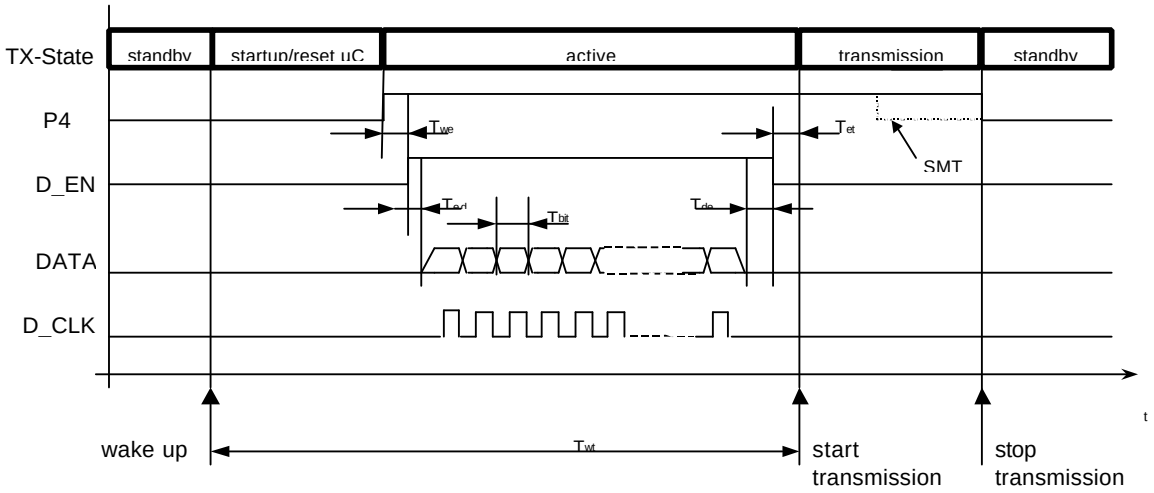


Figure 5: µC interface timing for data transmission when ASCell3911 and µC are active.

Note: Figure 4 shows the timing for the CMT-mode where the controller sets P4 to “L” and so the transmission stops. The broken line shows the Signal P4 in the SMT mode where the ASCell3911 stops the transmission.

Control bit description:

bit#	Name	Comments
1	Quartz crystal (“CRYSTAL”):	L=13,5600 / 13,5672MHz H=19,6875 MHz
2	Operating frequency range (“RANGE”):	L=315/433MHz, H=868,3MHz
3	Duty cycle operation (“DCO”)	L = OFF H = ON
4	Single / Continuous Message Transmission (“SMT/CMT”)	L = SMT H = CMT

5	GP	
6	GP	

Table 2: Control bit description.

Single message transmission: After completing the data transmission to the ASCell3911, the µC may indicate ”end of transmission” by setting P4 (not end of transmit) to ”L” and pulls the WAKEUP line to ”L”. Sensing this, 4 clock cycles later the ASCell3911 will switch the µC back to standby mode, disabling the µC_CLK output, setting the active WAKEUP pin to ”L”. The AS-Cell3911 will finish the transmission sequence and than turning off the XTAL oscillator to and goes back to the standby mode too. The SMT/CMT bit is ”L” indicates the single transmission mode.
Note: SMT/CMT is one bit of the control information.

Continuous message transmission: After completing the data transmission to the AS-Cell3911, the µC may indicate ”end of transmission” by setting P4 to ”L” and pulls the WAKEUP line to ”L”. Sensing this, 4 clock cycles later the ASCell3911 will switch back to standby mode, disabling the µC_CLK output, setting the active WAKEUP pin to ”L” and than turning off the XTAL oscillator. The SMT/CMT bit is ”H” indicates the continuous transmission mode.
Note: SMT/CMT is one bit of the control information.

Due to the sophisticated tri-state - active/inactive pull-up configuration of the WAKEUP pin the ASCell3911 does not drain current during its standby periods.
The interface implemented in the ASCell3911 system cell is a general, non-specialized example only. It can be modified on customers demand.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings (non operating)

Symbol	Parameter	Min	Max	Units	Note
VDD; VDDSYN	Positive supply voltage	-0,5	6	V	
GND; GNDSYN	Negative supply voltage	0	0	V	
Vin	Voltage at every input pin	Gnd-0,5	VCC+0,5	V	
Iin	Input current into any pin except supply pins	-10	10	mA	Latch-up Test
ESD	Electrostatic discharge		1k	V	1) 3)
ESD_{IN}	Electrostatic discharge of RF pins		500	V	1) 4)
Tstg	Storage temperature	-55	125	°C	
Tlead	Lead temperature		260	°C	2)

1) Test according to MIL STD 883C, Method 3015.7. HBM: R=1,5 kΩ, C=100 pF, 5 positive pulses per pin against supply pin(s), 5 negative pulses per pin against supply pin(s).
2) 260 °C for 10 s (Reflow and Wave Soldering), 360 °C for 3 s (Manual soldering).
3) All pins except RF+, RF-, XTAL.
4) Pins RF+, RF-, XTAL.

2.2 Operating Conditions

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
VDD	Positive supply voltage		2,2		3,5	V
GND	Negative supply voltage		0	0	0	V
TA	Operating temperature		-40		85	°C
ICC	Current consumption	VCC= 3,5 V VCC= 3,0 V VCC= 2,2 V		10 9 8,5	12 11 10	mA mA mA
ICC_{SD}	Standby current	low voltage reset circuit active			0,5	µA

2.3 FSK Operation

TA = 23 °C, VDD, VSYN = 2,7 V, unless specified otherwise. Device functional for TA= -40 to +85 °C.

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
F_C	Carrier frequency	Depends on different external crystals.		315,000 433,920 868,300		MHz MHz MHz
ΔF	FSK frequency deviation	315,000 MHz: 433,920 MHz: 868,300 MHz:	-68,4 -61,7 -61,7		+68,4 +61,7 +61,7	kHz kHz kHz
F_{xosc}	Crystal oscillator (XOSC) frequency	315,000 MHz, Crystal=H 433,920 MHz, Crystal=L 868,300 MHz, Crystal=L		19,6875 13,5600 13,5672		MHz MHz MHz
FT_{xosc}	Crystal oscillator (XOSC) fequency tolerance	315,000 M: (-40~+85 °C), 433,920 MHz: (-40~+85 °C), 868,300 MHz: (-40~+85 °C)			50 50 25	ppm ppm ppm
$D_{R,gross}$	Gross data rate	Including burst protocol.		18,235[1)]		kbps
P_{out}	Available output power, into Z_{out} = 2000 Ω differential	315,000MHz (USA), 433,920 MHz 868,300 MHz 315MHz (Japan) - set through RPA???	-1,5 –1,5 –3,0	0,0 0,0 -1,5 -20?	+1,5 +1,5 +0,0	dBm dBm dBm dBm
T_{abTX}	Time between two different transmitted messages “a”&“b”		30			ms

1) @ 868,300 MHz: $D_{R,gross}$ = 13,5672 MHz / 46,5 / 16 = 18,235 kbps.
@ 433,920 MHz: 18,225 kbps.
@ 315,000 MHz: 19,226 kbps.

2) Antenna dependent - will not be production tested.

2.4 Digital Pin Characteristics

TA = 23 °C, VDD = 2,7 V, unless specified otherwise. GND is the 0 V reference.
Input parameters for bi-directional pins (µC_CLK, WAKEUP) are valid at disabled outputs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
µC_CLK (µC clock output / wake-up input)						
VOH	High level output voltage	IOH =-1 mA	VDD-0,5	-		V
VOL	Low level output voltage	IOL =1 mA		-	0,3	V
tr	Rise time	CLoad = 10 pF		20		ns
td	Fall time	CLoad = 10 pF		20		ns
jcc	Cycle to cycle jitter				+/-5	%
VIH	High level input voltage		VDD-0,5	-		V
VIL	Low level input voltage			-	0,3	V
IIH	High level input current	VIH = VDD			1	µA
IIL	Low level input current	VIL =0 V; Due to internal pull-up	-40			µA

DATA(serial data input), D_EN (serial data enable input), D_CLK (serial data clock input)						
VIH	High level input voltage		VDD-0,5	-		V
VIL	Low level input voltage			-	0,3	V
IIH	High level input current	VIH= VDD			1	µA
IIL	Low level input current	VIL =0 V	-1			µA
WAKEUP (µC clear output / transmitter power down input)						
VOH	High level output voltage	IOH = -1mA	VDD-0,5	-		V
VOL	Low level output voltage	IOL = 1mA		-	0,3	V
VIH	High level input voltage		VDD-0,5	-		V
VIL	Low level input voltage			-	0,3	V
IIH	High level input current	VIH = VDD			1	µA
IIL	Low level input current	VIL =0 V; Due to internal pull-up	-40			µA

2.4.1 µController Interface

Symbol	Parameter	Conditions / Notes	Min	Typ	Max	Units
T_{bit}	FSK Data Bit duration				tbd	s
T_{we}	Time between Wake up and Data Enable	Data input prepared to receive data	tbd			s
T_{ed}	Time between Data Enable and Data	Data input prepared to receive data	tbd			s
T_{de}	Time between Data and Data Enable	Start-up and lock PLL	tbd			s
T_{et}	Time between Data Enable and Transmit	Start-up and lock PLL	tbd			s
T_{wt}	Time between Wake up and Transmit start				tbd	s
T_{ca}	Time that CLK output stays active after T_{wt}			tbd		s
V_{POR}	Power-On-Reset threshold voltage	RESET invalid when Vdd < $VCCmin_{POR}$	1,6		1,8	V
T_{POR}	Power-On-Reset duration		2		10	ms
$VCCmin_{POR}$	Minimum Supply Voltage for valid Power-On-Reset output				1,2	V

3 Pin Description

Note: pin ordering is preliminary - will be fixed at fab-in.

Pin	Name	Type	Description
1	RF+	A	Power amplifier output (open collector)
2	RF-	A	Power amplifier output (open collector)
3	PAGND	P	Power amplifier ground

Pin	Name	Type	Description
4	RESET / TEST	O	Power-On-Reset output Test output in test mode
5	XTAL	A	XTAL oscillator input
6	VDDSYN	P	PLL, mixer positive supply
7	GNDSYN	P	PLL, mixer, negative supply
8	GND	P	Negative supply of DC/DC, POR, LBAT, XOSC, Data Interface, SinCos
9	uC_CLK	O	Clock output for micro-controller
10	WAKEUP	I	Wake-up signal, pos. edge wakes up the chip, negative edge stops transmission
11	D_CLK	I	Data clock, data is clocked into the chip with negative edge of DCLK
12	D_EN	I	Data enable, high while data is clocked into the chip
13	DATA	I	Data input for 128 bits of FSK data preceeded by 8 control bits
14	VDD	P	Positive supply of DC/DC, POR, LBAT, XOSC, Data Interface, SinCos

4 Application Schematic

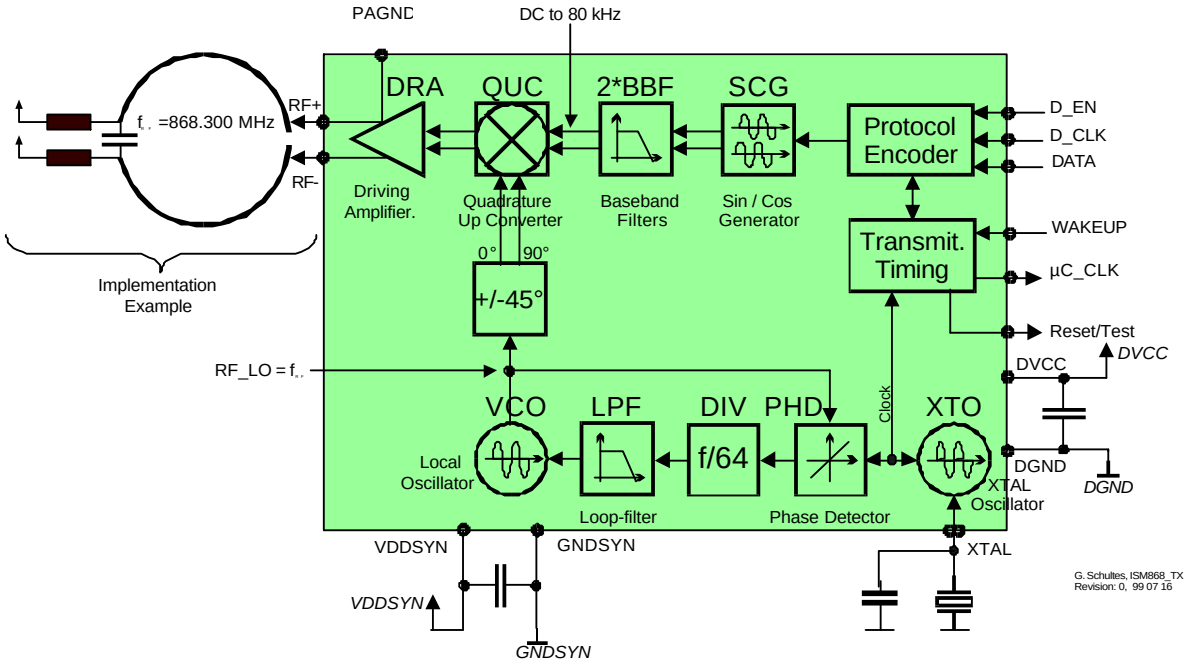


Figure 6: Basic application schematic of the ASCell3911.

5 Package Information

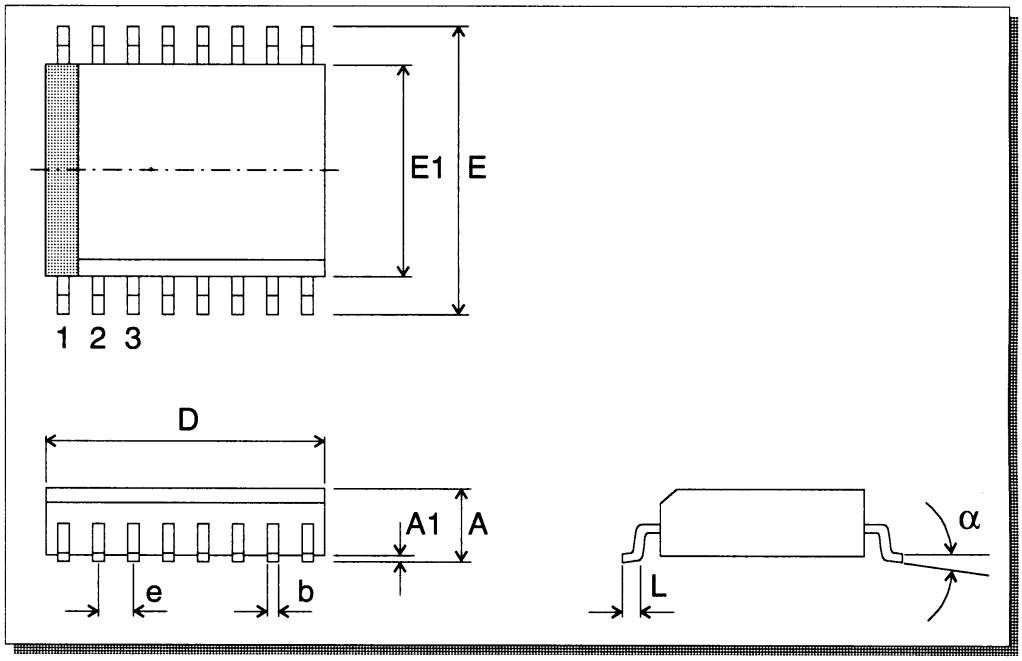


Figure 7: Physical dimensions of TSSOP-14.

Symbol	Common Dimensions		
	Minimal (mm/mil)	Nominal (mm/mil)	Maximal (mm/mil)
A	-	-	1,10/0,0433
A1	0,05/0,002	0,10/0,004	0,15/0,006
b	0,19/0,0075	-	0,30/0,0118
D			
e	0,65 BSC		
E	6,25/0,246	6,40/0,252	6,50/0,256
E1	4,30/0,169	4,40/0,173	4,50/0,177
L	0,50/0,020	0,60/0,024	0,70/0,028
α	0°	4°	8°

ASCell's are functional and in-spec circuits, which are usually available as samples with documentation and demoboard. However they are intentionally to be used as a basis for ASIC derivatives. If an ASCell fits into a customer's application as it is, it will be immediately qualified and transfered to an ASSP to be ordered as a regular AS product.