

### Preliminary Specification

### PRODUCT SPECIFICATION

#### Product Description

The aSC7611 has a two wire digital interface compatible with SMBus 2.0. Using a 10-bit  $\Sigma\Delta$ - ADC, the aSC7611 measures the temperature of two remote diode connected transistors as well as its own die.

Using temperature information from these three zones, an automatic fan speed control algorithm is employed to minimize acoustic impact while achieving recommended CPU temperature under varying operational loads.

To set fan speed, the aSC7611 has three independent pulse width modulation (PWM) outputs that are controlled by one, or a combination of three, temperature zones. Both high- and low-frequency PWM ranges are supported. The aSC7611 also includes a digital filter that can be invoked to smooth temperature readings for better control of fan speed and minimum acoustic impact. The aSC7611 has tachometer inputs to measure fan speed on up to four fans. Limit and status registers for all measured values are included to alert the system host that any measurements are outside of programmed limits via status registers.

System voltages of VCCP, 2.5V, 3.3V, 5.0V, and 12V motherboard power are monitored efficiently with internal scaling resistors.

#### Features

- 2-wire, SMBus 2.0 compliant, serial interface
- 10-bit  $\Sigma\Delta$ -ADC
- Monitors internal and remote thermal diodes
- Monitors VCCP, 2.5V, 3.3V, 5.0V, and 12V motherboard/processor supplies
- Programmable autonomous fan control based on temperature readings
- Noise filtering of temperature reading for fan control
- 0.25°C digital temperature sensor resolution
- 3 PWM fan speed control outputs for 2-, 3- or 4-wire fans.
- Provides high and low PWM frequency ranges
- 4 fan tachometer inputs
- Monitors 5 VID control lines
- 24-Lead QSOP package
- XOR-tree test mode

#### Measurement System

Temperature:

- 0.25°C resolution,  $\pm 2^\circ\text{C}$  accuracy on remote diode
- 0.25°C resolution,  $\pm 3^\circ\text{C}$  accuracy on local sensor
- Temperature measurement range on remote sensor  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  using 2's complement coding.

Voltage:

- 10-bit Resolution,  $\pm 2\%$  of Full Scale

Fan Tachometer:

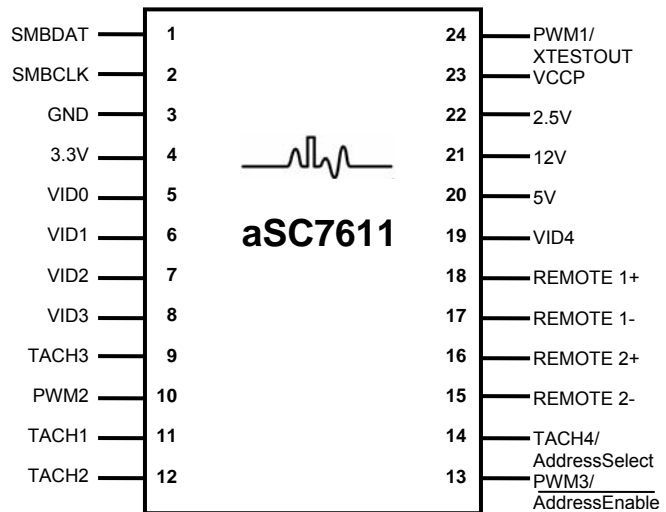
- 16-bit count of 90kHz clock periods

Limit alarms for all measured values

#### Applications

- Desktop Computers – Motherboards and Graphics Cards
- Laptop Computers
- Microprocessor based equipment (e.g. Base-stations, Routers, ATMs, Point of Sales)

#### Connection Diagram



#### Ordering Information

Part Number	Package	Temperature Range and Operating Voltage	Marking	How Supplied
aSC7611QS24	24-lead QSOP	0°C to +120°C, 3.3V	aSC7611 Ayww	2500 units Tape & Reel

*Ayww – Assembly site, year, workweek*

Block Diagram

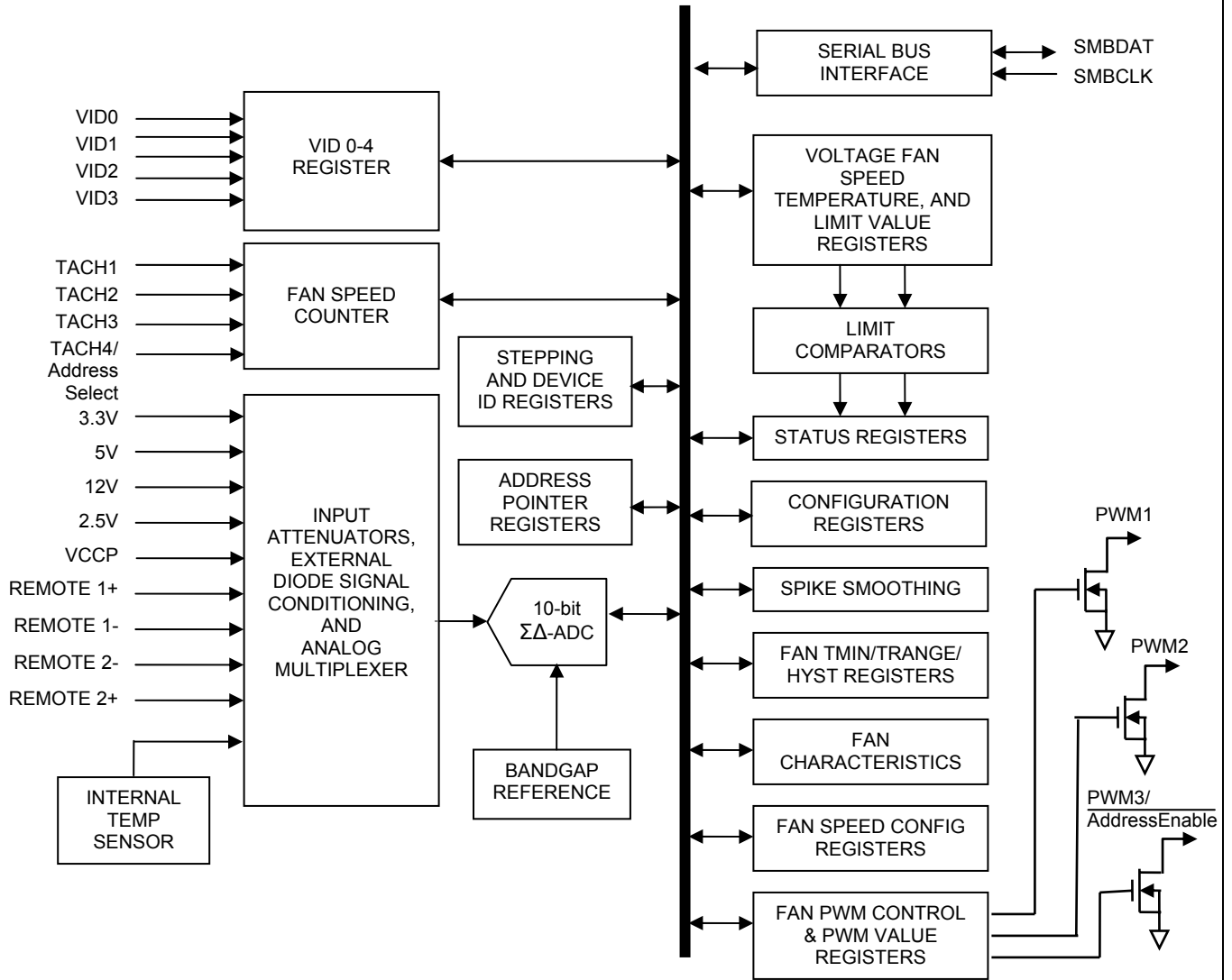


Figure 1 Block Diagram

Preliminary Specification – Subject to change without notice

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**Pin Descriptions**

	Symbol	Pin	Type	Name and Function/Connection
<b>SMBus</b>	SMBDAT	1	Digital I/O (Open-Drain)	System Management Bus Data. Open-drain output. 5V tolerant, SMBus 2.0 compliant.
	SMBCLK	2	Digital Input	System Management Bus Clock. Tied to Open-drain output. 5V tolerant, SMBus 2.0 compliant.
<b>Processor VID Lines</b>	VID0	5	Digital Input	Voltage identification signal from the processor. This value is read in VID0-VID4 Status Register.
	VID1	6	Digital Input	Voltage identification signal from the processor. This value is read in VID0-VID4 Status Register.
	VID2	7	Digital Input	Voltage identification signal from the processor. This value is read in VID0-VID4 Status Register.
	VID3	8	Digital Input	Voltage identification signal from the processor. This value is read in VID0-VID4 Status Register.
	VID4	19	Digital Input	Voltage identification signal from the processor. This value is read in VID0-VID4 Status Register.
<b>Power</b>	3.3V	4	POWER	+3.3V pin. Can be powered by +3.3V Standby power if monitoring in low power states is required. This pin should be bypassed with a 0.1 $\mu$ F capacitor in parallel with 100pF. A bulk capacitance of approximately 10 $\mu$ F needs to be in near vicinity of the aSC7611.
	GND	3	GROUND	Ground for all analog and digital circuitry.
<b>Voltage Inputs</b>	5V	20	Analog Input	Analog Input for +5V monitoring.
	12V	21	Analog Input	Analog Input for +12V monitoring.
	2.5V	22	Analog Input	Analog Input for +2.5V monitoring..
	VCCP	23	Analog Input	Analog Input for VCCP (processor voltage) monitoring.
<b>Remote</b>	Remote 1+	18	Remote Thermal Diode Positive Input	Positive input (current source) from the first remote thermal diode Serves as the positive input into the A/D. Connected to THERMDA pin of Pentium processor.
	Remote 1-	17	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode Serves as the negative input into the A/D. Connected to THERMDC pin of Pentium processor.
	Remote 2+	16	Remote Thermal Diode Positive Output	Positive input (current source) from the first remote thermal diode Serves as the positive input into the A/D. Connected to the base of a diode connected MMBT3904 NPN transistor.
	Remote 2-	15	Remote Thermal Diode Negative Input	Negative input (current sink) from the first remote thermal diode Serves as the negative input into the A/D. Connected to the emitter of a diode connected MMBT3904 NPN transistor.
<b>Fan Tachometer Inputs</b>	TACH1	11	Digital Input	Input for monitoring tachometer output of fan 1.
	TACH2	12	Digital Input	Input for monitoring tachometer output of fan 2.
	TACH3/AddressEnable	9	Digital Input	Input for monitoring tachometer output of fan 3. During power-up, if held low through a 10K $\Omega$ resistor, SMBus address may be selected based on the state of TACH4 pin.
	TACH4/AddressSelect	14	Digital Input	Input for monitoring tachometer output of fan 4. If in Address Select Mode, determines the SMBus address of aSC7611.

	Symbol	Pin	Type	Name and Function/Connection
Fan Control	PWM1/XTESTOUT	24	Digital Open-Drain Output	Fan speed control 1. When in XOR tree test mode, functions as XOR Tree output.
	PWM2	10	Digital Open-Drain Output	Fan speed control 2.
	PWM3/Address Enable	13	Digital Open-Drain Output	Fan speed control 3. Pull to ground at power on to enable Address Select Mode (Address Select pin controls SMBus address of the device).

### Absolute Maximum Ratings<sup>1</sup>

Parameter	Rating	
Supply Voltage, $V_{DD}$	-0.5V to 6.0V	
Voltage on Any Digital Input or Output Pin	-0.5V to 6.0V	
Voltage on 12V Analog Input	-0.5V to 16V	
Voltage on 5V Analog Input	-0.5V to 6.6V	
Voltage on Remote 1 +, Remote 2 +	-0.5V to ( $V_{DD} + 0.50V$ )	
Voltage on Other Analog Inputs	-0.5V to 6.0V	
Current on Remote 1 -, Remote 2 -	$\pm 1mA$	
Input Current on Any Pin <sup>2</sup>	$\pm 5mA$	
Package Input Current <sup>2</sup>	$\pm 20mA$	
Package Dissipation at $T_A = 25^\circ C$	See (Note 3)	
Storage Temperature	$-65^\circ C$ to $+150^\circ C$	
ESD <sup>4</sup>	Human Body Model	3000 V
	Machine Model	200 V
	Charged Device Model	1500 V

### Operating Ratings<sup>1</sup>

Parameter	Rating	
aSC7611 Operating Temperature Range, Ambient Temperature, $T_{MIN}$ to $T_{MAX}$	$0^\circ C \leq T_A \leq +120^\circ C$	
Remote Diode Temperature Range	$-55^\circ C \leq T_D \leq +125^\circ C$	
Supply Voltage (3.3V nominal)	+3.0V to +3.6V	
$V_{IN}$ Voltage Range	+12V $V_{IN}$	-0.05V to 16V
	+5V $V_{IN}$	-0.05V to 6.6V
	+3.3V $V_{IN}$	3.0V to 4.4V
VCCP and All Other Inputs	-0.05V to $V_{DD} + 0.05V$	
VID0-VID4	-0.05V to 5.5V	
All Other Inputs	-0.05V to $V_{DD} + 0.05V$	
Typical Supply Current	1.8mA	

#### Notes:

1. Absolute maximum ratings are limits beyond which operation may cause permanent damage to the device. These are stress ratings only; functional operation at or above these limits is not implied.
2. When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supplies ( $V_{IN} < GND$  or  $V_{IN} > V_{DD}$ ), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four. Parasitic components and/or ESD protection circuitry are present on the aSC7611 pins. Care should be taken not to forward bias the parasitic diode present on pins D+ and D-. Doing so by more than 50mV may corrupt temperature measurements.
3. Thermal resistance junction-to-ambient when attached to a double-sided printed circuit board with 1oz. foil is  $115^\circ C/W$
4. Human Body Model: 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin. Machine Model: 200pF capacitor discharged directly into each pin. Charged-Device Model is per JESD22-C101C.

## DC Electrical Characteristics<sup>5</sup>

The following specifications apply for  $V_{DD} = 3.0V$  to  $3.6V$ , and all analog input source impedance  $R_s = 50\Omega$  unless otherwise specified in conditions. **Boldface limits apply for  $T_A = T_J$  over  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$ .  $T_A$  is the ambient temperature of the aSC7611;  $T_J$  is the junction temperature of aSC7611;  $T_D$  is the remote thermal diode junction temperature. Specifications subject to change without notice

Parameter		Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY CHARACTERISTICS</b>						
Supply Current		Converting, Interface and Fans Inactive, Peak Current		1.8	<b>3.5</b>	mA(max)
		Converting, Interface and Fans inactive, Average Current		0.5		mA
Power-On Reset Threshold Voltage			<b>1.6</b>		<b>2.8</b>	V
<b>TEMPERATURE TO DIGITAL CONVERTER CHARACTERISTICS</b>						
Resolution				0.25 10		$^\circ C$ Bits
Remote Sensor Accuracy <sup>6</sup>		$0^\circ C \leq T_A \leq +100^\circ C$ , $0^\circ C \leq T_D \leq +100^\circ C$ , $3V \leq V_{DD} \leq 3.6V$			$\pm 2$	$^\circ C$
		$0^\circ C \leq T_A \leq +120^\circ C$ , $-55^\circ C \leq T_D \leq +125^\circ C$ , $3V \leq V_{DD} \leq 3.6V$			$\pm 3$	$^\circ C$
Temperature Accuracy using Internal Diode <sup>7</sup>		$0^\circ C \leq T_A \leq +120^\circ C$ , $3V \leq V_{DD} \leq 3.6V$		$\pm 1$	$\pm 3$	$^\circ C$
External Diode Current Source	$I_{DS}$	High Level		96		$\mu A$ (max)
		Low Level		6		$\mu A$
External Diode Current Ratio				16		
<b>ANALOG TO DIGITAL CONVERTER CHARACTERISTICS</b>						
Total Unadjusted Error <sup>8</sup>	TUE				$\pm 2$	%FS(max)
Differential Non-linearity	DNL			1		LSB
Power Supply Sensitivity				$\pm 1$		%V
Total Monitoring Cycle Time <sup>9</sup>		All Voltage and Temperature readings		182	<b>200</b>	ms (max)
Input Resistance, all analog inputs			<b>140</b>	210	<b>400</b>	k $\Omega$
<b>DIGITAL OUTPUT: PWM1, PWM2, PWM3, XTESTOUT</b>						
Logic Low Sink Current	$I_{OL}$	$V_{OL} = 0.4V$	<b>8</b>			mA (min)
Logic Low Level	$V_{OL}$	$I_{OUT} = +8mA$			<b>0.4</b>	V (max)
<b>SMBUS OPEN-DRAIN OUTPUT: SMBDAT</b>						
Logic Low Output Voltage	$V_{OL}$	$I_{OUT} = +4mA$			<b>0.4</b>	V (max)
High Level Output Current	$I_{OH}$	$V_{OUT} = V+$		0.1	<b>10</b>	$\mu A$ (max)
<b>SMBUS INPUTS: SMBCLK, SMBDAT</b>						
Logic Input High Voltage	$V_{IH}$		<b>2.1</b>			V (min)
Logic Input Low Voltage	$V_{IL}$				<b>0.8</b>	V (max)
Logic Input Hysteresis Voltage	$V_{HYST}$			300		mV
<b>DIGITAL INPUTS: ALL</b>						
Logic Input High Voltage	$V_{IH}$		<b>2.1</b>			V (min)

Parameter		Conditions	Min	Typ	Max	Units
Logic Input Low Voltage	$V_{IL}$				<b>0.8</b>	V (max)
Logic Input Threshold Voltage	$V_{TH}$			1.5		V
Logic High Input Current	$I_{IH}$	$V_{IN} = V_{+}$		0.005	<b>10</b>	$\mu A$ (max)
Logic Low Input Current	$I_{IL}$	$V_{IN} = GND$		-0.005	<b>-10</b>	$\mu A$ (max)
Digital Input Capacitance	$C_{IN}$			20		pF

### AC Electrical Characteristics

The following specifications apply for  $V_{DD} = 3.0V$  to  $3.6V$  unless otherwise specified in conditions. **Boldface limits apply for  $T_A = T_J$  over  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^{\circ}C$ .

Parameter		Conditions	Min	Typ	Max	Units
<b>TACHOMETER</b>						
Fan Full-Scale Count					<b>65535</b>	(max)
Fan Counter Clock Frequency				90		kHz
Fan Count Conversion Time				0.7	<b>1.46</b>	sec(max)
<b>FAN PWM OUTPUT</b>						
Frequency Range		Low-Frequency Range		10 94		Hz Hz
		High-Frequency Range		23 30		kHz kHz
Duty-Cycle Range					<b>0 to 100</b>	%(max)
Duty-Cycle Resolution (8-bits)				0.3906		%/count
Spin-Up Time Interval Range				0		ms
				4000		ms

### Logic Electrical Characteristics

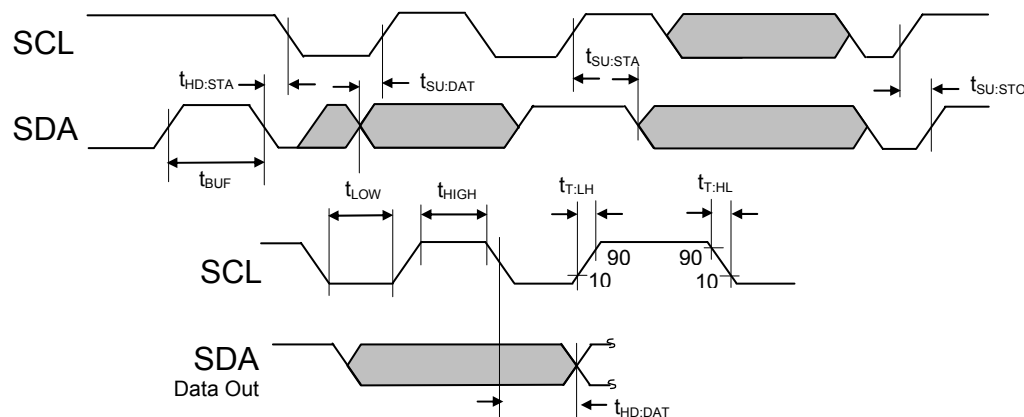
( $T_A = 25^{\circ}C$ ,  $V_{DD} = 3.3V$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Logic High	$V_{IH}$	$3V \leq V_{DD} \leq 3.6V$	2.1			V
Input Voltage Logic Low	$V_{IL}$	$3V \leq V_{DD} \leq 3.6V$			0.8	V
Input Leakage Current	$I_{IN}$	$V_{IN} = 0V$ or $5.5V$ , $0^{\circ}C \leq T_A \leq +125^{\circ}C$			$\pm 1.0$	$\mu A$
SMBus Output Sink Current	$I_{OL}$	$T_A = 25^{\circ}C$ , $V_{OL} = 0.6V$	6			mA
SMBus Logic Input Current	$I_{IH}, I_{IL}$		-1		+1	$\mu A$
Output Leakage Current	$I_{OH}$	$V_{OH} = V_{DD} = 5.5V$		0.1	1	$\mu A$
Output Transition Time	$t_F$	$C_L = 400pF$ , $I_{OL} = -3mA$			250	ns
Input Capacitance	$C_{IN}$	All Digital Inputs			5	pF

## Serial Port Timing

( $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V}$  unless otherwise noted, Guaranteed by design, not production tested)

Parameter	Symbol	Min	Typ	Max	Units
SCL Operating Frequency	$f_{\text{SCL}}$			400	kHz
SCL Clock Transition Time	$t_{\text{T:LH}}, t_{\text{T:HL}}$			300	ns
SCL Clock Low Period	$t_{\text{LOW}}$	1.3			$\mu\text{s}$
SCL Clock High Period	$t_{\text{HIGH}}$	0.6		50	$\mu\text{s}$
Bus free time between a Stop and a new Start Condition	$t_{\text{BUF}}$	1.3			$\mu\text{s}$
Data in Set-Up to SCL High	$t_{\text{SU:DAT}}$	100			ns
Data Out Stable after SCL Low	$t_{\text{HD:DAT}}$	300			ns
SCL Low Set-up to SDA Low (Repeated Start Condition)	$t_{\text{SU:STA}}$	600			ns
SCL High Hold after SDA Low (Start Condition)	$t_{\text{HD:STA}}$	600			ns
SDA High after SCL High (Stop Condition)	$t_{\text{SU:STO}}$	600			ns
Time in which aSC7611 must be operational after a power-on reset	$t_{\text{POR}}$			500	ms
SMBus Time-out before device communication interface reset <sup>10</sup>	$t_{\text{TIMEOUT}}$	25		35	ms



### Notes (cont'd):

- These specifications are guaranteed only for the test conditions listed.
- The accuracy of the aSC7611 is guaranteed when using the thermal diode of Intel Pentium 4, 65nm processors or any thermal diode with a non-ideality of 1.009 and series resistance of 4.52 $\Omega$ . When using a 2N3904 type transistor or an CPU with a different non-ideality the error band will be typically shifted depending on transistor diode or CPU characteristics. See applications section for details.
- Accuracy (expressed in  $^\circ\text{C}$ ) = Difference between the aSC7611 reported output temperature and the temperature being measured. Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the aSC7611 and the thermal resistance. See (Note 3) for the thermal resistance to be used in the self-heating calculation.
- TUE, total unadjusted error, includes ADC gain, offset, linearity and reference errors. TUE is defined as the "actual  $V_{in}$ " to achieve a given code transition minus the "theoretical  $V_{in}$ " for the same code. Therefore, a positive error indicates that the input voltage is greater than the theoretical input voltage for a given code. If the theoretical input voltage was applied to an aSC7611 that has positive error, the aSC7611's reading would be less than the theoretical.
- This specification is provided only to indicate how often temperature and voltage data is updated. The aSC7611 can be read at any time without regard to conversion state (and will yield last conversion result).
- Holding the SMBCLK lines low for a time interval greater than  $t_{\text{TIMEOUT}}$  will reset the aSC7611's SMBus state machine, therefore setting the SMBDAT pin to a high impedance state.



## Control Communication

### SMBus

The aSC7611 is compatible with devices that are compliant to the SMBus 2.0 specifications. More information on this bus can be found at <http://www.smbus.org/>. Compatibility of SMBus2.0 to other buses is discussed in the SMBus 2.0 specification.

### General Operation

Writing to and reading from the aSC7611 registers is accomplished via the SMBus-compatible two-wire serial interface. SMBus protocol requires that one device on the bus initiate and control all read and write operations. This device is called the “master” device. The master device also generates the SCL signal that is the clock signal for all other devices on the bus. All other devices on the bus are called “slave” devices. The aSC7611 is a slave device. Both the master and slave devices can send and receive data on the bus.

During SMBus operations, one data bit is transmitted per clock cycle. All SMBus operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation—therefore there must be no breaks in the stream of data and ACKs / NACKs during data transfers.

For most operations, SMBus protocol requires the SDA line to remain stable (unmoving) whenever SCL is high — i.e. any transitions on the SDA line can only occur when SCL is low. The exceptions to this rule are when the master device issues a start or stop condition. Note that the slave device cannot issue a start or stop condition.

### SMBus Definitions

The following are definitions for some general SMBus terms:

**Start Condition:** This condition occurs when the SDA line transitions from high to low while SCL is high. The master device uses this condition to indicate that a data transfer is about to begin.

**Stop Condition:** This condition occurs when the SDA line transitions from low to high while SCL is high. The master device uses this condition to signal the end of a data transfer.

**Acknowledge and Not Acknowledge:** When data are transferred to the slave device it sends an “acknowledge” (ACK) after receiving each byte. The receiving device sends an ACK by pulling SDA low for one clock. Following the last byte, a master device sends a “not acknowledge” (NACK) followed by a stop condition. A NACK is indicated by forcing SDA high during the clock after the last byte.

### Slave Address

aSC7611 is designed to be used primarily in desktop systems that require only one monitoring device. If only one aSC7611 is used on the motherboard, the designer should be sure that the AddressEnable /PWM3 pin is High during the first SMBus communication addressing the aSC7611.

AddressEnable /PWM3 is an open drain I/O pin that at power-on defaults to the input state of AddressEnable . A maximum of 10k pull-up resistance on

AddressEnable /PWM3 is required to assure that the SMBus address of the device will be locked at 010 1110b, which is the default address of the aSC7611.

During the first SMBus communication TACH4 and PWM3 can be used to change the SMBus address of the aSC7611 to 0101101b or 0101100b. aSC7611 address selection procedure:

A 10kΩ pull-down resistor to ground on the

AddressEnable /PWM3 pin is required. Upon power up, the aSC7611 will be placed into

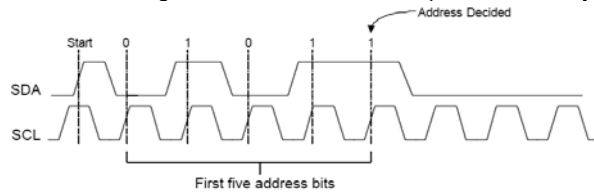
AddressEnable mode and assign itself on SMBus address according to the state of the Address Select input. The aSC7611 will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the aSC7611 address, 0 1011b. This feature eliminates the possibility of a glitch on the SMBus interfering with

address selection. When the AddressEnable /PWM3 pin is not used to change the SMBus address of the aSC7611, it will remain in a high state until the first communication with the aSC7611. After the first SMBus transaction is completed PWM3 and TACH4 will return to normal operation.

Address Enable	Address Select	Board Implementation	SMBus Address	
			Binary	Hex
0	0	Both pins pulled to ground through a 10 kΩ resistor	010 1100	2Ch
0	1	Address Select pulled to 3.3V and <u>AddressEnable</u> pulled to GND through a 10 kΩ resistor	010 1101	2Dh
1	X	<u>AddressEnable</u> pulled to 3.3V through a 10 kΩ resistor	010 1110	2Eh



In this way, up to three aSC7611 devices can exist on a SMBus at any time. Multiple aSC7611 devices can be used to monitor additional processors in the temperature zones. When using the non-default addresses, additional circuitry will be required if Tach4 and PWM3 require to function correctly. Such circuitry could consist of GPIO pins from a micro-controller. During the first communication the micro-controller would drive the AddressEnable and Address Select pins to the proper state for the required address. After the first SMBus communication the micro-controller would drive its pins into Tri-State allowing TACH4 and PWM3 to operate correctly.



## Writing to and Reading from the aSC7611

All read and write operations must begin with a start condition generated by the master device. After the start condition, the master device must immediately send a slave address (7-bits) followed by a R/W bit. If the slave address matches the address of the aSC7611, it sends an ACK by pulling the SDA line low for one clock. Read or write operations may contain one- or two-bytes. See Figures 2 through 6 for timing diagrams for all aSC7611 operations.

### Setting the Register Address Pointer

For all operations, the address pointer stored in the address pointer register must be pointing to the register address that is going to be written to or read from. This register's content is automatically set to the value of the first byte following the R/W bit being set to 0.

After the aSC7611 sends an ACK in response to receiving the address and R/W bit, the master device must transmit an appropriate 8-bit address pointer value as explained in the Registers section of this data sheet. The aSC7611 will send an ACK after receiving the new pointer data.

The register address pointer set operation is illustrated in Figure 2. If the address pointer is not a valid address the aSC7611 will internally terminate the operation. Also recall that the address register retains the current address pointer value between operations. Therefore, once a register is being pointed to, subsequent read operations do not require another Address Pointer set cycle.

## Writing to Registers

All writes must start with a pointer set as described previously, even if the pointer is already pointing to the desired register. The sequence is described in Figure 2.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the SDA line for one clock to allow the aSC7611 to acknowledge receiving the byte. The write operation should be terminated by a stop condition from the master.

## Reading from Registers

To read from a register other than the one currently being pointed to by the address pointer register, a pointer set sequence to the desired register must be done as described previously. Immediately following the pointer set, the master must perform a repeat start condition that indicates to the aSC7611 that a read is about to occur. It is important to note that if the repeat start condition does not occur, the aSC7611 will assume that a write is taking place, and the selected register will be overwritten by the upcoming data on the data bus. The read sequence is described in Figure 4. After the start condition, the master must again send the device address and read/write bit.

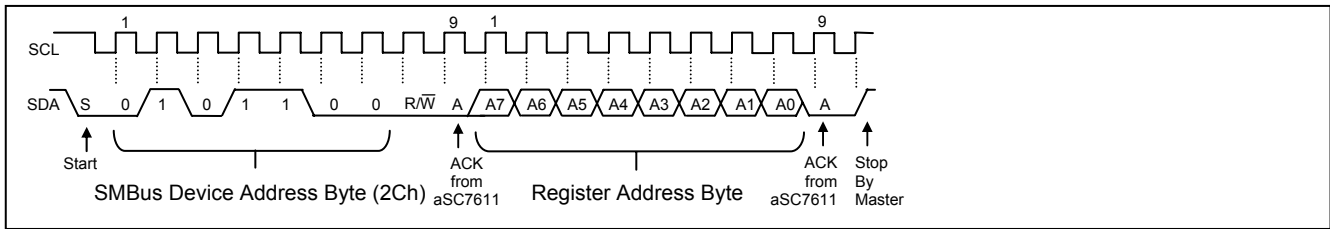
This time the R/W bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraph for reading from a preset pointer location.

If the pointer is already pointing to the desired register, the master can read from that register by setting the R/W bit (following the slave address) to a 1. After sending an ACK, the aSC7611 will begin transmitting data during the following clock cycle. After receiving the 8 data bits, the master device should respond with a NACK followed by a stop condition.

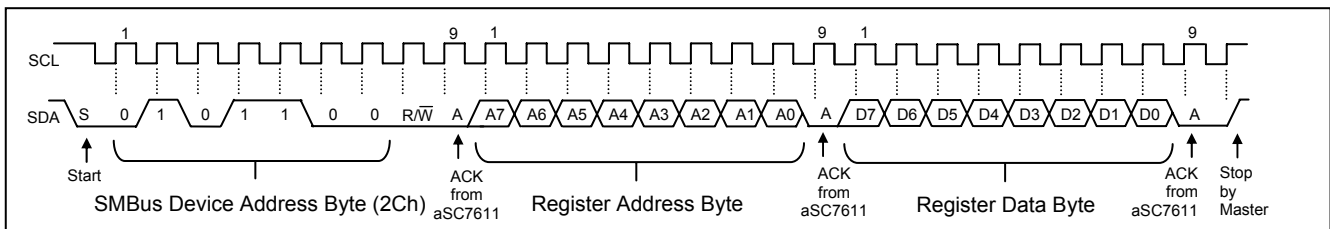
If the master is reset while the aSC7611 is in the process of being read, the master should perform an SMBus reset. This is done by holding the data or clock low for more than 35ms, allowing all SMBus devices to be reset. This follows the SMBus 2.0 specification of 25-35ms.

When the aSC7611 detects an SMBus reset, it will prepare to accept a new start sequence and resume communication from a known state.

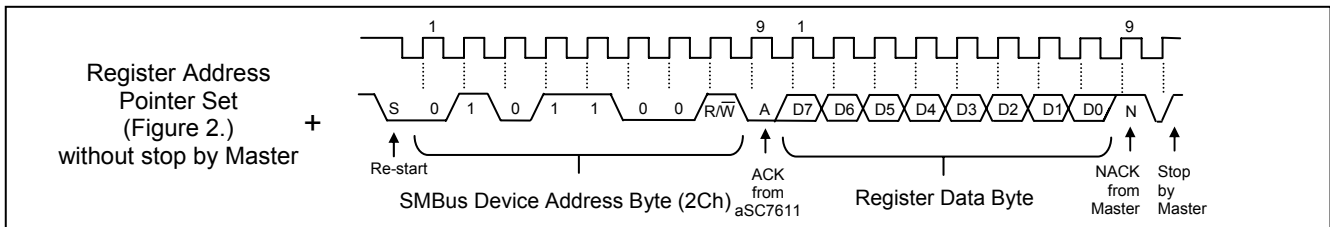
Note: The following figures assume that Device Address 2Ch has been chosen by the user.



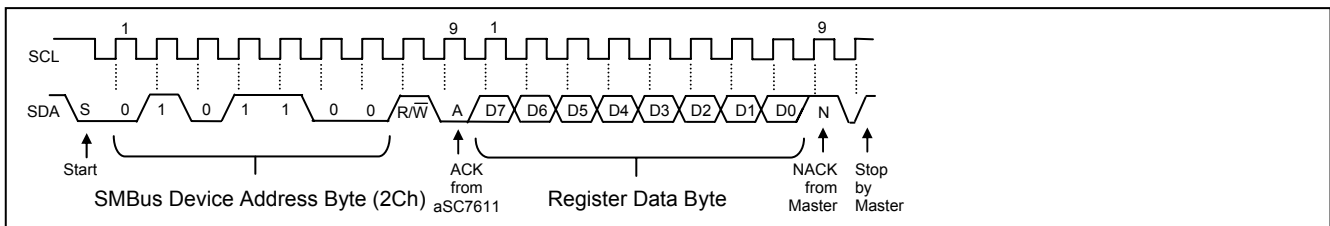
**Figure 2 Register Address Pointer Set**



**Figure 3 Register Write**



**Figure 4 Register Read**



**Figure 5 Register Read When Read Address Already Set**

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## Register Set

Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (hex)	Lock
04h	R/W	Tach 1 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	
05h	R/W	Tach 2 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	
06h	R/W	Tach 3 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	
07h	R/W	Tach 4 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36	
08h	R	Vccp (LS Byte)	1	0	X	X	X	X	X	X	00	
09h	R/W	Configuration	RES	Run/Stop	RES	RES	RES	RES	RES	RES	00	
0Eh	R	Zone 3 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00	
0Fh	R/W	One shot Measurement	RES	RES	RES	RES	RES	RES	RES	RES	00	
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00	
11h	R	3.3V (LS Byte)	1	0	X	X	X	X	X	X	00	
12h	R	5V (LS Byte)	1	0	X	X	X	X	X	X	00	
13h	R	2.5V (LS Byte)	1	0	X	X	X	X	X	X	00	
14h	R	12V (LS Byte)	1	0	X	X	X	X	X	X	00	
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00	
20h	R	2.5V (MS Byte)	9	8	7	6	5	4	3	2	00	
21h	R	Vccp (MS Byte)	9	8	7	6	5	4	3	2	00	
22h	R	3.3 V (MS Byte)	9	8	7	6	5	4	3	2	00	
23h	R	5V (MS Byte)	9	8	7	6	5	4	3	2	00	
24h	R	12V (MS Byte)	9	8	7	6	5	4	3	2	00	
25h	R	Zone 1 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00	
26h	R	Zone 2 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00	
27h	R	Zone 3 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00	
28h	R	Tach 1 LS Byte	7	6	5	4	3	2	1	0	00	
29h	R	Tach 1 MS Byte	15	14	13	12	11	10	9	8	00	
2Ah	R	Tach 2 LS Byte	7	6	5	4	3	2	1	0	00	
2Bh	R	Tach 2 MS Byte	15	14	13	12	11	10	9	8	00	

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (hex)	Lock
2Ch	R	Tach 3 LS Byte	7	6	5	4	3	2	1	0	00	
2Dh	R	Tach 3 MS Byte	15	14	13	12	11	10	9	8	00	
2Eh	R	Tach 4 LS Byte	7	6	5	4	3	2	1	0	00	
2Fh	R	Tach 4 MS Byte	15	14	13	12	11	10	9	8	00	
30h	R/W	Fan 1 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
31h	R/W	Fan 2 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
32h	R/W	Fan 3 Current PWM Duty	7	6	5	4	3	2	1	0	FF	
38h	R/W	Fan 1 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	
39h	R/W	Fan 2 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	
3Ah	R/W	Fan 3 Max Duty Cycle	7	6	5	4	3	2	1	0	FF	
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61	
3Fh	R	Version/Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	69	
40h	R/W	Ready/Lock/Start/Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00	
41h	R	Interrupt Status Register 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	00	
42h	R	Interrupt Status Register 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00	
43h	R	VID0-4	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	00	
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00	
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FF	
46h	R/W	Vccp Low Limit	7	6	5	4	3	2	1	0	00	
47h	R/W	Vccp High Limit	7	6	5	4	3	2	1	0	FF	
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00	
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FF	

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (hex)	Lock
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00	
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FF	
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00	
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FF	
4Eh	R/W	Zone 1 Low Temperature	7	6	5	4	3	2	1	0	81	
4Fh	R/W	Zone 1 High Temperature	7	6	5	4	3	2	1	0	7F	
50h	R/W	Zone 2 Low Temperature	7	6	5	4	3	2	1	0	81	
51h	R/W	Zone 2 High Temperature	7	6	5	4	3	2	1	0	7F	
52h	R/W	Zone 3 Low Temperature	7	6	5	4	3	2	1	0	81	
53h	R/W	Zone 3 High Temperature	7	6	5	4	3	2	1	0	7F	
54h	R/W	Tach 1 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
55h	R/W	Tach 1 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
56h	R/W	Tach 2 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
57h	R/W	Tach 2 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
58h	R/W	Tach 3 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
59h	R/W	Tach 3 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
5Ah	R/W	Tach 4 Minimum LS Byte	7	6	5	4	3	2	1	0	FF	
5Bh	R/W	Tach 4 Minimum MS Byte	15	14	13	12	11	10	9	8	FF	
5Ch	R/W	Fan 1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Dh	R/W	Fan 2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Eh	R/W	Fan 3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Fh	R/W	Zone 1 Range/ Fan 1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X

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Register Address	R/W	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (hex)	Lock
60h	R/W	Zone 2 Range/ Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
61h	R/W	Zone 3 Range/ Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
62h	R/W	Min/Off, Zone 1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone2 / Zone 3 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00	X
64h	R/W	Fan 1 PWM Minimum	7	6	5	4	3	2	1	0	80	X
65h	R/W	Fan 2 PWM Minimum	7	6	5	4	3	2	1	0	80	X
66h	R/W	Fan 3 PWM Minimum	7	6	5	4	3	2	1	0	80	X
67h	R/W	Zone 1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone 2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
69h	R/W	Zone 3 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Dh	R/W	Zone 1, Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X
6Eh	R/W	Zone 3 Hysteresis	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40	X
6Fh	R/W	XOR Tree Enable	RES	RES	RES	RES	RES	RES	RES	XEN	00	X
75h	R/W	Fan Spin-up Mode	Tach4 Disable	Tach3/4 Disable	Tach2 Disable	Tach1 Disable	RES	PWM3SU	PWM2SU	PWM1SU	00	X

Note: Reserved bits will always return 0 when read, X-bits in readings may be ignored.

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### Temperature Measurement

Temperatures are measured with a precision Delta- $V_{BE}$  methodology converted to a digital temperature reading by a 10-bit sigma-delta converter. The user may set limits on these readings to be continuously monitored and alarm bits set when they are exceeded. Separately, the measurements are also delivered to the automatic fan control system to adjust fan speed. The following registers contain the readings from the internal and remote sensors.

#### Registers 25-10h, 26-15h and 27-0Eh: Zone Temperature Readings (10-Bit, 2's Complement Reporting)

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
25h	R	Zone 1 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00
10h	R	Zone 1 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00
26h	R	Zone 2 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00
15h	R	Zone 2 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00
27h	R	Zone 3 Temperature (MS Byte)	9	8	7	6	5	4	3	2	00
0Eh	R	Zone 3 Temperature (LS Byte)	1	0	X	X	X	X	X	X	00

The Zone Temperature registers reflect the current temperature of the internal and remote diodes. Processor (Zone 1) Temp register reports the temperature measured by the thermal diode connected to the Remote 1- and Remote 1+ pins. Internal (Zone 2) Temp register reports the temperature measured by the internal (junction) temperature sensor. Remote 2 (Zone 3) Temp register reports the temperature measured by the thermal diode connected to the second set of Remote 2- and Remote 2+ pins. Temperatures are represented as 10 bit, 2's complement, signed numbers, in degrees Celsius, as shown below in Table 1.

The Temperature Reading register will return a value of 8000h if the remote diode pins are not used by the board designer or are not functioning properly. This reading will cause the zone limit bits (bits 4 and 6) in the Interrupt Status Register (41h) and the remote diode fault status bit (bits 6 and 7) in the Interrupt Status Register 2 (42h) to be set. These registers are read-only – a write to these registers has no effect.

Temperature	Digital Output (2's Complement)				
	High Byte		Low Byte		
	10-Bit Resolution			Ignore	
+125°C	0111	1101	00	XX	XXXX
+100°C	0110	0100	00	XX	XXXX
+50°C	0011	0010	00	XX	XXXX
+25°C	0001	1001	00	XX	XXXX
+10°C	0000	1010	00	XX	XXXX
+1.75°C	0000	0001	11	XX	XXXX
+0.25°C	0000	0000	01	XX	XXXX
0°C	0000	0000	00	XX	XXXX
-1.75°C	1111	1110	01	XX	XXXX
-55°C	1100	1001	00	XX	XXXX

**Table 1 Relationship between Temperature and 2's Complement Digital Output, -55°C to +125°C**

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## Temperature Measurement Configuration

### Registers 09h and 0Fh: Measurement Configuration

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
09h	R/W	Configuration	RES	Run/Stop	RES	RES	RES	RES	RES	RES	00
0Fh	R/W	One shot Measurement	RES	RES	RES	RES	RES	RES	RES	RES	00

A write to the One-shot Measurement register address 0Fh initiates a temperature measurement when aSC7611 is in Stop mode (set by bit 6 of register 09h) and returns to that mode after all three temperature and five voltage measurements are complete.

Bit	Name	R/W	Default	Description
0:5	Reserved	R/W	0	Reserved
6	Run/Stop	R/W	0	Measurement system run(default) or stop, places aSC7611 in a low-power or standby mode.
7	Reserved	R/W	0	Reserved

**Table 2 Configuration Register [09h] bits**

## Voltage Measurement and Limits

### Register 20-24h: Voltage Reading

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
20h	R	2.5V	7	6	5	4	3	2	1	0	00
21h	R	VCCP	7	6	5	4	3	2	1	0	00
22h	R	3.3V	7	6	5	4	3	2	1	0	00
23h	R	5V	7	6	5	4	3	2	1	0	00
24h	R	12V	7	6	5	4	3	2	1	0	00

The Register Names define the typical input voltage at which the reading is  $\frac{3}{4}$  full scale or C0h.

The Voltage Reading registers are updated automatically by the aSC7611 at a minimum frequency of 4Hz. These registers are read only – a write to these registers has no effect.

### Register 44-4Dh: Voltage Limit Registers

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
44h	R/W	2.5V Low Limit	7	6	5	4	3	2	1	0	00h
45h	R/W	2.5V High Limit	7	6	5	4	3	2	1	0	FFh
46h	R/W	VCCP Low Limit	7	6	5	4	3	2	1	0	00h
47h	R/W	VCCP High Limit	7	6	5	4	3	2	1	0	FFh
48h	R/W	3.3V Low Limit	7	6	5	4	3	2	1	0	00h
49h	R/W	3.3V High Limit	7	6	5	4	3	2	1	0	FFh
4Ah	R/W	5V Low Limit	7	6	5	4	3	2	1	0	00h
4Bh	R/W	5V High Limit	7	6	5	4	3	2	1	0	FFh
4Ch	R/W	12V Low Limit	7	6	5	4	3	2	1	0	00h
4Dh	R/W	12V High Limit	7	6	5	4	3	2	1	0	FFh

If a voltage input either exceeds the value set in the voltage high limit register or falls below the value set in the voltage low limit register, the corresponding bit will be set automatically by the aSC7611 in the interrupt status registers (41-42h). Voltages are presented in the registers at  $\frac{3}{4}$  of full-scale for the nominal voltage, meaning that at nominal voltage, each input will be C0h, as shown in Table 3. Note that 3.3V input is Vdd and is not allowed to go below 3.0V during normal operation.

Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Input	Nominal Voltage	Register Reading at Nominal Voltage	Maximum Voltage	Register Reading at Maximum Voltage	Minimum Voltage	Register Reading at Minimum Voltage
2.5V	2.5V	C0h	3.32V	FFh	0V	00h
VCCP	2.25V	C0h	3.00V	FFh	0V	00h
3.3V	3.3V	C0h	4.38V	FFh	3.0V	AFh
5V	5.0V	C0h	6.64V	FFh	0V	00h
12V	12.0V	C0h	16.00V	FFh	0V	00h

**Table 3 Voltage Limits vs Register Setting**

## Status Registers

### Register 41h: Interrupt Status Register 1

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
41h	R	Interrupt Status 1	ERR	ZN3	ZN2	ZN1	5V	3.3V	VCCP	2.5V	00

The Interrupt Status Register 1 bits will be automatically set, by the aSC7611, whenever a fault condition is detected. A fault condition is detected whenever a measured value is outside the window set by its limit registers. ZN1 bit will be set when a diode fault condition, such as an open or short, is detected. More than one fault may be indicated in the interrupt register when read. The register will hold a set bit(s) until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7611 after it is read by software, if the fault condition no longer exists. Once set, the Interrupt Status Register 1 bits will remain set until a read event occurs, even if the fault condition no longer exists. This register is read-only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	2.5V Limits Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the 2.5V input voltage is less than or equal to the limit set in the 2.5V Low Limit register or greater than the limit set in the 2.5V High Limit register.
1	Vccp Limits Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the VCCP input voltage is less than or equal to the limit set in the VCCP Low Limit register or greater than the limit set in the VCCP High Limit register.
2	3.3V Limits Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the 3.3V input voltage is less than or equal to the limit set in the 3.3V Low Limit register or greater than the limit set in the 3.3V High Limit register.
3	5V Limits Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the 5V input voltage is less than or equal to the limit set in the 5V Low Limit register or greater than the limit set in the 5V High Limit register.
4	Zone 1 Limit Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the temperature input measured by the Remote1- and Remote1+ inputs is less than or equal to the limit set in the Processor (Zone 1) Low Temp register or more than the limit set in the Processor (Zone 1) High Temp register. This bit will be set when a diode fault is detected.
5	Zone 2 Limit Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the temperature input measured by the internal temperature sensor is less than or equal to the limit set in the thermal (Zone 2) Low Temp register or greater than the limit set in the Internal (Zone 2) High Temp register.
6	Zone 3 Limit Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the temperature input measured by the second remote temperature sensor is less than or equal to the limit set in the thermal (Zone 3) Low Temp register or greater than the limit set in the Internal (Zone 3) High Temp register.
7	Error in Status Register 2	R	0	If there is a set bit in Status Register 2, this bit will be set to 1.

**Table 4 Interrupt Status Register 1**

**Register 42h: Interrupt Status Register 2**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
42h	R	Interrupt Status 2	ERR2	ERR1	FAN4	FAN3	FAN2	FAN1	RES	12V	00

The Interrupt Status Register 2 bits will be automatically set, by the aSC7611, whenever a fault condition is detected. Interrupt Status Register 2 identifies faults caused by temperature sensor error, fan speed dropping below minimum set by the tachometer minimum register. Interrupt Status Register 2 will hold a set bit until the event is read by software. The contents of this register will be cleared (set to 0) automatically by the aSC7611 after it is read by software, if fault condition no longer exists. Once set, the Interrupt Status Register 2 bits will remain set until a read event occurs, even if the fault no longer exists. This register is read-only – a write to this register has no effect.

Bit	Name	R/W	Default	Description
0	12V Limits Exceeded	R	0	The aSC7611 automatically sets this bit to 1 when the 12V input voltage is less than or equal to the limit set in the 12V Low Limit register or greater than the limit set in the 12V High Limit register.
1	RES	R	0	Reserved
2	FAN 1 STALLED	R	0	The aSC7611 automatically sets this bit to 1 when the TACH 1 input reading is above the count value set in the Tach 1 Minimum MSB and LSB registers.
3	FAN 2 STALLED	R	0	The aSC7611 automatically sets this bit to 1 when the TACH 2 input reading is above the count value set in the Tach 2 Minimum MSB and LSB registers.
4	FAN 3 STALLED	R	0	The aSC7611 automatically sets this bit to 1 when the TACH 3 input reading is above the count value set in the Tach 3 Minimum MSB and LSB registers.
5	FAN 4 STALLED	R	0	The aSC7611 automatically sets this bit to 1 when the TACH 4 input reading is above the count value set in the Tach 4 Minimum MSB and LSB registers.
6	Remote Diode 1 Fault	R	0	The aSC7611 automatically sets this bit to 1 when there is an open circuit fault on the Remote1+ or Remote1- thermal diode input pins. A diode fault will also set bit 4 Zone 1 Limit bit, of Interrupt Status Register 1.
7	Remote Diode 2 Fault	R	0	The aSC7611 automatically sets this bit to 1 when there is an open circuit fault on the Remote2+ or Remote2- thermal diode input pins. A diode fault will also set bit 6 Zone 3 Limit bit, of Interrupt Status Register 1.

**Table 5 Interrupt Status Register 2**
**Register 43h: VID Register**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
43h	R	VID0-4	RES	RES	RES	VID4	VID3	VID2	VID1	VID0	00

The VID register contains the values of aSC7611 VID0-VID4 input pins. This register indicates the status of the VID lines that interconnect the processor to the Voltage Regulator Module (VRM). Software uses the information in this register to determine the voltage that the processor is designed to operate at. With this information, software can then dynamically determine the correct values to place in the VCCP Low Limit and VCCP High Limit registers. This register is read-only – a write to this register has no effect.

**Tachometer Measurement and Configuration**
**Register 28-2Fh: Fan Tachometer Reading**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
28h	R	Tach 1 LS Byte	7	6	5	4	3	2	1	0	N/A
29h	R	Tach 1 MS Byte	15	14	13	12	11	10	9	8	N/A
2Ah	R	Tach 2 LS Byte	7	6	5	4	3	2	1	0	N/A
2Bh	R	Tach 2 MS Byte	15	14	13	12	11	10	9	8	N/A
2Ch	R	Tach 3 LS Byte	7	6	5	4	3	2	1	0	N/A

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
2Dh	R	Tach 3 MS Byte	15	14	13	12	11	10	9	8	N/A
2Eh	R	Tach 4 LS Byte	7	6	5	4	3	2	1	0	N/A
2Fh	R	Tach 4 MS Byte	15	14	13	12	11	10	9	8	N/A

The Fan Tachometer Reading registers contains the number of 11.111µs periods (90 kHz) between full fan revolutions. The results are based on the time interval of two tachometer pulses, since most fans produce two tachometer pulses per full revolution. These registers will be updated at least once every second. Common interpretation of tachometer readings is to take the binary period measurement and convert it to RPM. This may be done by applying the formula:

$$\text{RPM} = (90,000 \times 60) / (\text{Decimal Equivalent of binary Tach Reading})$$

The value, for each fan, is represented by a 16-bit unsigned number.

The Fan Tachometer Reading registers will always return an accurate fan tachometer measurement, even when a fan is disabled or non-functional, however, if PWM commands for a fan (register 30h to 32h) is zero, tach measurements are suspended and the last reading may remain in the register.

FF FFh indicates that the fan is not spinning, or that the tachometer input is not connected to a valid signal. This value may be FF FEh or FF FCh if Measurement Duration, bits 1:0 of register 3A-3Dh are set to 01 or 00, respectively. These registers are read-only – a write to these registers has no effect.

When the LSByte of the aSC7611 16-bit register is read, the other byte (MSByte) is latched at the current value until it is read. At the end of the MSByte read the Fan Tachometer Reading registers are updated. During spin-up, the PWM duty cycle reported is 0%.

### Registers 54-5Bh: Fan Tachometer Limits

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
54h	R/W	Tach 1 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
55h	R/W	Tach 1 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
56h	R/W	Tach 2 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
57h	R/W	Tach 2 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
58h	R/W	Tach 3 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
59h	R/W	Tach 3 Minimum MS Byte	15	14	13	12	11	10	9	8	FF
5Ah	R/W	Tach 4 Minimum LS Byte	7	6	5	4	3	2	1	0	FF
5Bh	R/W	Tach 4 Minimum MS Byte	15	14	13	12	11	10	9	8	FF

The Fan Tachometer Low Limit registers indicate the tachometer reading under which the corresponding bit will be set in the Interrupt Status Register 2 register. In Auto Fan Control mode, the fan can run at low speeds, so care should be taken in software to ensure that the limit is high enough not to cause sporadic alerts. The fan tachometer will not cause a bit to be set in Interrupt Status Register 2 if the current value in Current PWM Duty registers (30h to 32h) is 00h or if the fan is disabled via the Fan Configuration Register. Interrupts will not be generated for a fan if its minimum is set to FF FFh except for timeout. Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Given the relative insignificance of Bit 0 and Bit 1, these bits could be programmed to designate the physical location of the fan generating the tachometer signal, as follows:

Register Name	Bit 1	Bit 0 (LSB)
CPU Cooler	0	0
Memory Controller	0	1
Chassis Front	1	0
Chassis Rear	1	1

Register 04-07h: Fan Tachometer Measurement Configuration

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
04h	R/W	Tach 1 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36
05h	R/W	Tach 2 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36
06h	R/W	Tach 3 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36
07h	R/W	Tach 4 Configuration	3-Wire Enable1	3-Wire Enable0	Meas Blank 1	Meas Blank 0	Meas Dwell 1	Meas Dwell 0	Meas Duration 1	Meas Duration 0	36

The Fan Tachometer Configuration registers contain the settings that define the modes of measurement of the Tachometer input signals. The user is allowed to disable a tachometer measurement or to request PWM stretching, in the case of a 3-wire fan. Also, the rate, start-up and period of measurements within a fan rotation cycle may be selected. The table below describes the controls.

Bit	Name	R/W	Default	Description																																				
1:0	Measurement Duration	R/W	10	The amount of fan rotation used for the tach measurement. Assumes 2 pulse periods per rotation of fan. 00: ¼ Rotation – Tach Count x4 = Reported Value 01: ½ Rotation – Tach Count x2 = Reported Value 10: 1 Rotation – Tach Count x1 = Reported Value (default) 11: 2 Rotation – Tach Count x1 = Reported Value																																				
3:2	Measurement Dwell	R/W	01	Delay between Tach Measurements 00: 100 ms 01: 300 ms (default) 10: 500 ms 11: 728 ms																																				
5:4	Measurement Blank	R/W	11	In 3-wire fan mode, a delay is needed to assure that the tach input has stabilized after the PWM has been set to 100% 00: 11.1 µs 01: 22.2 µs 10: 33.3 µs 11: 44.4 µs (default)																																				
7:6	3-Wire Enable	R/W	00	For 3-Wire mode, the PWM output will be forced to 100% when the tach measurement is being processed. Each fan has a 3-Wire Mode control that will behave as indicated in this table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>HLFRQ (5Fh-61h)</th> <th colspan="2">3-Wire Enable (7:6)</th> <th>3-Wire Mode</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>Enabled</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Enabled</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>Enabled</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>Disabled</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>Disabled</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>Disabled</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>Enabled</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>Disabled</td></tr> </tbody> </table>	HLFRQ (5Fh-61h)	3-Wire Enable (7:6)		3-Wire Mode	0	0	0	Enabled	0	0	1	Enabled	0	1	0	Enabled	0	1	1	Disabled	1	0	0	Disabled	1	0	1	Disabled	1	1	0	Enabled	1	1	1	Disabled
HLFRQ (5Fh-61h)	3-Wire Enable (7:6)		3-Wire Mode																																					
0	0	0	Enabled																																					
0	0	1	Enabled																																					
0	1	0	Enabled																																					
0	1	1	Disabled																																					
1	0	0	Disabled																																					
1	0	1	Disabled																																					
1	1	0	Enabled																																					
1	1	1	Disabled																																					

Table 6 Tachometer Configuration Register

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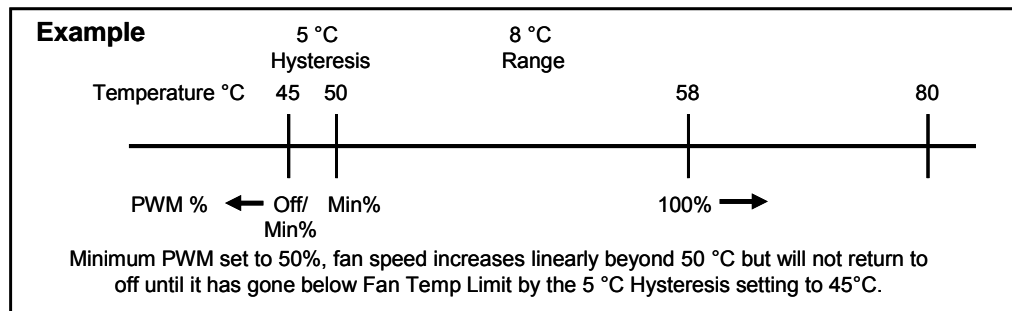
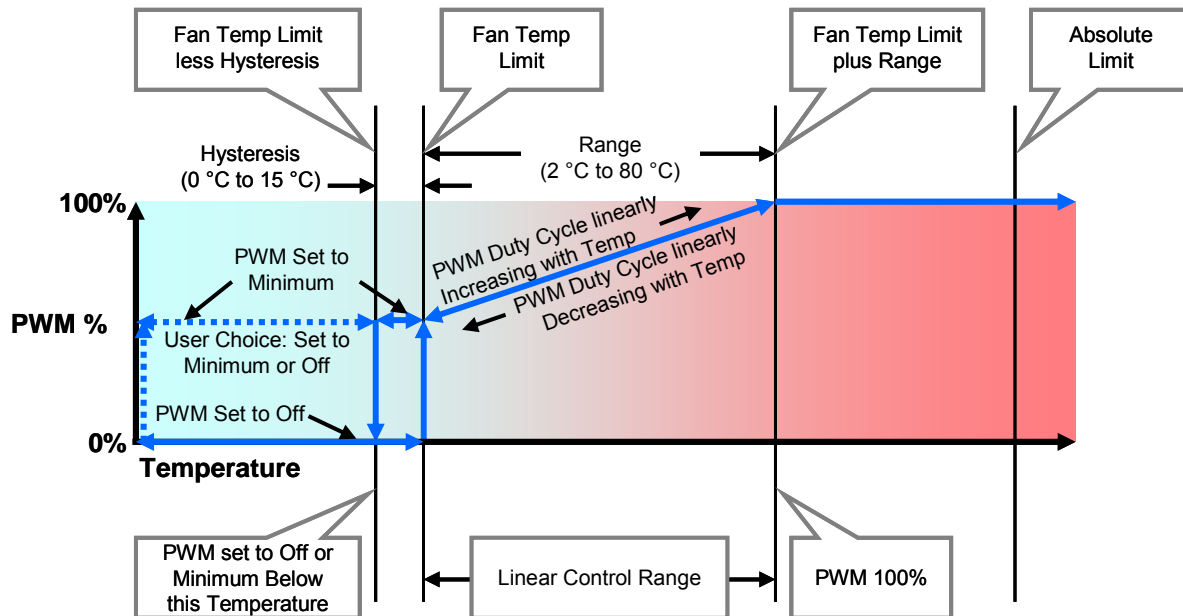
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## Automatic Fan Control

### Auto Fan Control Operating Mode

The aSC7611 includes the circuitry for automatic fan control. In Auto Fan Mode, the aSC7611 will automatically adjust the PWM duty cycle of the PWM output. PWM outputs are assigned to a thermal zone based on the fan configuration registers. At any time, the temperature of a zone exceeds its Absolute Limit, all PWM outputs will go to 100% duty cycle to provide maximum cooling to the system.



**Figure 6 Automatic Fan Speed Control Example**

Example for PWM1 assigned to Zone 1:

- Zone 1 Fan Temp Limit (Register 67h) is set to 50°C (32h).
- Zone 1 Range (Register 5Fh) is set to 8°C (6xh).
- Fan PWM Minimum (Register 64h) is set to 50% (80h).

In this case, the PWM duty cycle will be 50% at 50°C.

Since (Zone 1 Fan Temp Limit) + (Zone 1 Range) = 50°C + 8°C = 58°C, the fan will run at 100% duty cycle when the temperature of the Zone 1 sensor reaches 58°C.

Since the midpoint of the fan control range is 54°C, and the median duty cycle is 75% (Halfway between the PWM Minimum and 100%), PWM1 duty cycle would be 75% at 54°C.

Above (Zone 1 Fan Temp Limit) + (Zone 1 Range), the duty cycle will be 100%.

### Automatic Fan Speed Control using Maximum PWM Setting

The previously described and illustrated mode had no restriction on the maximum PWM setting. It is useful to limit the maximum PWM command sent to the fan in order to minimize the acoustic impact. The Maximum PWM setting will clamp the automatic fan PWM command at a user selected value. The Absolute Limit setting will still cause the PWM command to be 100% and that will remain until the temperature falls below the Absolute Limit temperature by an amount equal to the hysteresis setting. This will minimize the acoustic impact of having a temperature moving back and forth close to the Absolute Limit.

The Absolute Limit may be set above or below the Fan Temp Limit plus Range. The PWM value will be overridden and will follow the hysteresis curve in either case, but the acoustic impact will be different, running the fan to 100% PWM at a lower temperature, but enhancing the cooling effect. Absolute Limit set on the low end is shown in Figure 6. Setting it above is shown in Figure 8.

It is important to consider the combination of Fan Temp Limit, Range, Maximum PWM and Absolute Limit and their impact on cooling and acoustics. In addition, the capability to operate a fan from a combination of thermal zones allows a compound linear slope to be achieved for further optimization.

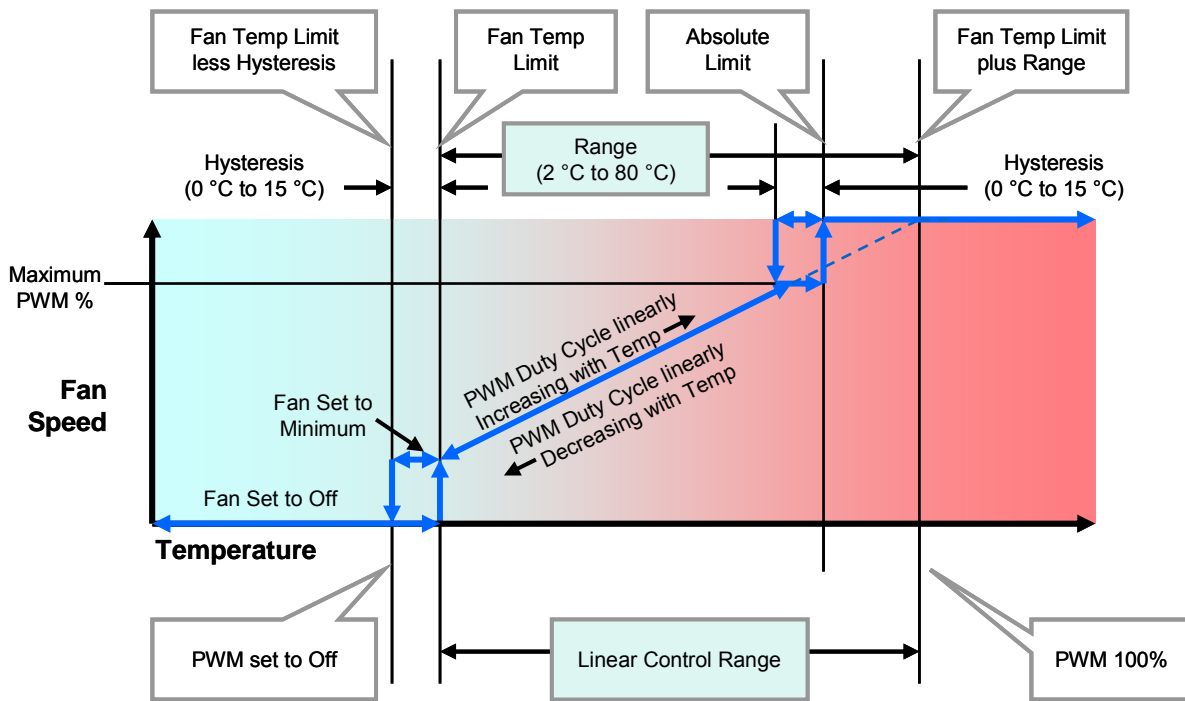


Figure 7 Fan Control with Absolute Limit Set below Fan Temp Limit Plus Range

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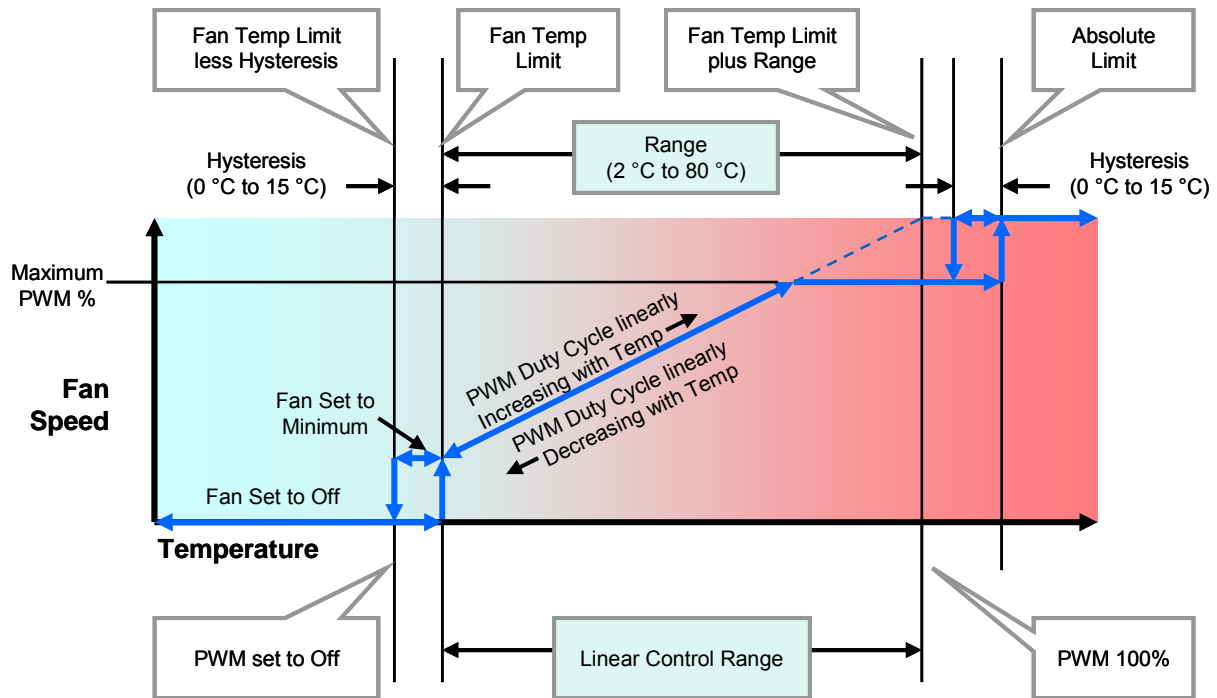


Figure 8 Fan Control with Absolute Limit Set above Fan Temp Limit Plus Range

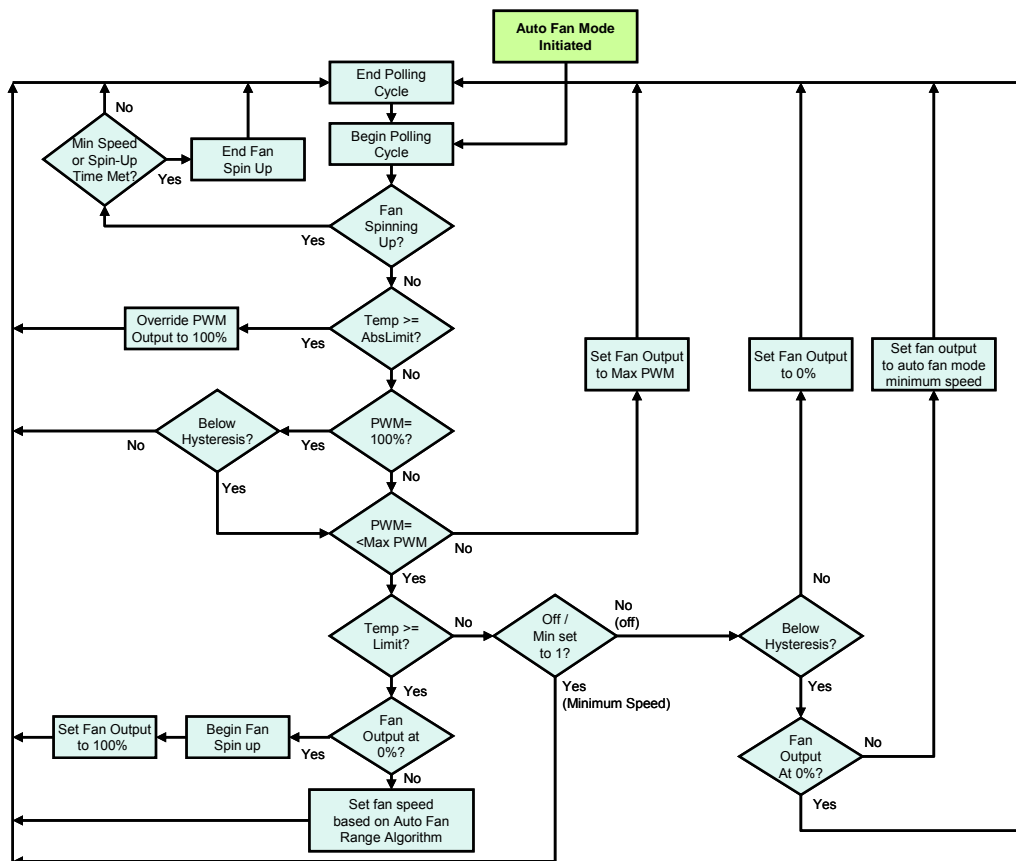


Figure 9 Automatic Fan Control Algorithm

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## Fan Register Device Set-Up

The BIOS will follow the following steps to configure the fan registers on the aSC7611. The registers corresponding to each function are listed. All steps may not be necessary if default values are acceptable. Regardless of all changes made by the BIOS to the fan limit and parameter registers during configuration, the aSC7611 will continue to operate based on default values until the START bit (bit 0), in the Ready/Lock/Start/Override register (address 40h), is set. Once the fan mode is updated, by setting the START bit to 1, the aSC7611 will operate using the values that were set by the BIOS in the fan control limit and parameter registers (address in the range 5Ch through 75h).

1. Set limits and parameters (not necessarily in this order):
  - [5F-61h] Set PWM frequency for the fan and auto fan control range for each zone.
  - [62-63h] Set spike smoothing and min/off.
  - [5C-5Eh] Set the fan spin-up delay.
  - [75h] Set PWM spin-up mode to terminate after time set in [5Ch]. Value = 00h instead of default 01h.
  - [5Ch] Match fan with a corresponding thermal zone.
  - [67-69h] Set the fan temperature limits.
  - [6A-6Ch] Set the temperature absolute limits.
  - [64-66h] Set the PWM minimum duty cycle.
  - [6D-6Eh] Set the temperature hysteresis values.
2. [40h] Set bit 0 (START) to update fan control and limit register values and start fan control based on these new values.

[40h] (Optional) Set bit 1 (LOCK) to lock the fan limit and parameter registers. **WARNING:** this is a **non-reversible** change in state and locks out further change in critical fan control parameters until power is removed from the aSC7611.

### Register 5F-61h: Auto Fan Speed Range, PWM Frequency

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Fh	R/W	Zone 1 Range Fan1 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
60h	R/W	Zone 2 Range/ Fan 2 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X
61h	R/W	Zone 3 Range/ Fan 3 Frequency	RAN3	RAN2	RAN1	RAN0	HLFRQ	FRQ2	FRQ1	FRQ0	C3	X

In Auto Fan Mode, when the temperature for a zone is above the Temperature Limit (Registers 67-69h) and below its Absolute Temperature Limit (Registers 6A-6Ch), the speed of a fan assigned to that zone is determined as follows:

When the temperature reaches the Fan Temp Limit for a zone, the PWM output assigned to that zone will be Fan PWM Minimum. Between Fan Temp Limit and (Fan Temp Limit + Range), the PWM duty cycle will increase linearly according to the temperature as shown in the figure below. The PWM duty cycle will be 100% at (Fan Temp Limit + Range).

#### PWM frequency - FRQ[3:0] and HLFRQ

The PWM frequency bits [3:0] determine the PWM frequency for the fan. The aSC7611 has high and low frequency ranges for the PWM outputs that are controlled by the HLFRQ bit.

PWM Frequency Selection (Default = 0011 ≈ 30 Hz).

HLFRQ	FRQ [2:0]	PWM Frequency
0	000	~10 Hz
0	001	~15 Hz
0	010	~23 Hz
0	011	~30 Hz (Default)
0	100	~38 Hz
0	101	~47 Hz
0	110	~62 Hz
0	111	~94 Hz
1	000	~23 kHz
1	001	~24 kHz
1	010	~25 kHz
1	011	~26 kHz
1	100	~27 kHz
1	101	~28 kHz
1	110	~29 kHz
1	111	~30 kHz

**Table 7 Register Setting vs PWM Frequency**

RAN[3:0]	Linear Control Range (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

**Table 8 Zone Range Setting, RAN[3:0]**

This register becomes Read-Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect. After power up the default value is used for bits 3:0 of registers 5F-61h whenever the Ready/Lock/Start/Override register Start bit is cleared even though modifications to this register are possible.

**Register 40h: Ready/Lock/Start/Override**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
40h	R/W	Ready/Lock/Start/Override	RES	RES	RES	RES	OVRID	READY	LOCK	START	00

Bit	Name	R/W	Default	Description
0	START	R/W	0	When software writes a 1 to this bit, the aSC7611 fan monitoring and PWM output control functions will use the values set in the fan control limit and parameter registers (addresses 30-32h and 5Fh through 61h). Before this bit is set, the aSC7611 will not update the used register values, the default values will remain in effect. Whenever this bit is set to 0, the aSC7611 fan monitoring and PWM output control functions use the default fan limits and parameters, regardless of the current values in the limit and parameter registers (addresses 30-32h and 5Fh through 61h). The aSC7611 will preserve the values currently stored in the limit and parameter registers when this bit set or cleared. This bit is not affected by the state of the Lock bit. It is expected that all limit and parameter registers will be set by BIOS or application software prior to setting this bit.
1	LOCK	R/W	0	Setting this bit to 1 locks specified limit and parameter registers. <b>WARNING:</b> Once this bit is set, limit and parameter registers become read-only and will remain locked <b>until the device is powered off</b> . This register bit becomes read-only once it is set.
2	READY	R	0	The aSC7611 sets this bit automatically after the part is fully powered up, has completed the power-up-reset process, and after all A/D converters are properly functioning.
3	OVRID	R/W	0	If this bit is set to 1, all PWM outputs will go to 100% duty cycle regardless of whether or not the lock bit is set. The OVRID bit has precedence over the disabled mode. Therefore, when OVRID is set the PWM will go to 100% even if the PWM is in the disabled mode.
4-7	RESERVED	R	0	Reserved

**Table 9 READY / LOCK / START / OVRID Settings**

### Register 30-32h: Current PWM Duty Cycle

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
30h	R/W	Fan 1 Current PWM Duty	7	6	5	4	3	2	1	0	FF
31h	R/W	Fan 2 Current PWM Duty	7	6	5	4	3	2	1	0	FF
32h	R/W	Fan 3 Current PWM Duty	7	6	5	4	3	2	1	0	FF

The Current PWM Duty registers store the current duty cycle at each PWM output. At initial power-on, the PWM duty cycle is 100% and thus, when read, this register will return FFh. After the Ready/Lock/Start/Override register Start bit is set, this register and the PWM signals will be updated based on the algorithm described in the Auto Fan Control Operating Mode section. When Ready/Lock/Start/Override register Start bit is zero, default value (FFh) is used.

When read, the Current PWM Duty registers return the current PWM duty cycle. These registers are read-only unless the fan is in manual (test) mode, in which case a write to these registers will directly control the PWM duty cycle for each fan. The PWM duty cycle is represented as shown in Table 10.

If a 3-wire fan is being used and the option to enable 3-wire tach measurement is selected, the effective PWM duty cycle will be impacted by this feature. The 3-wire Enable setting will hold the PWM signal high for the period taken to make a tachometer reading. This period depends on the RPM and various tachometer measurement parameters. Overall impact is that lower PWM commands will be effectively increased and there may be acoustic effects.



Current PWM %	Register Value		
	Binary	Hex	
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

**Table 10 Current PWM Duty Cycle Setting**

**Register 4E-53h: Thermal Zone Temperature Limit Registers**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
4Eh	R/W	Zone 1 Low Temperature	7	6	5	4	3	2	1	0	81
4Fh	R/W	Zone 1 High Temperature	7	6	5	4	3	2	1	0	7F
50h	R/W	Zone 2 Low Temperature	7	6	5	4	3	2	1	0	81
51h	R/W	Zone 2 High Temperature	7	6	5	4	3	2	1	0	7F
52h	R/W	Zone 3 Low Temperature	7	6	5	4	3	2	1	0	81
53h	R/W	Zone 3 High Temperature	7	6	5	4	3	2	1	0	7F

If an external temperature input or the internal temperature sensor either exceeds the value set in the corresponding high limit register or falls below the value set in the corresponding low limit register, the corresponding bit will be set automatically by the aSC7611 in the Interrupt Status Register 1 (41h). For example, if the temperature read from the Remote - and Remote + inputs exceeds the Zone 1 High Temp register limit setting, Interrupt Status Register 1 ZN1 bit will be set. The temperature limits in these registers are represented as 8 bit 2's complement, signed numbers in Celsius, as shown below in Table 11. Setting the Ready/Lock/Start/Override register Lock bit has no effect on these registers.

Temperature	Temperature Limit (2's Complement)	
>127°C	0111	1111
+127°C (Default High)	0111	1111
+125°C	0111	1101
+90°C	0101	1010
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C (Default Low)	1000	0001

**Table 11 Zone Temperature High- and Low-Limit Registers - 8-Bit Two's Complement**

**Register 5C-5Eh: Fan Thermal Zone Assignment and Spin-up Mode**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
5Ch	R/W	Fan 1 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Dh	R/W	Fan 2 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X
5Eh	R/W	Fan 3 Configuration	ZON2	ZON1	ZON0	INV	RES	SPIN2	SPIN1	SPIN0	62	X

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

**Bits [7:5] Zone/Mode**

Bits [7:5] of the Fan Configuration registers associate each fan with a temperature sensor. When in Auto Fan Mode the fan will be assigned to a zone, and its PWM duty cycle will be adjusted according to the temperature of that zone. If "Hottest" option is selected (110), the fan will be controlled by the the hottest of zones 1, 2 or 3. To determine the "hottest zone", the PWM level for each zone is calculated then the zone with the higher PWM value (not temperature) is selected. When in manual control mode, the Current PWM duty register (30-32h) become Read/Write. It is then possible to control the PWM outputs with software by writing to these registers. When the fan is disabled (100) the corresponding PWM output should be driven low (or high, if inverted).

Zone 1: Remote Diode 1 (processor), Zone 2: Internal Sensor, Zone 3 : Remote Diode 2

Fan Configuration	ZON[2:0]
Fan on Zone 1 auto	000
Fan on Zone 2 auto	001
Fan on Zone 3 auto	010
Fan always on full	011
Fan disabled	100
Fan controlled by hotter of Zones 2 or 3	101
Fan controlled by hottest of Zones 1, 2 or 3	110
Fan manually controlled (Test Mode)	111

**Table 12 Fan Zone Setting**

**Bit [4] PWM Invert**

Bit [4] inverts the PWM output. If set to 0, 100% duty cycle will yield an output that is always high. If set to 1, 100% duty cycle will yield an output that is always low.

**Bit [3] Reserved**

**Bit [2:0] Spin Up**

Bits [2:0] specify the 'spin up' time for the fan. When a fan is being started from a stationary state, the PWM output is held at 100% duty cycle for the time specified in the table below before scaling to a lower speed.

Spin Up Time	SPIN[2:0]
0 ms	000
100 ms	001
250 ms	010
400 ms	011
700 ms	100
1000 ms	101
2000 ms	110
4000 ms	111

**Table 13 Fan Spin-Up Register**

**Register 62, 63h: Min/Off, Spike Smoothing**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
62h	R/W	Min/Off, Zone1 Spike Smoothing	OFF3	OFF2	OFF1	RES	ZN1E	ZN1-2	ZN1-1	ZN1-0	00	X
63h	R/W	Zone2 Spike Smoothing	ZN2E	ZN2-2	ZN2-1	ZN2-0	ZN3E	ZN3-2	ZN3-1	ZN3-0	00	X

The OFF1-OFF3 (Bits 7 to 5) specify whether the duty cycle will be 0% or Minimum Fan Duty when the measured temperature falls below the Temperature LIMIT register setting (see Table 15 below).

If the Remote pins are connected to a processor or chipset, instantaneous temperature spikes may be sampled by the aSC7611. Fan speed algorithm has two phases of filtering on temperature zone readings. First, a “No-Spike” value is created from the current temperature and three previous readings. This is an average of the two remaining values when the high and low values are removed. This is the temperature used to determine PWM and is always running.

The second phase is a user specified filter and coefficient. This filter determines a smoothed temperature value, Smooth  $T_i$ , by taking the No-Spike  $T_i$ , subtracting the previous smoothed temperature, Smooth  $T_{i-1}$ , divided by  $2^N$  and adding that to the previously smoothed temperature. N and GAIN are coefficients selected internally to provide the spike filter smoothing time constants shown in Table 14, designated ZN1-2:ZN1-0 for Zone 1, ZN2-2:ZN2-0 for Zone 2 and ZN3-2:ZN3-0 for Zone 3.

For the current temperature reading  $T_i$ :

$$\text{No-Spike } T_i = (\text{Discard min and max of } (T_i, T_{i-1}, T_{i-2}, T_{i-3}))/2$$

$$\text{Smooth } T_i = \text{GAIN} * (\text{No-Spike } T_i - \text{Smooth } T_{i-1})/2^N + \text{Smooth } T_{i-1}$$

If these spikes are not filtered, the CPU fan (if connected to aSC7611) may turn on prematurely or produce unpleasant noise. For this reason, any zone that is connected to a chipset or processor should have spike smoothing enabled. Individual system characteristics will determine how large this coefficient should be.

When spike smoothing is enabled, the temperature reading registers will still reflect the current value of the temperature – not the “smoothed out” value.

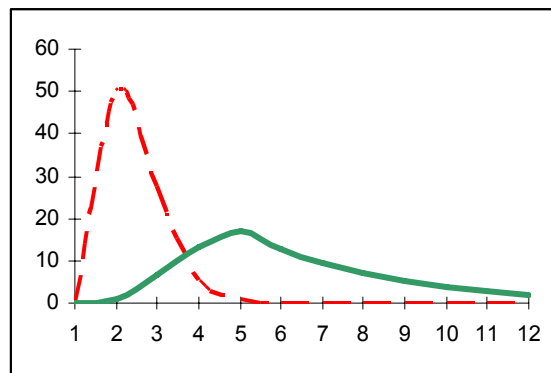
ZN1E, ZN2E and ZN3E enable temperature smoothing for zones 1, 2 and 3 respectively.

ZN1-2, ZN1-1 and ZN1-0 control smoothing time for Zone 1.

ZN2-2, ZN2-1 and ZN2-0 control smoothing time for Zone 2.

ZN3-2, ZN3-1 and ZN3-0 control smoothing time for Zone 3.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.



**Figure 10 Representation of What Temperature Is Passed to the aSC7611 Auto Fan Control with (green) and without (red dashed) Spike Smoothing**

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Spike Smoothing Time	ZNn-[2:0]
35 seconds	000
17.6 seconds	001
11.8 seconds	010
7.0 seconds	011
4.4 seconds	100
3.0 seconds	101
1.6 seconds	110
0.8 seconds	111

**Table 14 Spike Smoothing for ZN1 to ZN3**

PWM Action	Off/Min Bit
At 0% duty below LIMIT	0
At Min PWM Duty below LIMIT	1

**Table 15 PWM Output Below Limit Depending on Value of Off/Min**

**Register 64-66h: Minimum PWM Duty Cycle**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
64h	R/W	Fan 1 PWM Minimum	7	6	5	4	3	2	1	0	80	X
65h	R/W	Fan 2 PWM Minimum	7	6	5	4	3	2	1	0	80	X
66h	R/W	Fan 3 PWM Minimum	7	6	5	4	3	2	1	0	80	X

This register specifies the minimum duty cycle that the PWM will output when the measured temperature reaches the Temperature LIMIT register setting.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Minimum PWM %	Register Value		
	Binary	Hex	
0%	0000	0000	00
~25%	0100	0000	40
~50% (Default)	1000	0000	80
~75%	1100	0000	C0
100%	1111	1111	FF

**Table 16 Minimum PWM Duty Cycle Setting**

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**Register 38-3Ah: Maximum PWM Duty Cycle**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
38h	R/W	Fan 1 Max Duty Cycle	7	6	5	4	3	2	1	0	FF
39h	R/W	Fan 2 Max Duty Cycle	7	6	5	4	3	2	1	0	FF
3Ah	R/W	Fan 3 Max Duty Cycle	7	6	5	4	3	2	1	0	FF

The Maximum PWM Duty registers store the maximum duty cycle that may be commanded at each PWM output under automatic fan control. This value is overridden to 100% when the assigned zone's temperature has exceeded the Absolute Maximum Temperature setting. When temperature falls below Absolute Maximum, PWM command will resume the linear ramp only after it has fallen by the Thermal Zone Hysteresis value (Registers 6D-6Eh). Values follow the representation in Table 10.

**Register 67-69h: Temperature Limit**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
67h	R/W	Zone1 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
68h	R/W	Zone2 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X
69h	R/W	Zone 3 Fan Temp Limit	7	6	5	4	3	2	1	0	5A	X

These are the temperature limits for the individual zones. When the current temperature equals this limit, the fan will be turned on if it is not already. When the temperature exceeds this limit, the fan speed will be increased according to the algorithm set forth in the Auto Fan Range, PWM Frequency register description, Default = 90°C = 5Ah

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

Temperature	Fan Temp Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+90°C (default)	0101	1010
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001

**Table 17 Fan Temperature Limit Register - 8-Bit Two's Complement**

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**Register 6A-6Ch: Temperature Limit**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Ah	R/W	Zone 1 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Bh	R/W	Zone 2 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X
6Ch	R/W	Zone 3 Temp Absolute Limit	7	6	5	4	3	2	1	0	64	X

In the Auto Fan mode, if a zone exceeds the temperature set in the Absolute Temperature Limit register, all of the PWM outputs will increase its duty cycle to 100%. This is a safety feature that attempts to cool the system if there is a potentially catastrophic thermal event. If set to 80h (-128°C), the feature is disabled. Default = 100 C = 64h. The PWM will remain at 100% until the assigned zone temperature falls below the Absolute Temp Limit for that zone by an amount equal to the hysteresis value for that zone.

These registers become read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

Temperature	Absolute Limit (2's Complement)	
>127°C	0111	1111
+127°C	0111	1111
+125°C	0111	1101
+100°C (default)	0110	0100
+50°C	0011	0010
+25°C	0001	1001
0°C	0000	0000
-50°C	1100	1110
-127°C	1000	0001
-128°C (Disable)	1000	0000

**Table 18 Absolute Temperature Limit Register - 8-Bit Two's Complement**

**Register 6D-6Eh: Thermal Zone Hysteresis**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Dh	R/W	Zone 1 and Zone 2 Hysteresis	H1-3	H1-2	H1-1	H1-0	H2-3	H2-2	H2-1	H2-0	44	X
6Eh	R/W	Zone 3 Hysteresis	H3-3	H3-2	H3-1	H3-0	RES	RES	RES	RES	40	X

If the temperature is above Fan Temp Limit, then drops below Fan Temp Limit, the following will occur:

- The fan will remain on, at Fan PWM Minimum, until the temperature goes a certain amount below Fan Temp Limit.
- The Hysteresis registers control this amount. See below table for details, all values from 0°C to 15°C are possible.

This register becomes read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to these registers shall have no effect.

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Temperature	Zone Hysteresis Hn-[3:0]
0°C	0000
1°C	0001
4°C (default)	0100
10°C	1010
15°C	1111

**Table 19 Zone Hysteresis Register Format**
**Register 75h: Fan Spin-Up Mode**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
75h	R/W	Fan Spin-Up Mode	Tach4 Disable	Tach3/4 Disable	Tach2 Disable	Tach1 Disable	RES	PWM3 SU	PWM2 SU	PWM1 SU	00	X

The PWM SU bit configures the PWM spin-up mode. If PWM SU is cleared the spin-up time will terminate after time programmed by the Fan Configuration register has elapsed. When set to 1, the spin-up time will terminate early if the TACH reading interpreted as RPM exceeds the Tach Minimum RPM value or after the time programmed by the Fan Configuration register has elapsed, which ever occurs first. Note that the magnitudes of the tach readings and the limits in the registers represent a time period that is inversely proportional to RPM.

This register becomes Read-only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this register shall have no effect.

**Miscellaneous Registers**
**Register 3Eh: Company ID**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Eh	R	Company ID	7	6	5	4	3	2	1	0	61

The company ID register contains the company identification number. For Andigilog this is 61h. This number is assigned by Intel and is a method for uniquely identifying the part manufacturer. This register is read-only – a write to this register has no effect.

**Register 3Fh: Version/Stepping**

Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
3Fh	R	Version/Stepping	VER3	VER2	VER1	VER0	STP3	STP2	STP1	STP0	69

The four least significant bits of the Version/Stepping register [3:0] contain the current stepping of the aSC7611 silicon. The four most significant bits [7:4] reflect the aSC7611 base device number when set to a value of 0110b. For the aSC7611, this register will read 01101001b (69h).

The register is used by application software to identify which device in the hardware monitor family has been implemented in the given system. Based on this information, software can determine which registers to read from and write to. Further, application software may use the current stepping to implement work-around for bugs found in a specific silicon stepping.

This register is read-only – a write to this register has no effect.

**Register 6Fh: Test Register**

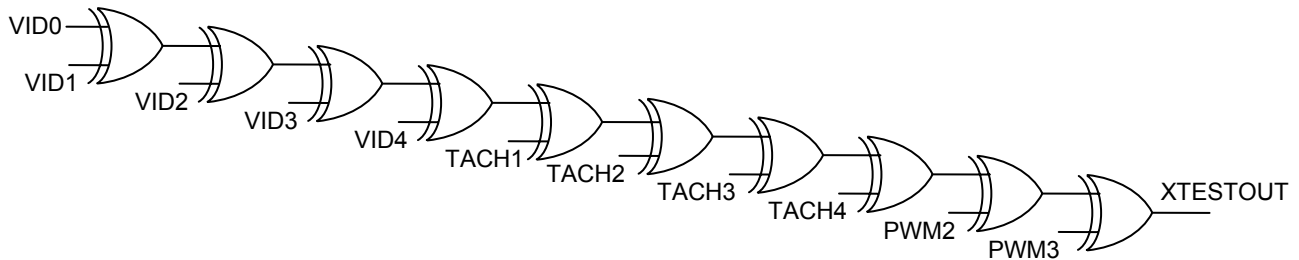
Register Address	Read/Write	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value	Lock
6Fh	R/W	Test Register	RES	RES	RES	RES	RES	RES	RES	XEN	00h	X

**XOR Tree Test**

The aSC7611 incorporates a XOR tree test mode. When the test mode is enabled by setting the “XEN” bit high in the Test Register at address 6Fh via the SMBus, the part will enter XOR test mode.

Since the test mode an XOR tree, the order of the signals in the tree is not important. SMBDAT and SMBCLK are not to be included in the test tree.

This register becomes Read-Only when the Ready/Lock/Start/Override register Lock bit is set. Any further attempts to write to this registers shall have no effect.



**Register 70-7Fh: Vendor Specific Registers**

These registers are for vendor specific features, including test registers. They will not default to a specific value on power up.

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## Applications Information

### Remote Diodes

The aSC7611 is designed to work with a variety of remote sensors in the form of the substrate thermal diode of a CPU or graphics controller or a diode-connected transistor. Actual diodes are not suited for these measurements.

There is some variation in the performance of these diodes, described in terms of its departure from the ideal diode equation. This factor is called diode non-ideality,  $nf$ .

The equation relating diode temperature to a change in thermal diode voltage with two driving currents is:

$$\Delta V_{BE} = (nf) \frac{KT}{q} \ln(N)$$

where:

- $nf$  = diode non-ideality factor, (nominal 1.009).
- $K$  = Boltzman's constant, ( $1.38 \times 10^{-23}$ ).
- $T$  = diode junction temperature in Kelvins.
- $q$  = electron charge ( $1.6 \times 10^{-19}$  Coulombs).
- $N$  = ratio of the two driving currents (16).

The aSC7611 is designed and trimmed for an expected  $nf$  value of 1.009, based on the typical value for the Intel Pentium™ III and AMD Athlon™. There is also a tolerance on the value provided. The values for other CPUs and the 2N3904 may have different nominal values and tolerances. Consult the CPU or GPU manufacturer's data sheet for the  $nf$  factor. Table 20 gives a representative sample of what one may expect in the range of non-ideality. The trend with CPUs is for a lower value with a larger spread.

When thermal diode has a non-ideality factor other than 1.009 the difference in temperature reading at a particular temperature may be interpreted with the following equation:

$$T_{actual} = T_{reported} \left( \frac{1.009}{n_{actual}} \right)$$

where:

- $T_{reported}$  = reported temperature in temperature register.
- $T_{actual}$  = actual remote diode temperature.
- $n_{actual}$  = selected diode's non-ideality factor,  $nf$ .
- Temperatures are in Kelvins or °C + 273.15.

This equation assumes that the series resistance of the remote diode is the same for each. This resistance is given in the data sheet for the CPU and may vary from 2.5Ω to 4.5Ω.

Although the temperature error caused by non-ideality difference is directly proportional to the difference from 1.008, but a small difference in non-ideality results in a relatively large difference in temperature reading. For example, if there were a ±1% tolerance in the non-ideality of a diode it would result in a ±2.7 degree difference (at 0°C) in the result ( $0.01 \times 273.15$ ).

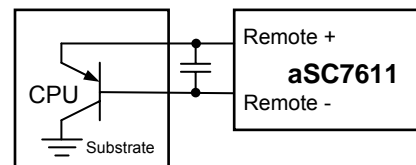
This difference varies with temperature such that a fixed offset value may only be used over a very narrow range. Typical correction method required when measuring a wide range of temperature values is to scale the temperature reading in the host firmware.

Part	$nf$ Min	$nf$ Nom	$nf$ Max	Series Res
Pentium™ III (CPUID 68h)	1.0057	1.008	1.0125	
Pentium 4, 130nM	1.001	1.002	1.003	3.64
Pentium 4, 90nM		1.011		3.33
Pentium 4, 65nM		1.009		4.52
Intel Pentium M	1.0015	1.0022	1.0029	3.06
AMD Athlon™ Model 6	1.002	1.008	1.016	
AMD Duron™ Models 7 and 8	1.002	1.008	1.016	
AMD Athlon Models 8 and 10	1.0000	1.0037	1.0090	
2N3904	1.003	1.0046	1.005	

**Table 20 Representative CPU Thermal Diode and Transistor Non-Ideality Factors**

### CPU or ASIC Substrate Remote Diodes

A substrate diode is a parasitic PNP transistor that has its collector tied to ground through the substrate and the base (Remote -) and emitter (Remote +) brought out to pins. Connection to these pins is shown in Figure 11. The non-ideality figures in Table 20 include the effects of any package resistance and represent the value seen from the CPU socket. The temperature indicated will need to be compensated for the departure from a non-ideality of 1.008.



**Figure 11 CPU Remote Diode Connection**

## Series Resistance

Any external series resistance in the connections from the aSC7611 to the CPU pins should be accounted for in interpreting the results of a measurement.

The impact of series resistance on the measured temperature is a result of measurement currents developing offset voltages that add to the diode voltage. This is relatively constant with temperature and may be corrected with a fixed value in the offset register. To determine the temperature impact of resistance is as follows:

$$\Delta T_R = R_S \times \Delta I_D / T_V$$

or,

$$\Delta T_R = R_S \times \frac{90\mu A}{230\mu V / ^\circ C} = R_S \times 0.39 ^\circ C / \Omega$$

where:

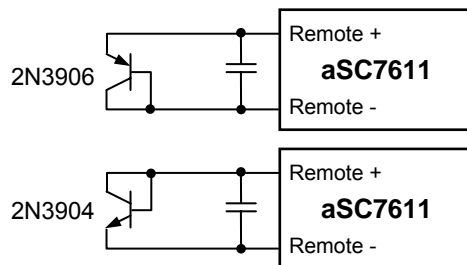
- $\Delta T_R$  = difference in the temperature reading from actual.
- $R_S$  = total series resistance of interconnect (both leads).
- $\Delta I_D$  = difference in the two diode current levels (90 $\mu$ A).
- $T_V$  = scale of temperature vs.  $V_{BE}$  (230 $\mu$ V/ $^\circ$ C).

For example, a total series resistance of 10 $\Omega$  would give an offset of +3.9 $^\circ$ C.

## Discrete Remote Diodes

When sensing temperatures other than the CPU or GPU substrate, an NPN or PNP transistor may be used. Most commonly used are the 2N3904 and 2N3906. These have characteristics similar to the CPU substrate diode with non-ideality around 1.0046. They are connected with base to collector shorted as shown in Figure 12.

While it is important to minimize the distance to the remote diode to reduce high-frequency noise pickup, they may be located many feet away with proper shielding. Shielded, twisted-pair cable is recommended, with the shield connected only at the aSC7611 end as close as possible to the ground pin of the device.



**Figure 12 Discrete Remote Diode Connection**

As with the CPU substrate diode, the temperature reported will be subject to the same errors due to non-ideality variation and series resistance. However, the

transistor's die temperature is usually not the temperature of interest and care must be taken to minimize the thermal resistance and physical distance between that temperature and the remote diode. The offset and response time will need to be characterized by the user.

## Board Layout Considerations

The distance between the remote sensor and the aSC7611 should be minimized. All wiring should be defended from high frequency noise sources and a balanced differential layout maintained on Remote + and Remote -.

Any noise, both common-mode and differential, induced in the remote diode interconnect may result in an offset in the temperature reported. Circuit board layout should follow the recommendation of Figure 13. Basically, use 10-mil lines and spaces with grounds on each side of the differential pair. Choose the ground plane closest to the CPU when using the CPU's remote diode.



**Figure 13 Recommended Remote Diode Circuit Board Interconnect**

Noise filtering is accomplished by using a bypass capacitor placed as close as possible to the two pairs of aSC7611 Remote + and Remote - pins. A 1.0nF ceramic capacitor is recommended, but up to 3.3nF may be used. Additional filtering takes place within the aSC7611.

It is recommended that the following guidelines be used to minimize noise and achieve highest accuracy:

1. Place a 0.1 $\mu$ F bypass capacitor to digital ground as close as possible to the power pin of the aSC7611.
2. Match the trace routing of the Remote + and Remote - leads and use a 1.0nF filter capacitor close to the aSC7611. Use ground runs along side the pair to minimize differential coupling as in Figure 13.
3. Place the aSC7611 as close to the CPU or GPU remote diode leads as possible to minimize noise and series resistance.
4. Avoid running diode connections close to or in parallel with high-speed busses or 12V, staying at least 2cm away.
5. Avoid running diode connections close to on-board switching power supply inductors.

6. PC board leakage should be minimized by maintaining minimum trace spacing and covering traces over their full length with solder mask.

### Thermal Considerations

The temperature of the aSC7611 will be close to that of the PC board on which it is mounted. Conduction through the leads is the primary path for heat flow. The reported local sensor is very close to the circuit board temperature and typically between the board and ambient.

In order to measure PC board temperature in an area of interest, such as the area around the CPU where voltage regulator components generate significant heat, a remote diode-connected transistor should be used. A surface-mount SOT-23 or SOT-223 is recommended. The small size is advantageous in minimizing response time because of its low thermal mass, but at the same time it has low surface area and a high thermal resistance to ambient air. A compromise must be achieved between minimizing thermal mass and increasing the surface area to lower the junction-to-ambient thermal resistance.

In order to sense temperature of air-flows near board-mounted heat sources, such as memory modules, the sensor should be mounted above the PC board. A TO-92 packaged transistor is recommended.

The power consumption of the aSC7611 is relatively low and should have little self-heating effect on the local sensor reading. At the highest measurement rate the dissipation is less than 2mW, resulting in only a few tenths of a degree rise.

### Evaluation Board

The Andigilog SMBus EVB provides a platform for evaluation of the operational characteristics of the aSC7511, aSC7512 and aSC7611. The board features a graphical user interface (GUI) to control and monitor all activities and readings of these parts. The provided software will run on a Windows XP™-based desktop or laptop PC with a USB port.

In addition to being a self-contained fan speed control demonstration, it may be connected into an operating PC's fan and CPU diode to evaluate various settings under real operating conditions without the need to adjust

BIOS code. After optimization, the settings may then be programmed into the BIOS.

#### Features:

- Interactive GUI for setting limits and operational configuration
- aSC7512 and aSC7611 Automatic Fan Control
- Powered and operated from the USB port
- Support for reading or writing to any register
- User-defined, time-stamped logging of any registers, saved in spreadsheet-compatible format
- Graphical readouts:
  - Temperature and alarms
  - Fan RPM
  - Automatic fan control state
  - Voltage
- Selectable on-board 2N3904 or wired remote diode
- Headers for 2-, 3- and 4-wire fans with PWM drive for aSC7512
- Headers for up to 3 4-wire fans for aSC7611
- Saving and recalling of full register set configurations
- LED indicators of alarm pin states
- Optional use of external 12V fan power for higher current fans
- Optional connection to off-board SMBus clients

### Application Diagram

The aSC7611 may be easily adapted to two-, three- or 4-wire fans for precise, wider-range fan speed control when compared to variable DC drive. Up to four fans may be controlled. Fans 1 and 2 are independent. Fan 3 is independent and may be tied to fan 4 for speed control. Separate tachometer readings may be reported for all four.

Application diagram in Figure 14 shows connections to four 4-wire fans. External FETs may be added to the PWM output to drive 3-wire fans.

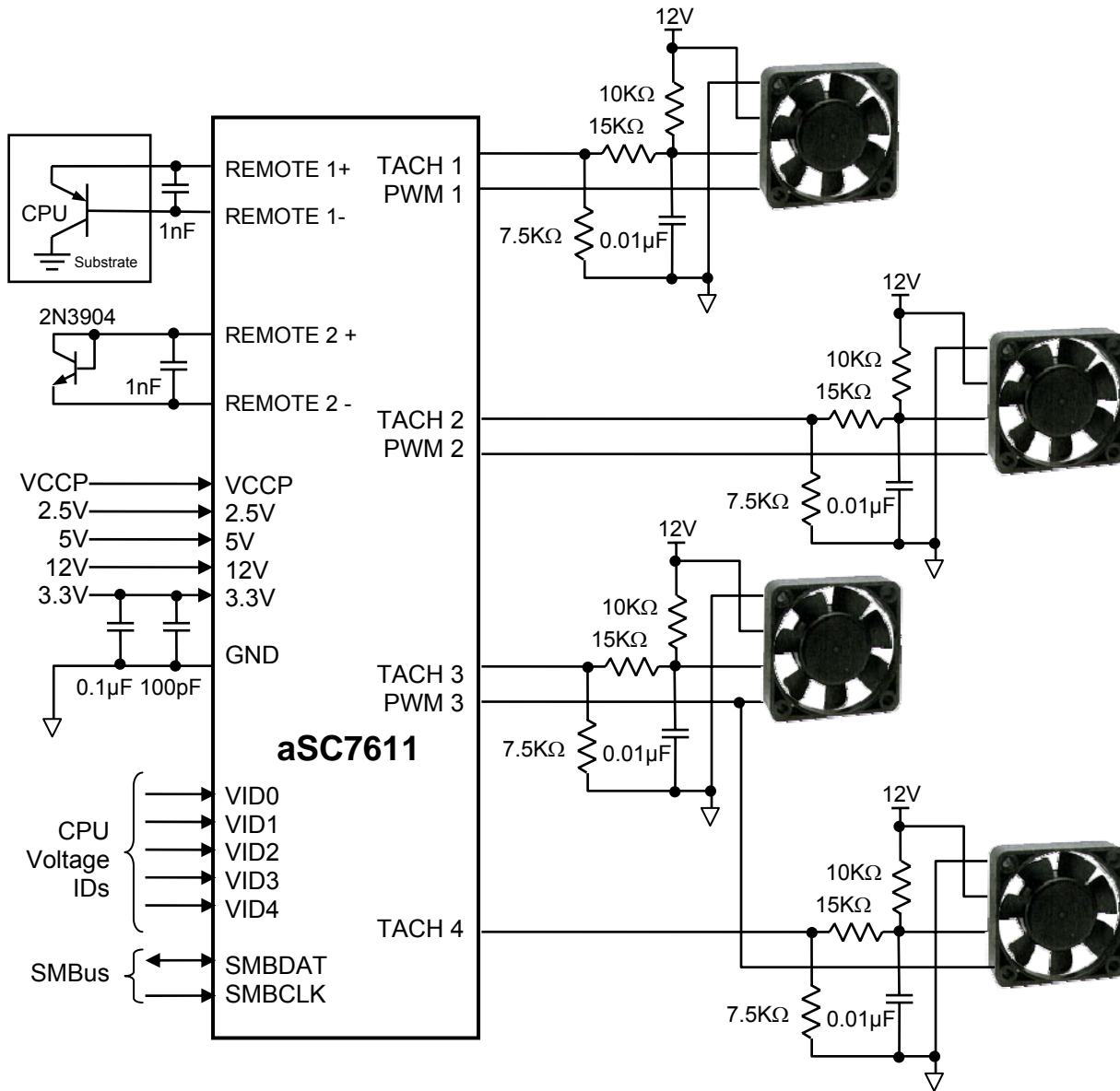


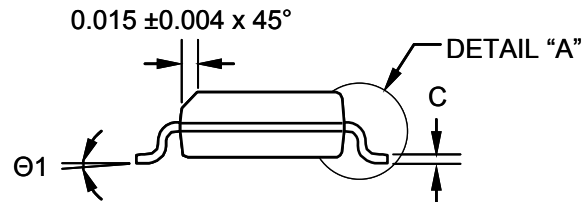
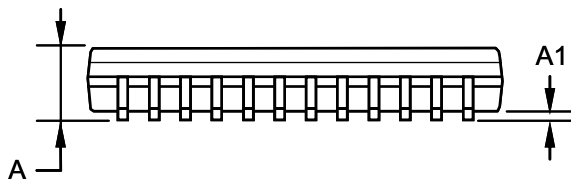
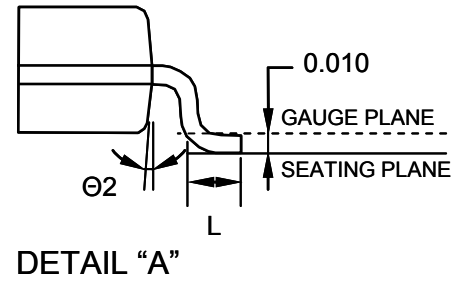
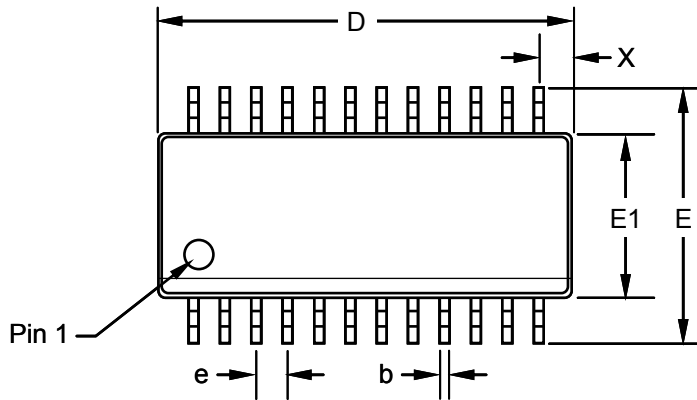
Figure 14 Application Diagram

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**Physical Dimensions** inches unless otherwise noted

**24-Lead Molded QSOP Package**



**Notes:**

1. Pb-Free
2. Co-planarity is 0 to 0.004" MAX
3. Package surface finish – Matte (VDI #24~27)
4. All dimensions exclude mold flash
5. The lead width, B, to be determined at 0.0075" from the lead tip

Symbol	MIN	MAX
A	0.054	0.068
A1	0.004	0.0098
B	0.008	0.012
D	0.337	0.344
E1	0.150	0.157
E	0.229	0.244
E	0.025 BSC	
C	0.0075	0.0098
L	0.016	0.034
X	0.0325 REF	
Θ1	0°	8°
Θ2	7° BSC	

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