

MOS FIELD EFFECT TRANSISTOR 2SJ492

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converters and motor/lamp driver circuits.

FEATURES

• Low on-state resistance

RDS(on)1 = 100 $m\Omega$ (MAX.) (VGS = -10 V, ID = -10 A)

RDS(on)2 = 185 m Ω (MAX.) (VGS = -4 V, ID = -10 A)

- Low Ciss: Ciss = 1210 pF (TYP.)
- · Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SJ492	TO-220AB
2SJ492-S	TO-262
2SJ492-ZJ	TO-263

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vss = 0 V)	VDSS	-60	V
Gate to Source Voltage (Vps = 0 V)	VGSS(AC)	∓ 20	V
Gate to Source Voltage (Vps = 0 V) Note1	VGSS(DC)	-20, 0	V
Drain Current (DC)	I _{D(DC)}	∓ 20	Α
Drain Current (pulse) Note2	D(pulse)	∓ 80	Α
Total Power Dissipation (T _A = 25°C)	PT	1.5	W
Total Power Dissipation (Tc = 25°C)	PT	70	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current Note3	las	-20	Α
Single Avalanche Energy Note3	Eas	40	mJ

Notes 1. f = 20 kHz, Duty Cycle $\leq 10\%$ (+Side)

- **2.** PW \leq 10 μ s, Duty Cycle \leq 1 %
- 3. Starting T_{ch} = 25 °C, R_A = 25 Ω , V_{GS} = -20 V \rightarrow 0

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.79	°C/W
Channel to Ambient	Rth(ch-A)	83.3	°C/W

The information in this document is subject to change without notice.

Document No. Date Published Printed in Japan

D11264EJ1V0DS00 (1st edition) December 1998 NS CP(K)

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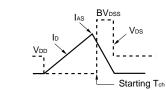


ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

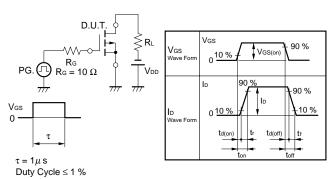
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = -10 V, ID = -10 A		70	100	mΩ
	RDS(on)2	Vgs = -4 V, ID = -10 A		120	185	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0	-1.5	-2.0	V
Forward Transfer Admittance	yfs	V _{DS} = -10 V, I _D = -10 A	5.0	12		S
Drain Leakage Current	Ipss	V _{DS} = -60 V, V _{GS} = 0 V			-10	μΑ
Gate to Source Leakage Current	Igss	$Vgs = \mp 20 V$, $Vps = 0 V$			∓ 10	μΑ
Input Capacitance	Ciss	Vps = -10 V		1210		pF
Output Capacitance	Coss	Vgs = 0 V		520		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		180		pF
Turn-on Delay Time	td(on)	I _D = -10 A		16		ns
Rise Time	t r	$V_{GS(on)} = -10 \text{ V}$		140		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = -30 V		90		ns
Fall Time	tf	$R_G = 10 \Omega$		80		ns
Total Gate Charge	Q _G	I _D = -20 A		42		nC
Gate to Source Charge	Qgs	V _{DD} = -48 V		8.0		nC
Gate to Drain Charge	QGD	Vgs = −10 V		10		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = -20 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = -20 A, VGS = 0 V		125		ns
Reverse Recovery Charge	Qrr	$di/dt = 50 A/\mu s$		280		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} & D.U.T. \\ \hline R_G = 25 \ \Omega \\ \hline > 50 \ \Omega \\ \hline \\ V_{GS} = -20 \rightarrow 0 \ V \\ \hline \end{array}$

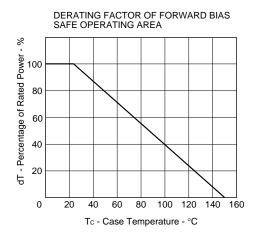


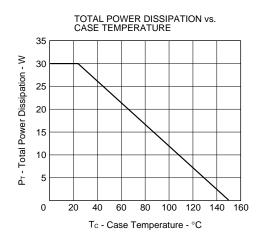
TEST CIRCUIT 2 SWITCHING TIME

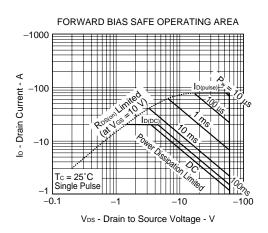


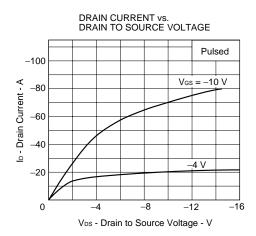
TEST CIRCUIT 3 GATE CHARGE

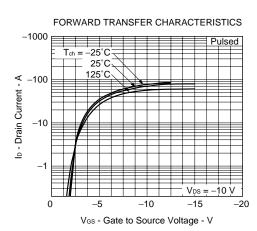
TYPICAL CHARACTERISTICS (TA = 25 °C)



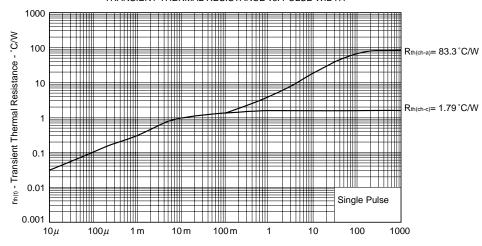






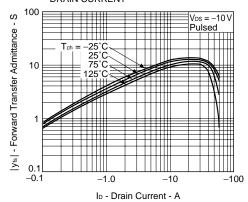


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

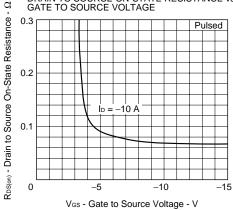


PW - Pulse Width - s

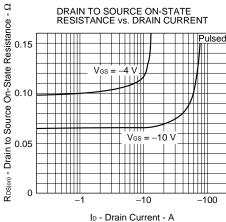
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



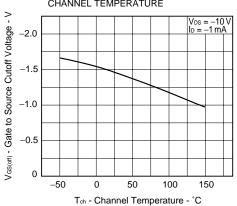


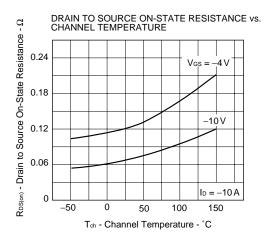


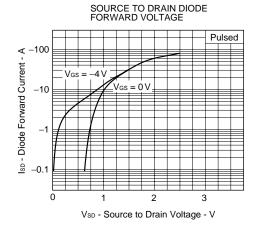
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

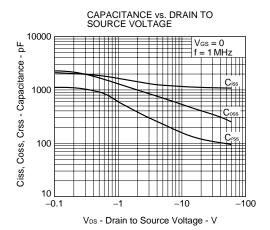


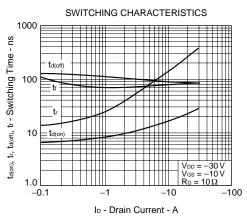
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

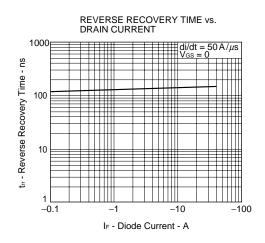


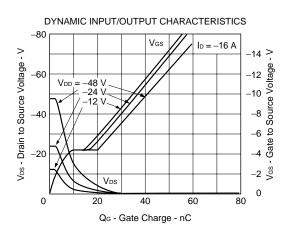


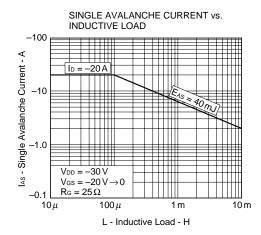


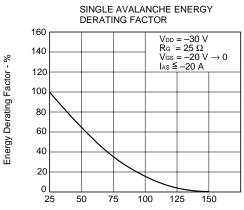










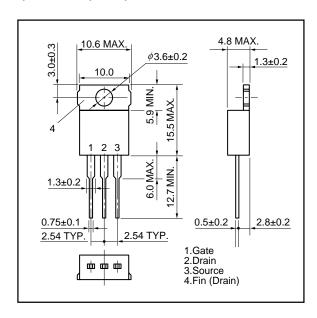


Starting Tch - Starting Channel Temperature - °C

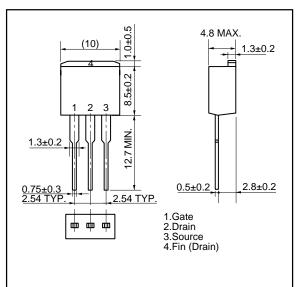


PACKAGE DRAWING (Unit: mm)

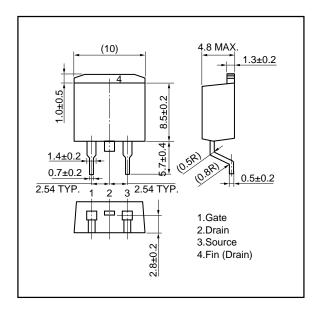
1) TO-220AB (MP-25)



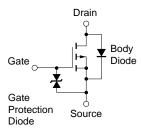
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (JEDEC TYPE: MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.

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