

BUK9608-55B

N-channel TrenchMOS logic level FET

Rev. 04 — 4 May 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C};$ see Figure 1 ; see Figure 3	[1]	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	203	W

Static characteristics

R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C}$	-	6.2	7	m Ω
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 11 ; see Figure 12	-	7.1	8.4	m Ω



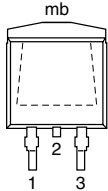
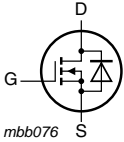
Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	-	-	352	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 44\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 13	-	16	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9608-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404
BUK9608-55B/C1	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

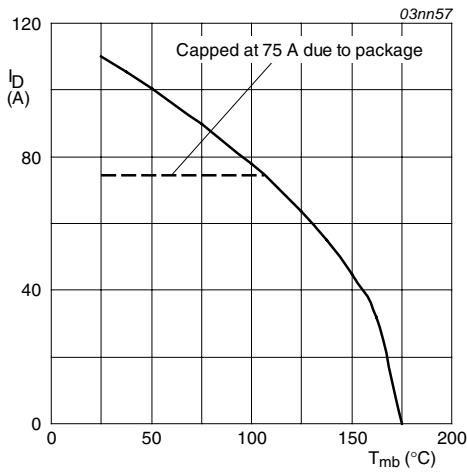
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-	55	V
V_{GS}	gate-source voltage		-15	-	15	V
I_D	drain current	$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1	[1]	-	75	A
		$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ;	[2]	-	110	A
		see Figure 3	[1]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	-	439	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	203	W
T_{stg}	storage temperature		-55	-	175	°C
T_j	junction temperature		-55	-	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[2]	-	110	A
			[1]	-	75	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	-	439	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$; $V_{sup} \leq 55\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	352	mJ

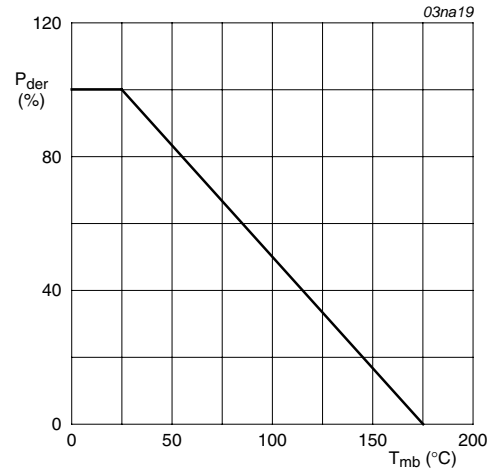
[1] Continuous current is limited by package.

[2] Current is limited by power dissipation chip rating.



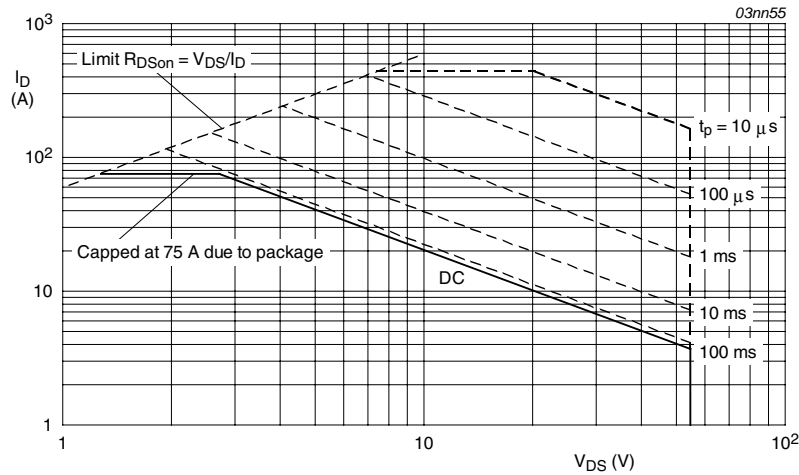
$$V_{GS} \geq 5V$$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.74	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a PCB	-	50	-	K/W

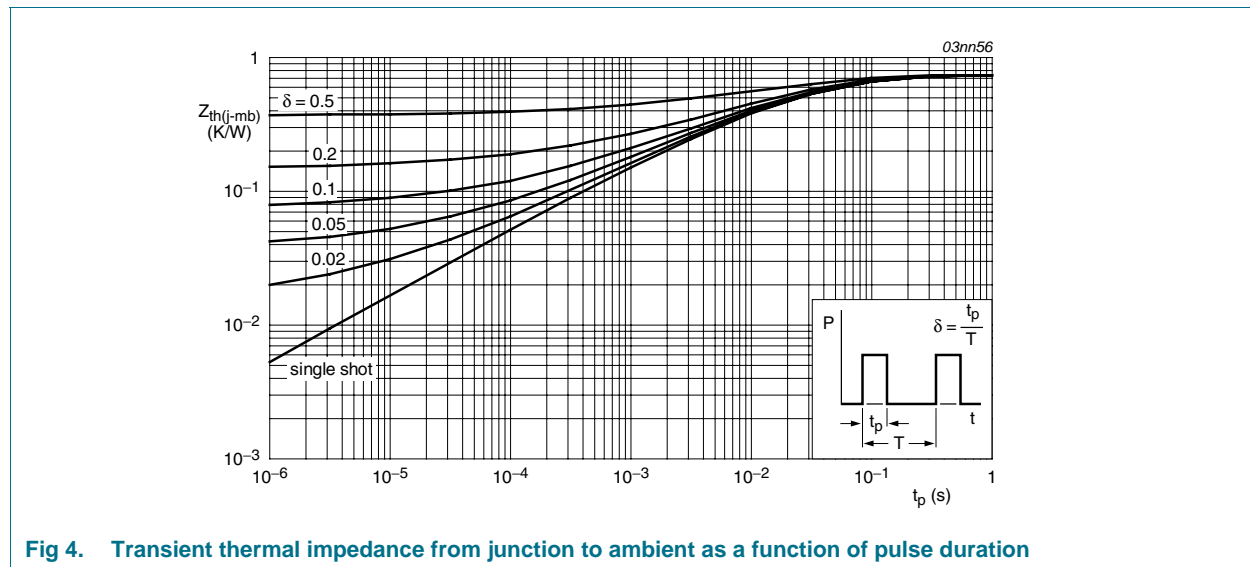


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration

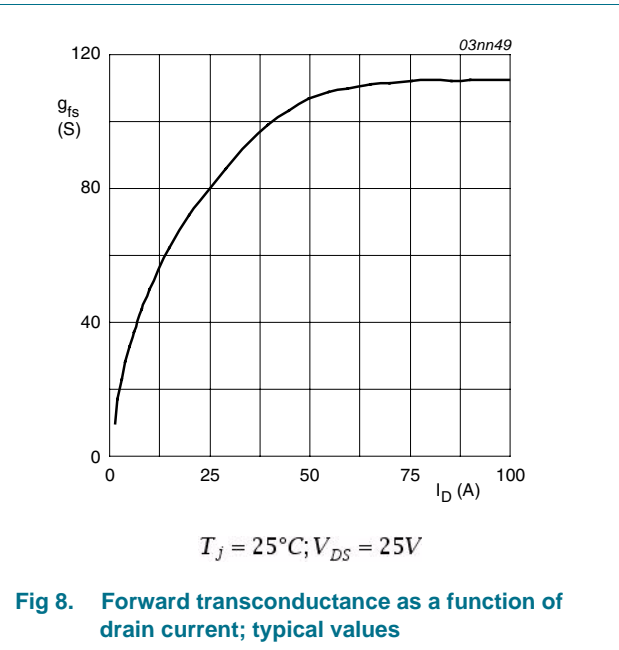
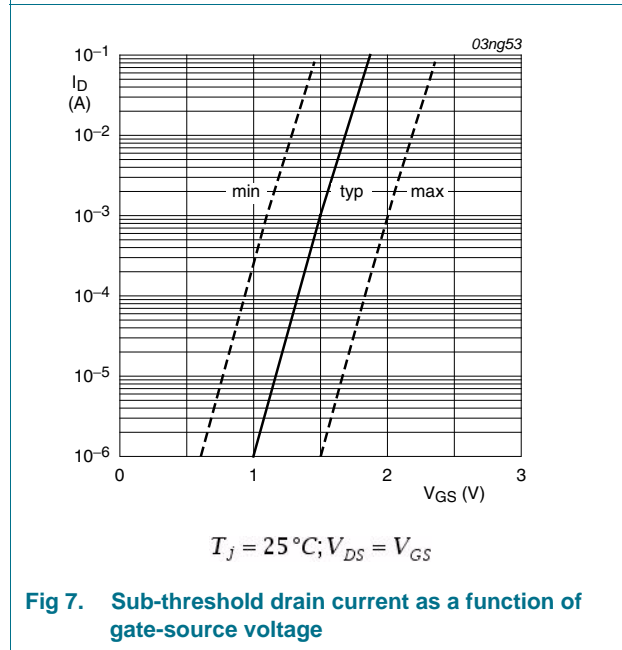
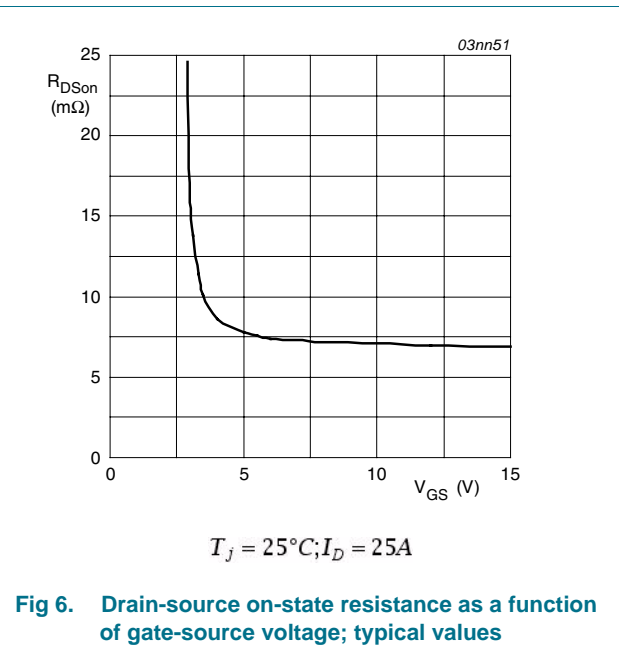
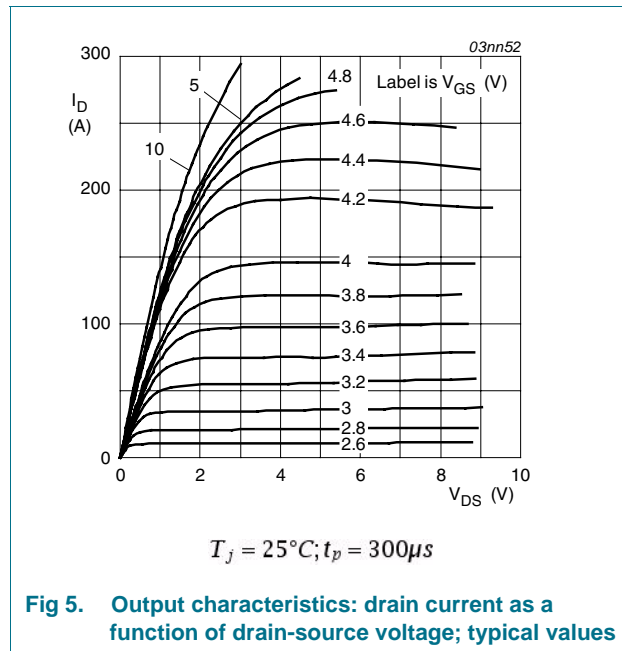
6. Characteristics

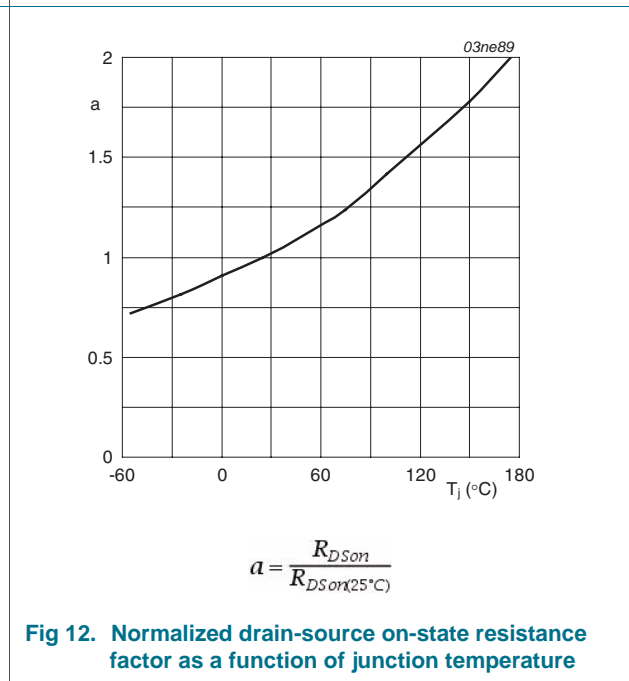
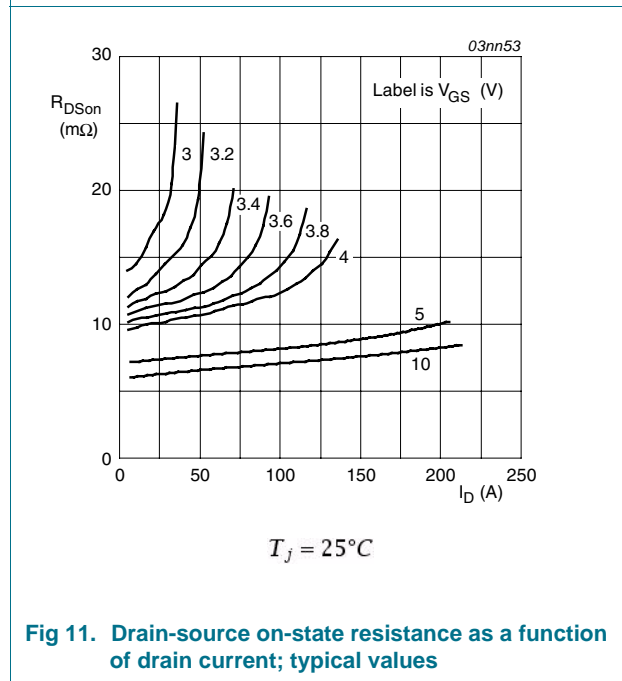
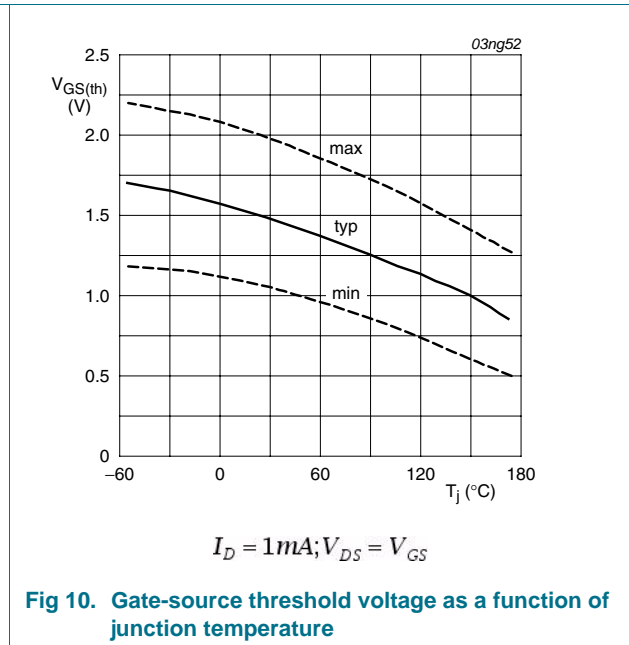
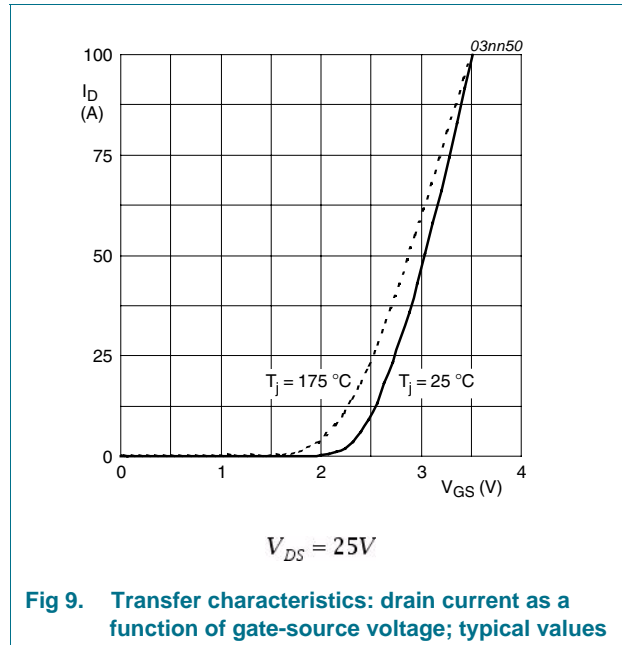
Table 6. Characteristics

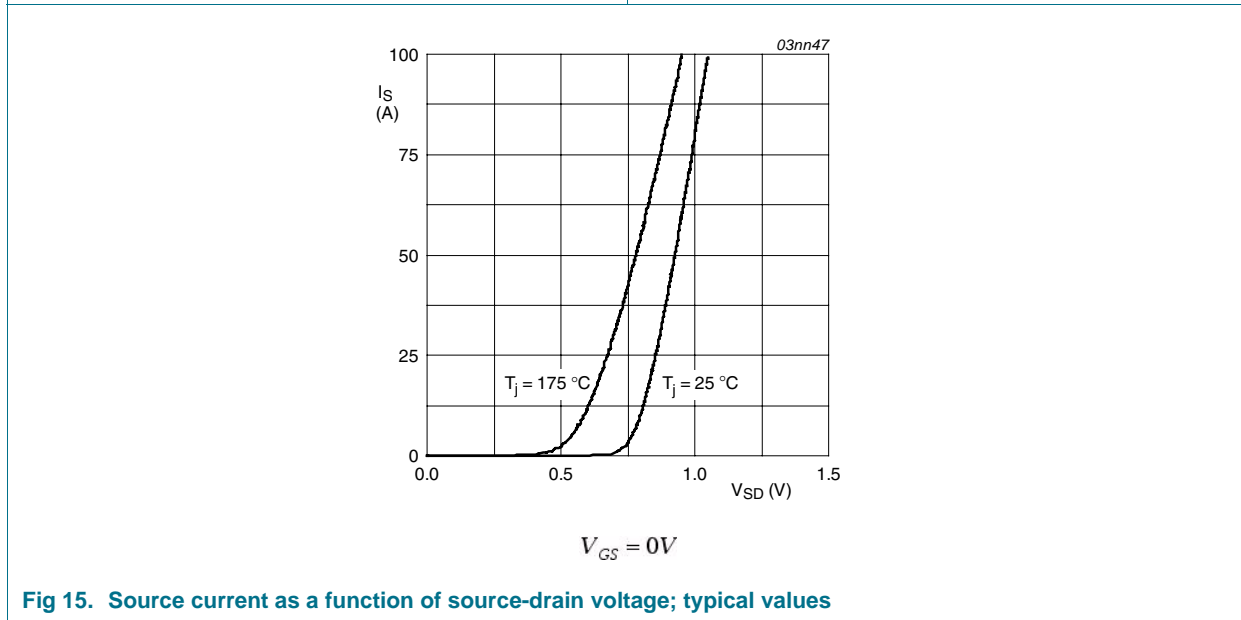
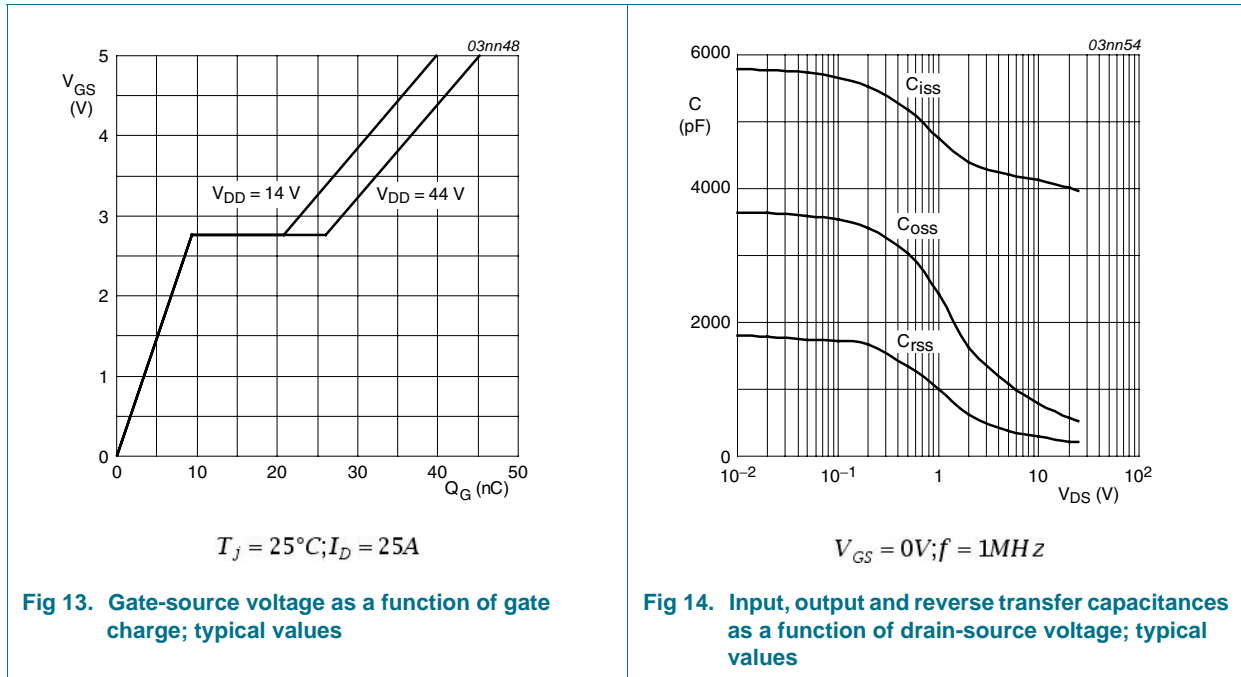
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10	1.1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	-	9.3	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 12	-	-	16.8	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	6.2	7	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 12	-	7.1	8.4	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	45	-	nC
Q_{GS}	gate-source charge		-	9	-	nC
Q_{GD}	gate-drain charge		-	16	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	3960	5280	pF
C_{oss}	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	517	620	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 14	-	206	282	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }^\circ\Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	29	-	ns
t_r	rise time		-	123	-	ns
$t_{d(off)}$	turn-off delay time		-	131	-	ns
t_f	fall time		-	86	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to center of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
		from upper edge of drain mounting base to center of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$;	-	69	-	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	72	-	nC







7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

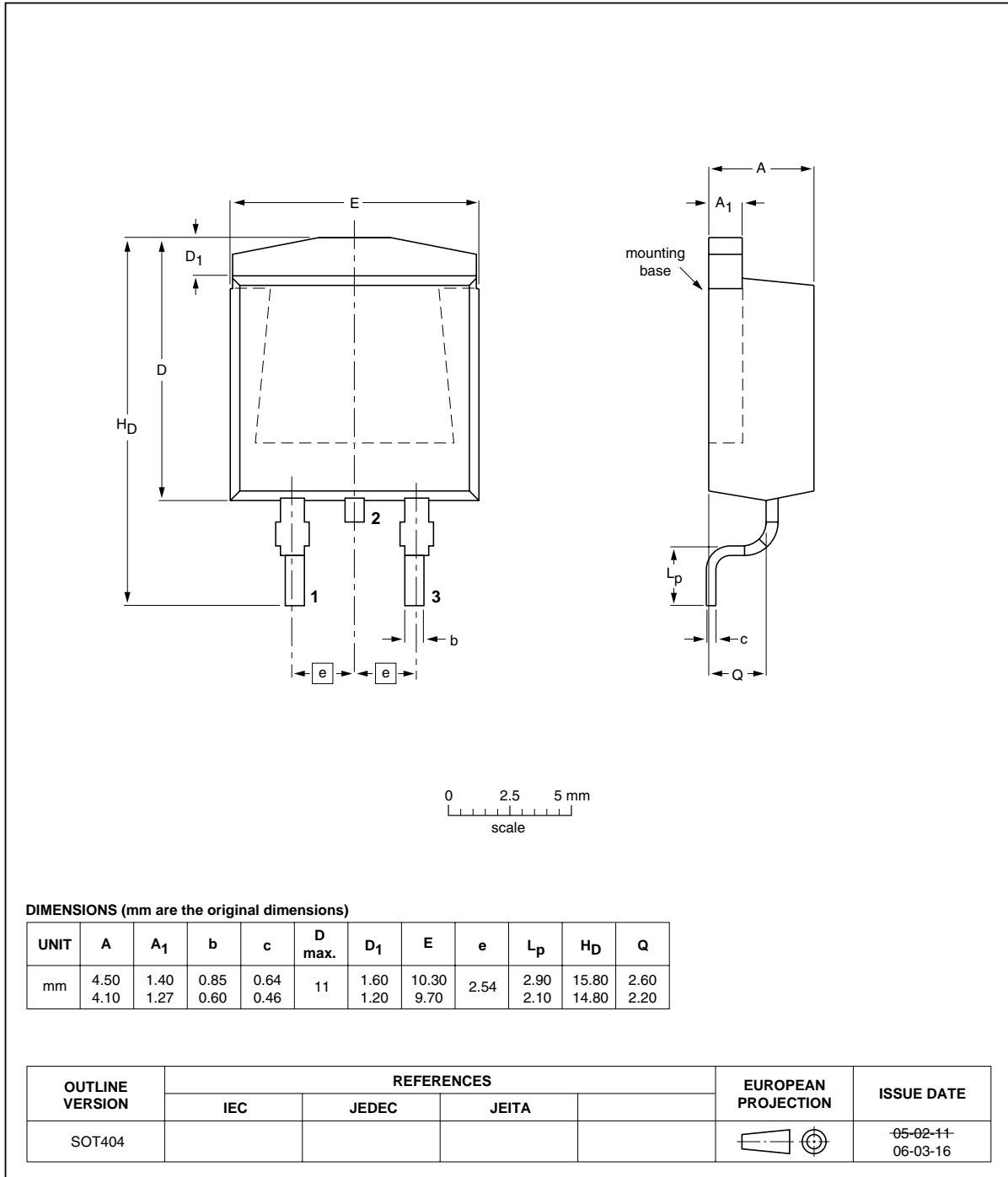


Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9608-55B_4	20100504	Product data sheet	-	BUK9608-55B_3
Modifications:	• Various changes to content.			
BUK9608-55B_3	20100429	Product data sheet	-	BUK95_96_9E08_55B-02

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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