FAIRCHILD SEMICONDUCTOR®

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# FDS4470

## 40V N-Channel PowerTrench® MOSFET

### General Description

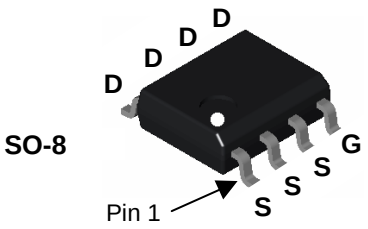
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

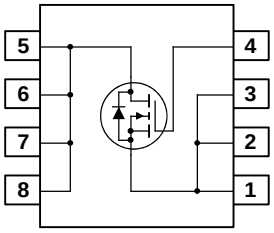
### Applications

- DC/DC converter

### Features

- 12.5 A, 40 V. $R_{DS(ON)}$ = 9 mΩ @ $V_{GS}$ = 10 V
- Low gate charge (45 nC)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 40 | V |
| $V_{GSS}$ | Gate-Source Voltage | | +30/–20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 12.5 | A |
| | – Pulsed | | 50 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.4 | |
| | | (Note 1c) | 1.2 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +175 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1c) | 125 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS4470 | FDS4470 | 13” | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings** (Note 2) | | | | | | |
| $E_{AS}$ | Drain-Source Avalanche Energy | Single Pulse, $V_{DD}$=40V, $I_D$=12.5A | | | 370 | mJ |
| $I_{AS}$ | Drain-Source Avalanche Current | | | | 12.5 | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 42 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 32 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 30 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –20 V, $V_{DS}$ = 0 V | | | –100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 2 | 3.9 | 5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | –8 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 12.5 A<br>$V_{GS}$ = 10 V, $I_D$ = 12.5 A,$T_J$=125°C | | 6<br>9 | 9<br>14 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 25 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 12.5 A | | 45 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 2659 | | pF |
| $C_{oss}$ | Output Capacitance | | | 605 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 298 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 20 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 14 | 25 | ns |
| $t_r$ | Turn–On Rise Time | | | 12 | 22 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 37 | 59 | ns |
| $t_f$ | Turn–Off Fall Time | | | 29 | 46 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 20 V, $I_D$ = 12.5 A, $V_{GS}$ = 10 V | | 45 | 63 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 11.2 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 11 | | nC |

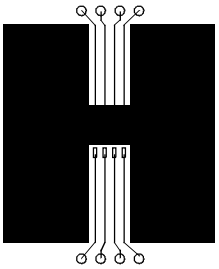
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

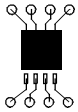
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 2.1 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.7 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 12.5 A, $d_{iF}/d_t$ = 100 A/µs | | 33 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 39 | | nC |

**Notes:**

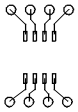
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in$^2$ pad of 2 oz copper



b) 105°C/W when mounted on a .04 in$^2$ pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

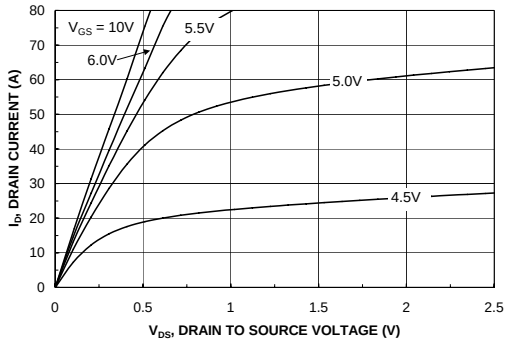



**Figure 1. On-Region Characteristics.**

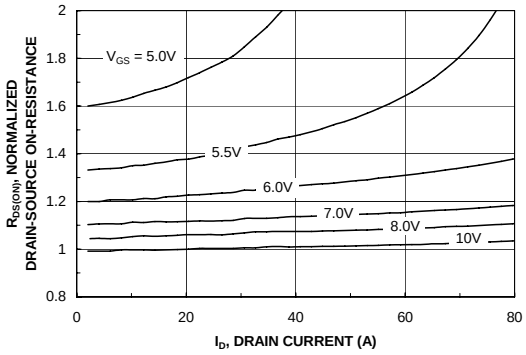



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

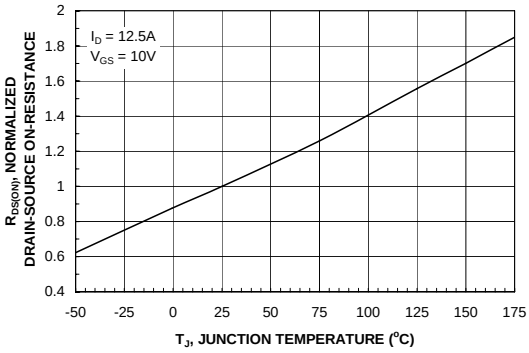



**Figure 3. On-Resistance Variation withTemperature.**

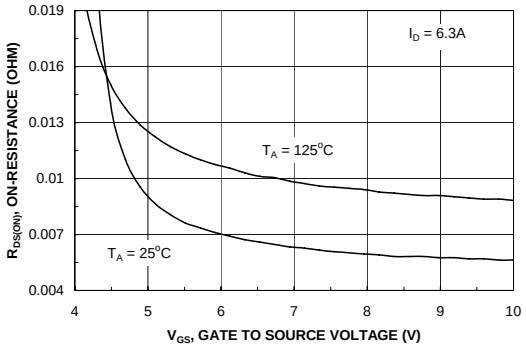



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

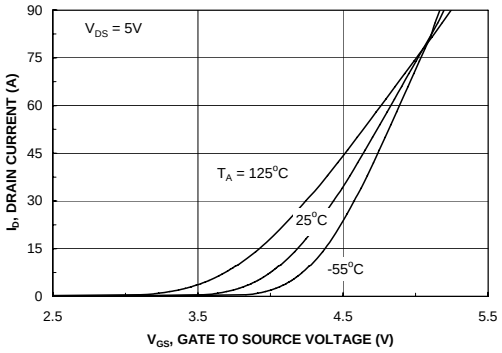



**Figure 5. Transfer Characteristics.**

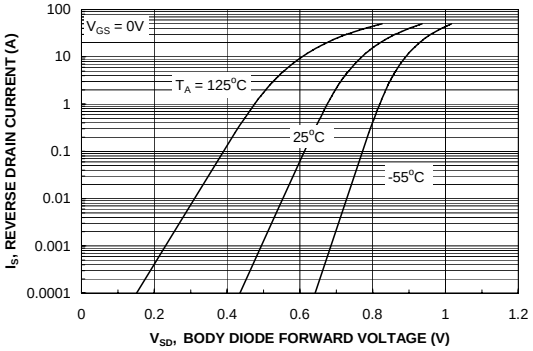



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

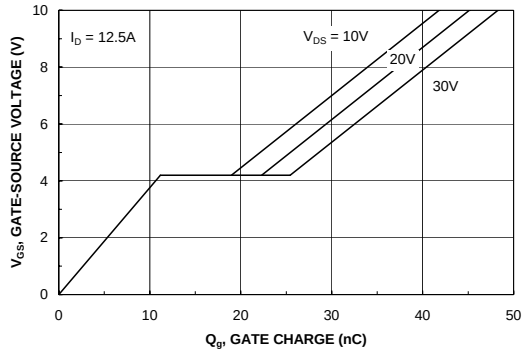



**Figure 7. Gate Charge Characteristics.**

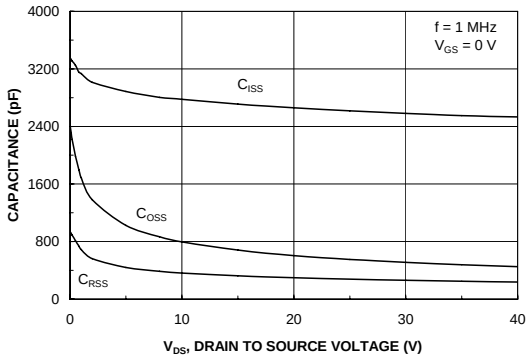



**Figure 8. Capacitance Characteristics.**

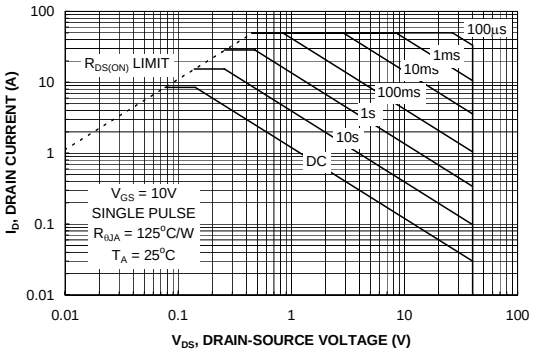



**Figure 9. Maximum Safe Operating Area.**

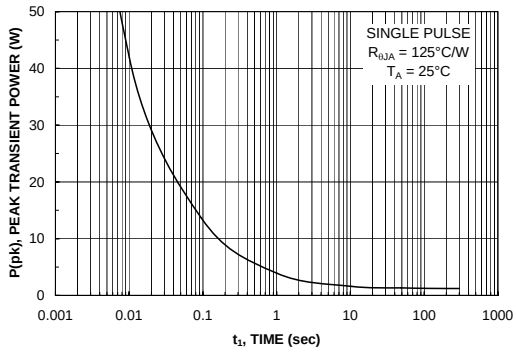



**Figure 10. Single Pulse Maximum Power Dissipation.**

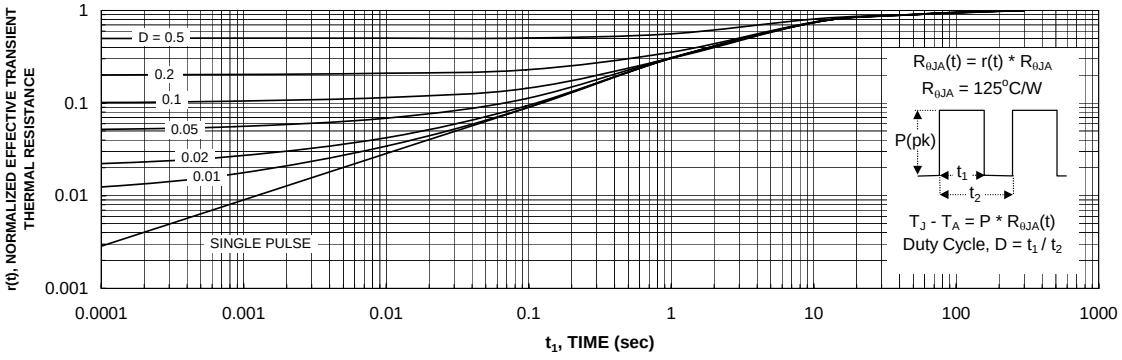



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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