





**NEW Product** 

## DC-DC CONVERTERS Non-isolated DDR/QDR Memory Bus Termination Module

- V<sub>TT</sub> bus termination output (output tracks the system V<sub>REF</sub>)
- 6 A output current (8 A Peak)
- 3.3 Vdc, 5 Vdc or 12 Vdc input voltage
- DDR and QDR compatible
- ON/OFF inhibit (for V<sub>TT</sub> standby)
- Under-voltage lockout
- Operating temperature range: -40 °C to +85 °C
- Efficiencies up to 88%
- · Output overcurrent protection (non-latching, auto-reset)
- Point-of-Load-Alliance (POLA) compatible
- Available RoHS compliant

The PTHxx050Y are a new series of non-isolated dc-dc converters designed specifically for bus termination in DDR and QDR memory applications. Operating from either a 3.3 Vdc, 5 Vdc or 12 Vdc input, the modules generate a V<sub>TT</sub> output that will source or sink up to 6 A of current to accurately track their V<sub>REF</sub> input. V<sub>TT</sub> is the required bus termination supply voltage, and V<sub>REF</sub> is the reference voltage for the memory and chipset bus receiver comparators. V<sub>REF</sub> is usually set to half the V<sub>DDQ</sub> power supply voltage. The PTHxx050Y series employs an actively switched synchronous rectifier output to provide state of the art stepdown switching conversion. The products are small in size and are an ideal choice where space, performance and high efficiency are desired.

All specifications are typical at nominal input,  $V_{REF} = 1.25 V$ , full load at 25 °C unless otherwise stated.  $C_{in}$ ,  $C_{o1}$  and  $C_{o2} =$  typical value

#### **OUTPUT SPECIFICATIONS**

Output current (over V <sub>REF</sub> range)	All models Continuous (See Not Repetitive pulse (See	e 1) ±6 A ±8 A
Tracking range for $\mathrm{V}_{\mathrm{REF}}$		0.55-1.8 V
Tracking tolerance to V <sub>REF</sub> (over line, load and temperature)	(V <sub>TT</sub> - V <sub>REF</sub> )	-10 mV to +10mV
Ripple and noise	20 MHz bandwidth	20 mV pk-pk
Load transient response (See Note 5)	Overshoot/und	80 µs settling time lershoot 25 mV typ.
Output capacitance: Non-ceramic values (See Notes 5 and 6) Ceramic values (See Note 5) (See Note 7)	PTH03050Y     470 µF       PTH05050Y     470 µF       PTH12050Y     940 µF       PTH03050Y     200 µ       PTH05050Y     200 µ       PTH12050Y     400 µ       ESR (non-ceramic)     400 µ	typ., 3,300 μF max. typ., 3,300 μF max. typ., 3,300 μF max. F typ., 300 μF max. F typ., 300 μF max. F typ., 600 μF max. 4 mΩ min

#### INPUT SPECIFICATIONS

Input current	No load	10 mA
Input voltage range	PTH03050Y PTH05050Y PTH12050Y	2.95-3.65 Vdc 4.5-5.5 Vdc 10.8-13.2 Vdc
Undervoltage lockout:		
PTH03050Y	Vin increasing Vin decreasing	2.45 V typ., 2.80 V max. 2.20 V min., 2.40 V typ.
PTH05050Y	Vin increasing Vin decreasing	4.30 V typ., 4.45 V max. 3.40 V min., 3.70 V typ.
PTH12050Y	Vin increasing Vin decreasing	9.5 V typ., 10.4 V max. 8.80 V min., 9.0 V typ.







### SPECIFICATIONS







# nce 3.3/5/12 Vin Single Output

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OUTPUT POWER (MAX.)	INPUT VOLTAGE	V <sub>TT</sub> RANGE	OUTPUT CURRENT (MIN.)	OUTPUT CURRENT (MAX.)	EFFICIENCY (TYP.)	MODEL NUMBER <sup>(9,10)</sup>
10.8 W	2.95-3.65 Vdc	0.55-1.8Vdc	0 A	±6 A	88%	PTH03050Y
10.8 W	4.5-5.5 Vdc	0.55-1.8Vdc	0 A	±6 A	87%	PTH05050Y
10.8 W	10.8-13.2 Vdc	0.55-1.8Vdc	0 A	±6 A	84%	PTH12050Y

#### Part Number System with Options



#### Notes

- 1 Rating is conditional on the module being directly soldered to a 4 layer PCB with 1 oz. copper. See the SOA curves or contact the factory for appropriate derating. The PTH03050Y and PTH05050Y require no derating up to 85 °C operating temperature and natural convection airflow.
- 2 Up to 10 ms pulse period at 10% maximum duty.
- 3 This control pin has an internal pull-up to the input voltage Vin. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult Application Note 178.
- 4 An input capacitor is required for proper operation. The capacitor must be rated for a minimum of 300 mA rms (750 mA rms for 12 V input) of ripple current.
- 5 The typical value of external output capacitance value ensures that V<sub>TT</sub> meets the specified transient performance requirements for the memory bus terminations. Lower values of capacitance may be possible when the measured peak change in output current is consistently less than 3 A. Test conditions were 15 A/µs load step, -1.5 A to +1.5 A.

#### International Safety Standard Approvals



UL/cUL CAN/CSA-C22.2 No. 60950 File No. E174104



TÜV Product Service (EN60950) Certificate No. B 04 06 38572 044 CB Report and Certificate to IEC60950, Certificate No. US/8292/UL

- 6 This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult Application Note 178 for further details.
- 7 This is the typical ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 m  $\!\Omega$  as the minimum when using max ESR values to calculate.
- 8 Tape and reel packaging only available on the surface-mount versions.
- 9 To order Pb-free (RoHS compatible) surface-mount parts replace the mounting option 'S' with 'Z', e.g. PTHxx050YAZ. To order Pb-free (RoHS compatible) through-hole parts replace the mounting option 'H' with 'D', e.g. PTHxx050YAD.
- 10 NOTICE: Some models do not support all options. Please contact your local Artesyn representative or use the on-line model number search tool at http://www.artesyn.com/powergroup/products.htm to find a suitable alternative.







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Figure 1 - Safe Operating Area Vin = 3.3 V, V<sub>REF</sub> = 1.25 V, Iout = 6 A (See Note A)



Figure 3 - Efficiency vs Load Current V<sub>REF</sub> = 1.25 V (See Note B)

#### Notes

- A The SOA curves represent the conditions at which internal components are within the Artesyn derating guidelines.
- B Characteristic data has been developed from actual products tested at 25 °C. This data is considered typical data for the converter.



Figure 2 - Safe Operating Area Vin = 12V,  $V_{REF}$  = 1.25 V, lout = 6 A (See Note A)



Figure 4 - Standard Application







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**PIN CONNECTIONS** 

**FUNCTION** 

Ground

V<sub>REF</sub>

Vin

Inhibit\*

N/C

 $V_{TT}$ 

\*Denotes negative logic: Open = Normal operation Ground = Function active

PIN NO.

1

2

3

4

6



Figure 5 - Plated Through-Hole Mechanical Drawing



Figure 6 - Surface-Mount Mechanical Drawing

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Application Note