Ordering number : EN*5715

Monolithic Linear IC

LA4725

2-Channel BTL Power Amplifier (30 W+30 W) with Standby Switch for Car Stereos

Preliminary

Overview

The LA4725 is a BTL two-channel power IC for car audios developed in pursuit of excellent sound quality. Low-region frequency characteristics have been improved through the use of a new NF capacitorless circuit, and crosstalk which causes "muddy" sound has been reduced by improving both circuit and pattern layout. As a result the LA4725 provides powerful bass and clear treble.

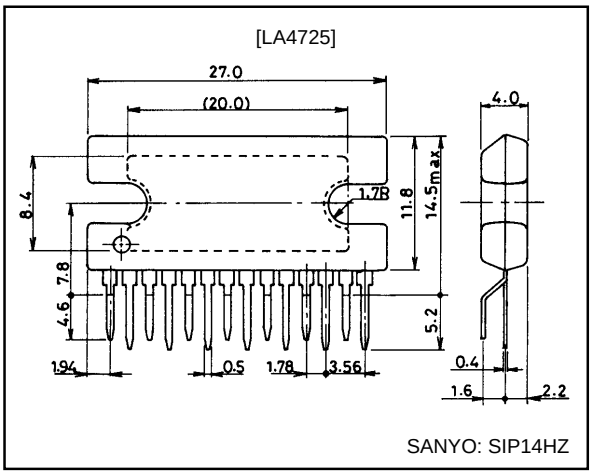
Features

- High power: supports total output of 30 W+30 W. [EIAJ power] (V_{CC}=14.4 V, THD=30 %, R_L=4 Ω)
- Less pop noise.
- Designed for excellent sound quality. (f_L<10 Hz, f_H=130 kHz)
- Any rise time settable by an external capacitor.
- Standby switch circuit on chip. (microcontroller supported)
- Various protectors on chip. (output-to-ground short/ output-to-V_{CC} short/ load short/ overvoltage/ thermal shutdown circuit)
- The LA4725 is pin-compatible with the LA4728.

Package Dimensions

unit: mm

3113A-SIP14HZ



Specifications

Maximum Ratings at Ta = 25 ˚C

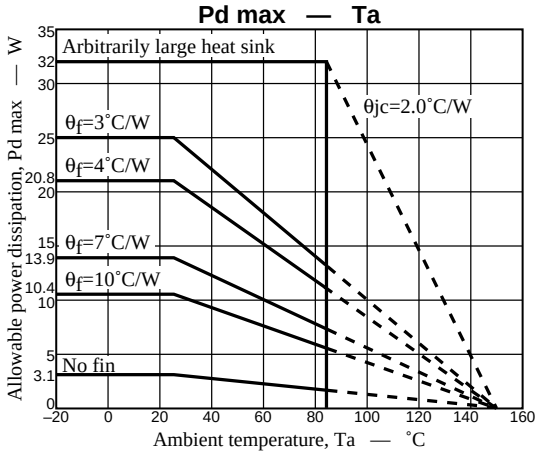
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		18	V
Surge supply voltage	V_{CC} surge	f ≤ 0.2 s, single giant pulse	50	V
Maximum output current	I_O peak	Per channel	3.0	A
Allowable power disspation	Pd max	With arbitrarily large heat sink	32	W
Operating temperature	Topr		–35 to +85	˚C
Storage temperature	Tstg		–40 to +150	˚C

Recommended Conditions at Ta = 25 ˚C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		13.2	V
Operating voltage range	V_{CC} op	Range where Pd max is not exceeded	9 to 16	V
Recommended load resistance	R_L op		4	Ω

Operating Characteristics at Ta = 25 ˚C, V_{CC} = 13.2 V, R_L = 4 kΩ, f = 1 kHz, Rg = 600 Ω

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	Rg=0	70	125	250	mA
Standby current	I_{ST}			10	60	μA
Voltage gain	VG		38	40	42	dB
Total harmonic distortion	THD	P_O=1 W		0.06	0.2	%
Output power	P_{O1}	R_L=4 Ω, THD=10 %, V_{CC}=13.2 V	13	17		W
	P_{O2}	R_L=4 Ω, THD=10 %, V_{CC}=14.4 V		20		W
	P_{O3}	R_L=4 Ω, THD=30 %, V_{CC}=14.4 V		30		W
Output offset voltage	$V_{N\ offset}$	Rg=0	–300		+300	mV
Output noise voltage	V_{NO}	Rg=0, B.P.F.=20 Hz to 20 kHz		0.1	0.5	mVrms
Ripple rejection ratio	SVRR	Rg=0, f_R=100 Hz, V_R=0 dBm	40	50		dB
Channel separation	Chsep	Rg=10 kΩ, V_O=0 dBm	50	60		dB
Input resistance	Ri		21	30	39	kΩ
Standby pin applied voltage	Vst	Amp on, applied through 10 kΩ	2.5		V_{CC}	V



Block Diagram and Sample Application Circuit