ESDALC6V1-1BM2

Single line low capacitance Transil™ for ESD protection

Features

- Single line low capacitance Transil diode
- Bidirectional ESD protection
- ESD protection > 30 kV (IEC 61000-4-2 contact discharge)
- Breakdown Voltage V_{BR} = 6.1 V min.
- Low diode capacitance (22 pF typ. at 0 V)
- Low leakage current: < 100 nA at 3 V
- Very small PCB area: 0.6 mm^2
- Leadfree package

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

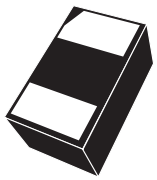
Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3B
  - Human body model

Applications

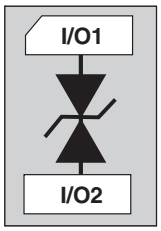
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment



SOD882

Figure 1. Functional diagram



Description

The ESDALC6V1-1BM2 is a bidirectional single line TVS diode designed to protect the datalines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

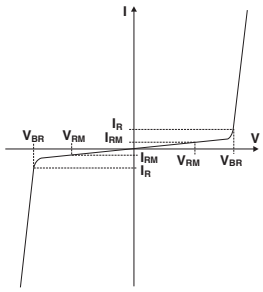
Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}(1)	Peak pulse voltage (IEC 61000-4-2 contact discharge)		± 30	kV
P_{PP}(1)	Peak pulse power dissipation (8/20 µs)	T_j initial = T_{amb}	140	W
I_{PP}	Repetitive peak pulse current (8/20 µs)		9	A
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{OP}	Operating temperature range		- 40 to + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-of voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
V_F	Forward voltage drop



Order code	V_{BR} @ I_R			I_{RM} @ V_{RM}		R_d	αT	C@0 V Bias
	min.	max.		max.		typ.	max.	typ.
	V	V	mA	nA	V	Ω	10^{-4}/°C	pF
ESDALC6V1-1BM2	6.1	8.0	1	100	3	0.65	2.5	22

Figure 2. Relative variation of peak pulse power versus initial junction temperature

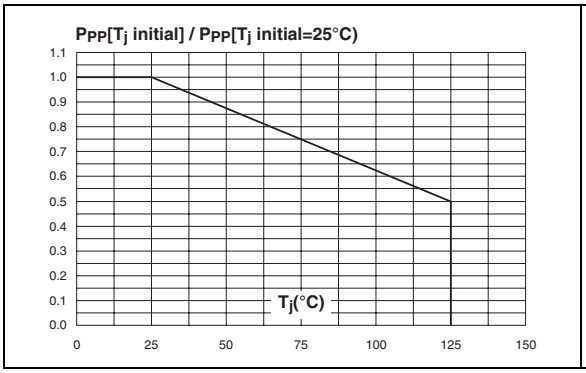


Figure 3. Peak pulse power versus exponential pulse duration

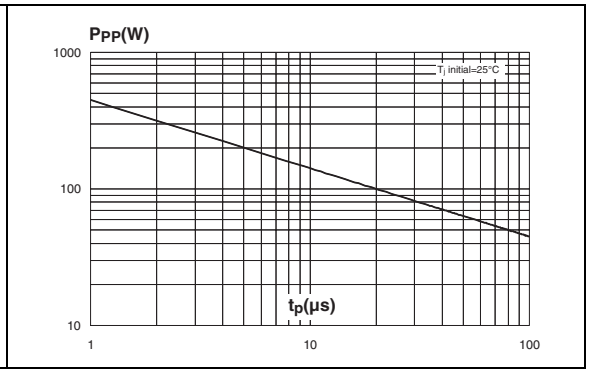


Figure 4. Clamping voltage versus peak pulse current (typical values)

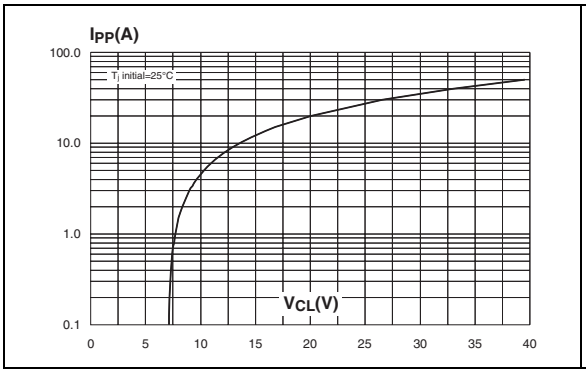


Figure 5. Junction capacitance versus reverse voltage applied (typical values)

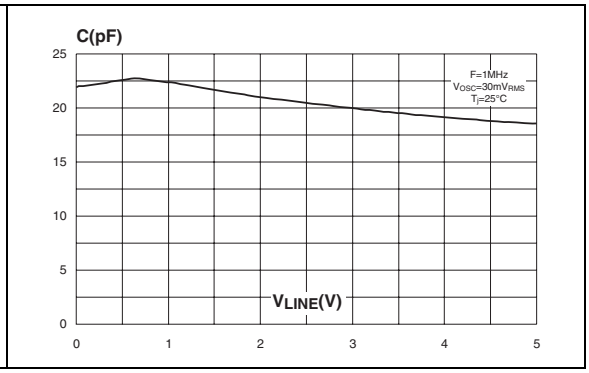


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

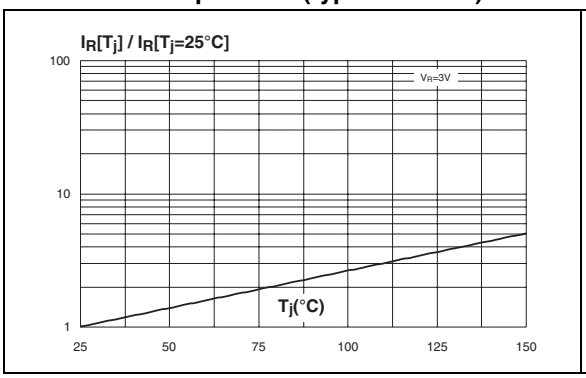


Figure 7. ESD response to IEC 61000-4-2 (+15 kV air discharge) on each channel

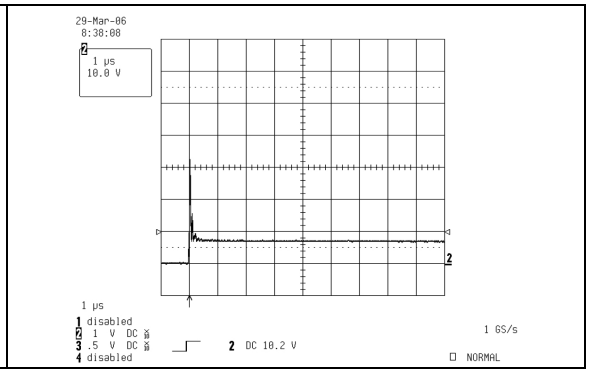


Figure 8. ESD response to IEC 61000-4-2 (-15 kV air discharge) on each channel

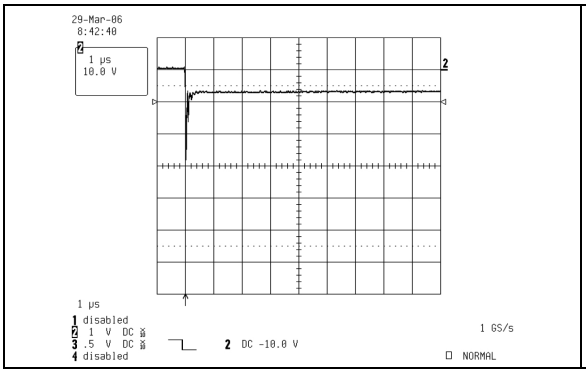
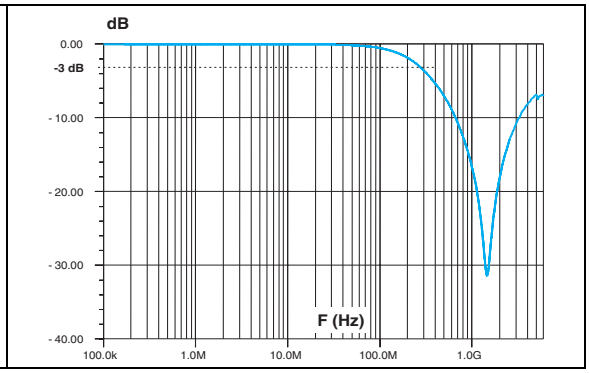
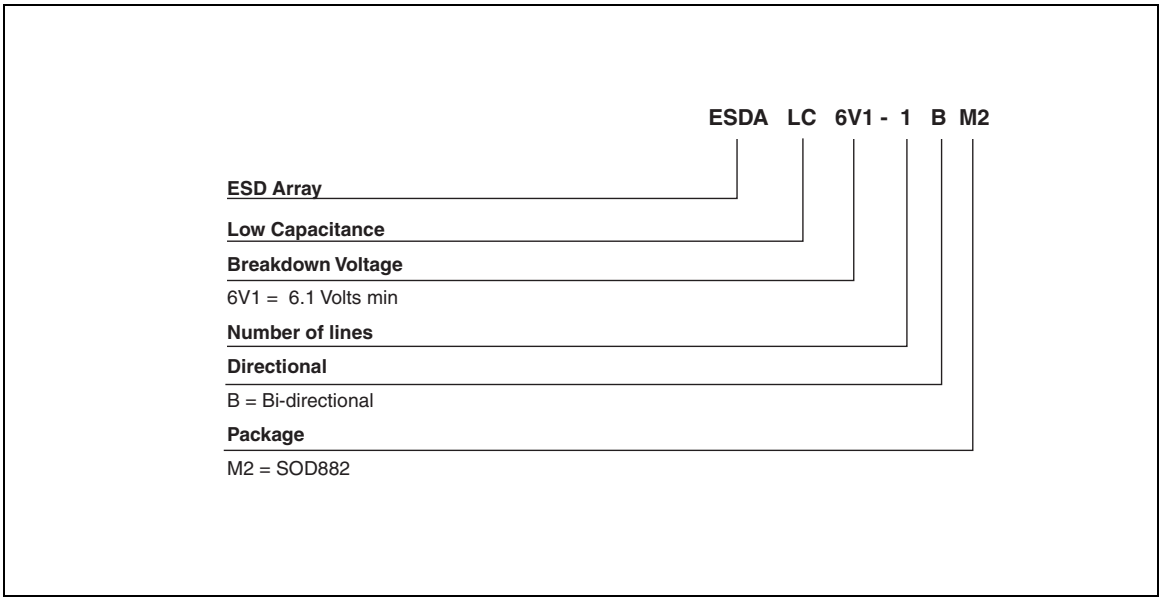


Figure 9. S21 attenuation measurement result



2 Ordering information scheme

Figure 10. Ordering information scheme

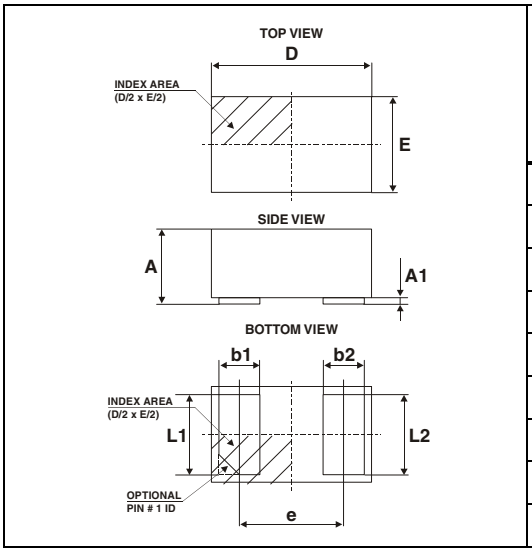


3 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 3. SOD882 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.20	0.25	0.30	0.008	0.010	0.012
b2	0.20	0.25	0.30	0.008	0.010	0.012
D		1.00			0.039	
E		0.60			0.024	
e		0.65			0.026	
L1	0.45	0.50	0.55	0.018	0.020	0.022
L2	0.45	0.50	0.55	0.018	0.020	0.022

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 11. Footprint (dimensions in mm)

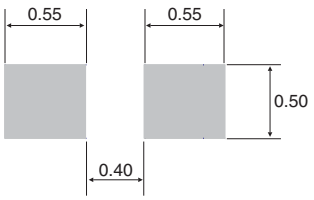
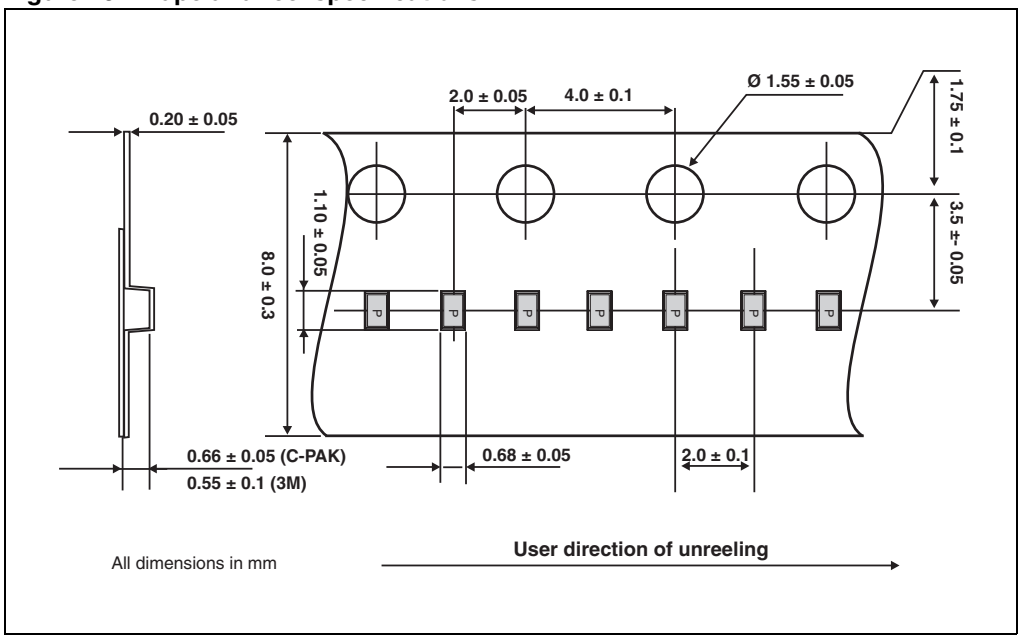


Figure 12. Marking

Figure 13. Tape and reel specifications

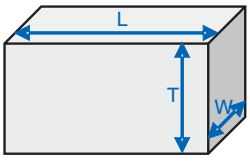


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 14. Stencil opening dimensions



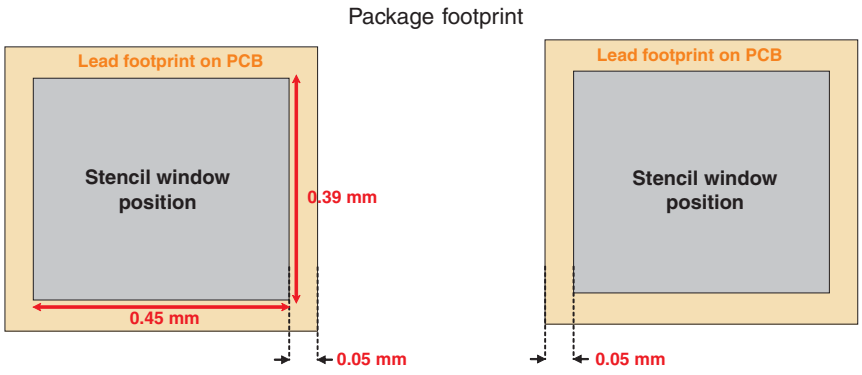
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 60% and 65%.

Figure 15. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

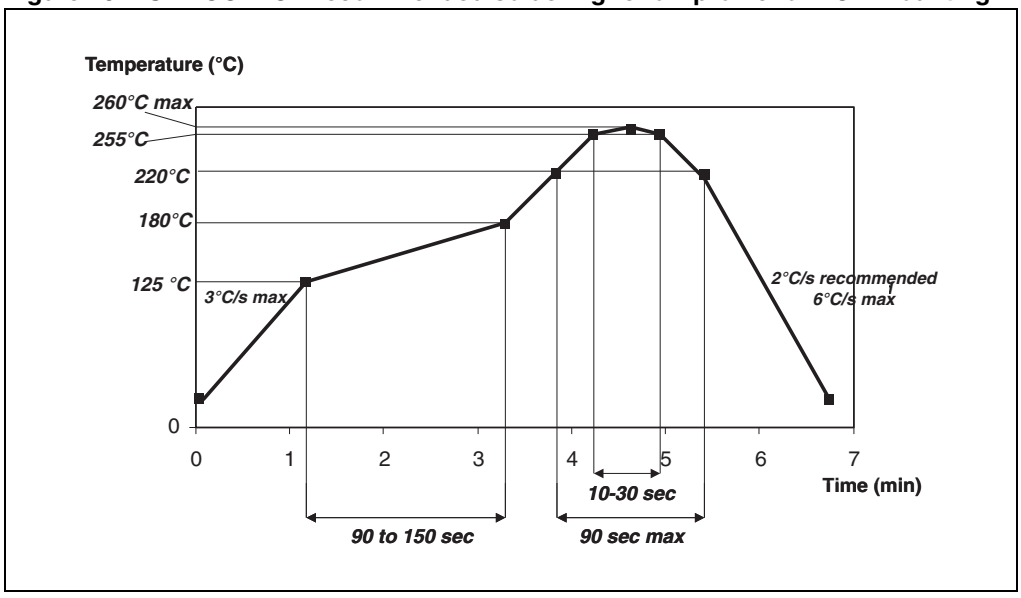
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 16. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1-1BM2	P(1)	SOD882	0.89 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
11-Jan-2007	1	Initial release.
1-Apr-2007	2	Reformatted to currrent standards. Added *Figure 12.: Marking*. Updated *Figure 13.: Tape and reel specifications*. Added *Section 4: Recommendation on PCB assembly*.

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