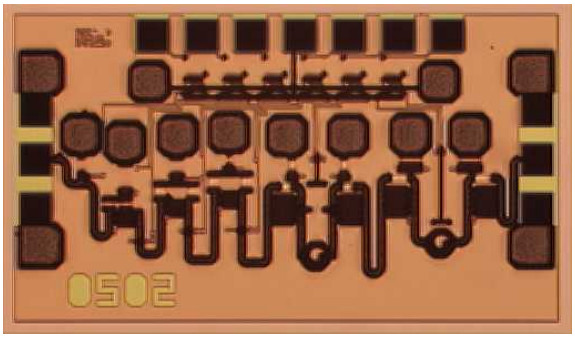
DC-6.0 GHz Attenuator

MAATGM0001-DIE
RO-P-DS-3043 B
Preliminary Information

Features

- 6 Bit Attenuator Range
- 35dB Coverage, LSB = 0.56dB
- TTL Control Inputs
- MSAG™ MESFET Process



Primary Applications

- Satellite Communication
- Phased Array Radar

Description

The MAATGM0001-Die is a 6-bit Attenuator with Parallel Input Control. This product is fully matched to 50 ohms on both the input and output.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Satellite Communication
- Phased Array Radar

Electrical Characteristics: T_B = 25°C[1], Z_0 = 50Ω, V_{EE} = -5V

Parameter	Symbol	Typical	Units
Bandwidth	f	DC-6.0	GHz
Insertion Loss	IL	3.5	dB
Input VSWR (At Reference)	VSWR	1.5:1	
Output VSWR (At Reference)	VSWR	1.3:1	
RMS Attenuation Error	RMS	0.5	dB
Attenuation Range	ΔG	35	dB
Phase Variation over all Attenuation States	ΔΦ	< 5	degree
Digital Supply Current	I_{EE}	< 10	mA
Input Third Order Intercept, >2 GHz	ITOI	36	dBm
Input 1-dB Compression Point, > 2GHz	P_{1dB}	26	dBm

1. T_B = MMIC Base Temperature

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• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Maximum Operating Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	31	dBm
Digital Supply Voltage	V_{EE}	-6	V
Digital Supply Current	I_{EE}	20	mA
Junction Temperature	T_j	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	V_{EE}	-5.2	-5	-4.8	V
Control Voltage					
Logic High / On		3	5	5	V
Logic Low / Off		0	0	0.8	V

Truth Table[2]

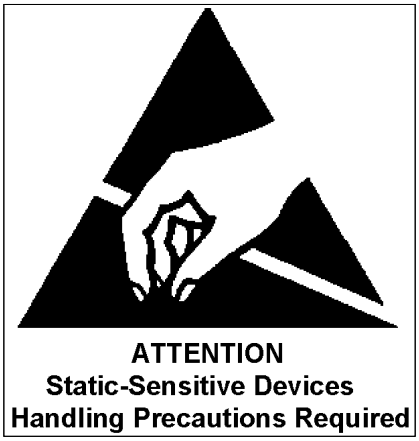
Designation	Description	Level	State
A6	18dB Attenuator Bit	Logic High	Attenuation ≈ 18dB
A5	9.0dB Attenuator Bit	Logic High	Attenuation ≈ 9.0dB
A4	4.5dB Attenuator Bit	Logic High	Attenuation ≈ 4.5dB
V_{EE}	DC Supply Voltage	-5V	ON
A3	2.25dB Attenuator Bit	Logic High	Attenuation ≈ 2.25dB
A2	1.12dB Attenuator Bit	Logic High	Attenuation ≈ 1.12dB
A1	0.56dB Attenuator Bit	Logic High	Attenuation ≈ 0.56dB

2. All Attenuator Bits at Logic Low = Reference State.

Operating Instructions

This device is static and light sensitive. The digital circuitry operation can be impaired under high intensity light, e.g. microscope light. Please handle with care. To operate the device, follow these steps.

1. Power Up: Apply V_{EE} = -5 V.
2. Apply TTL Levels to control pads as listed in Recommended Operating Conditions
3. Power Down: Set V_{EE} = 0



ATTENTION
Static-Sensitive Devices
Handling Precautions Required

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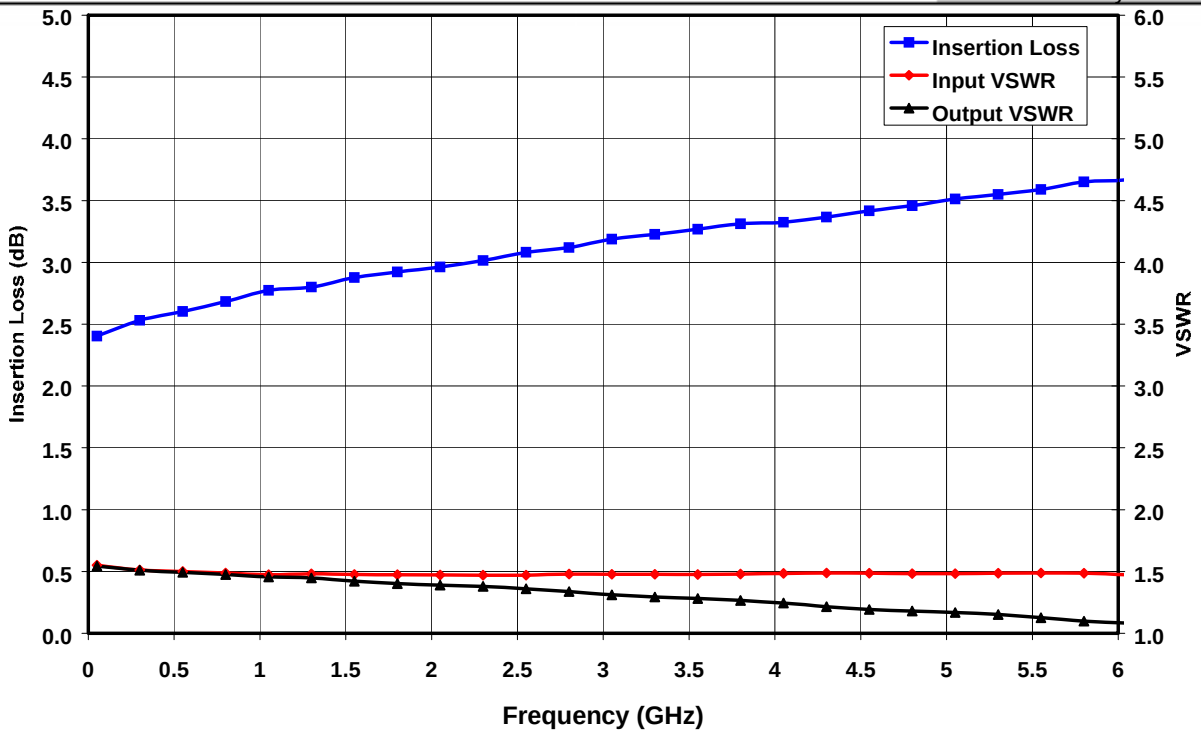

Figure 1. Insertion Loss and VSWR vs. Frequency.

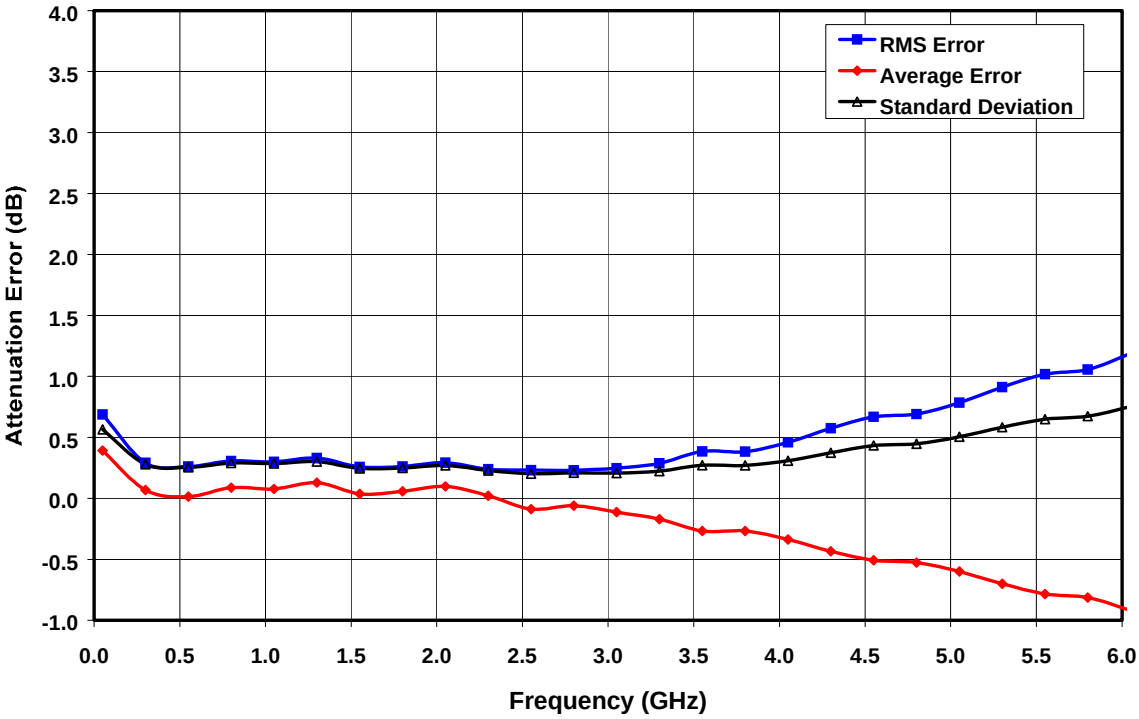

Figure 2. Attenuator Figures of Merit: RMS Error, Average Error, and Standard Deviation over All States .

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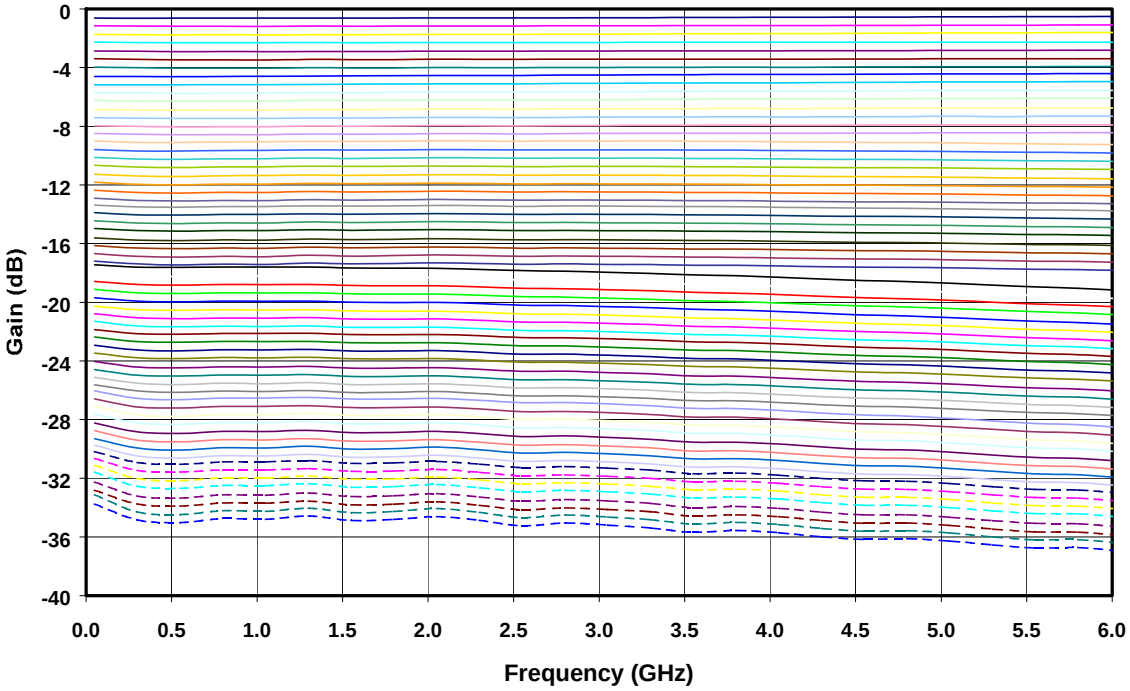

Figure 3. Gain Over All States.

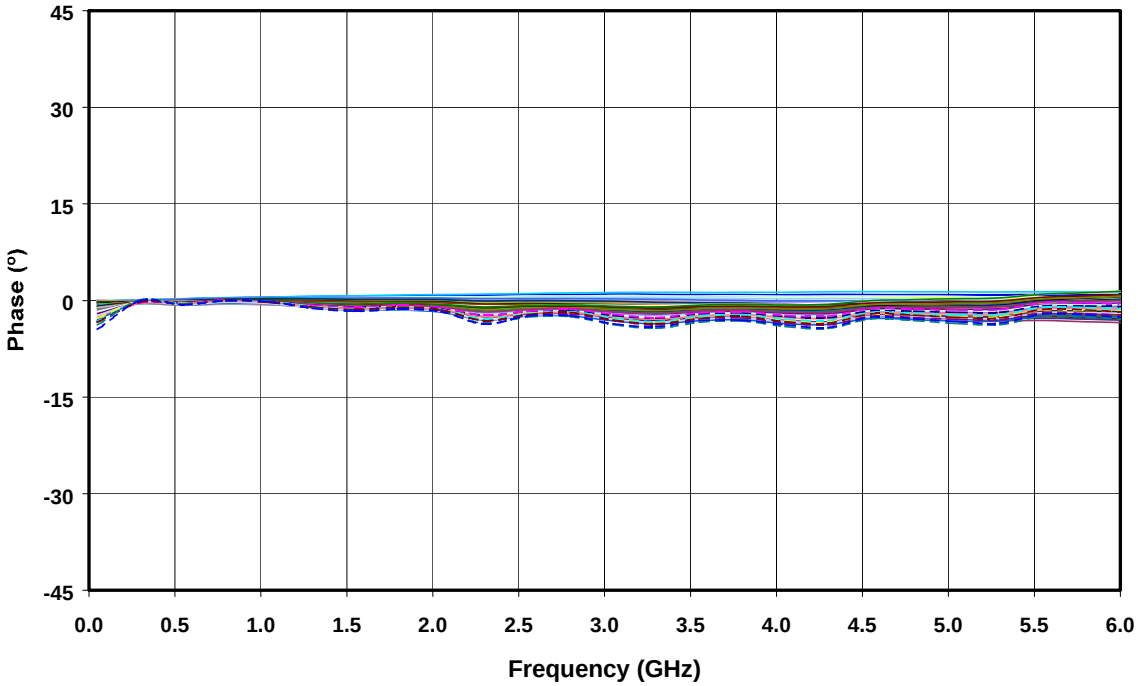

Figure 4. Phase Shift Over All Attenuator States.

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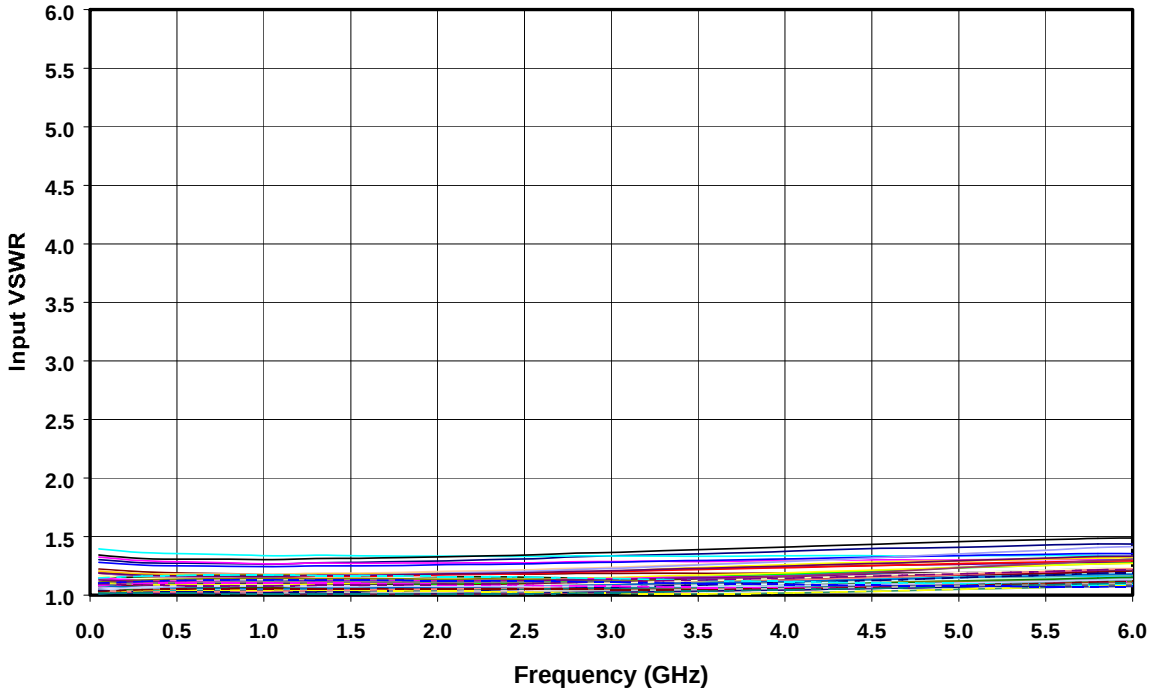

Figure 5. Input VSWR Over All Attenuation States.

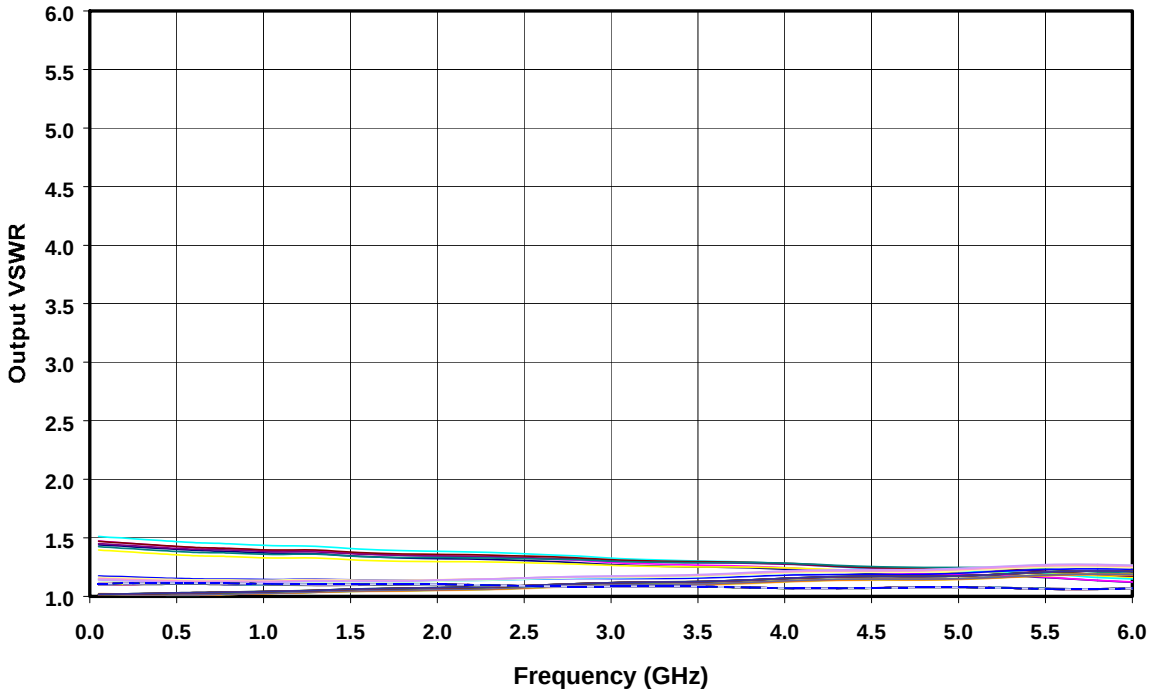

Figure 6. Output VSWR Over All Attenuation States.

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Mechanical Information

Chip Size: 2.32 x 1.354 x 0.075 mm (92 x 54 x 3 mils)

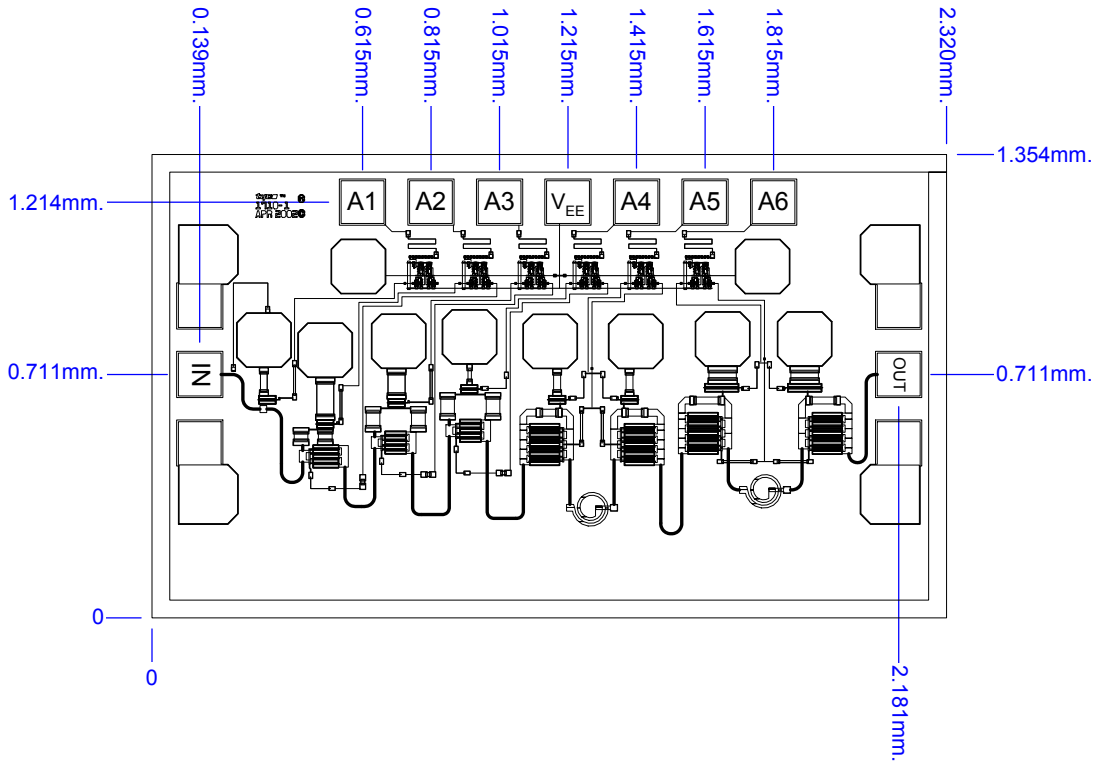

Figure 7. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF I/O: IN, OUT	100 x 200	4 x 8
Digital Supply Voltage: VEE	125 x 125	5 x 5
TTL Control Pads: A1, A2, A3, A4, A5, A6	125 x 125	5 x 5

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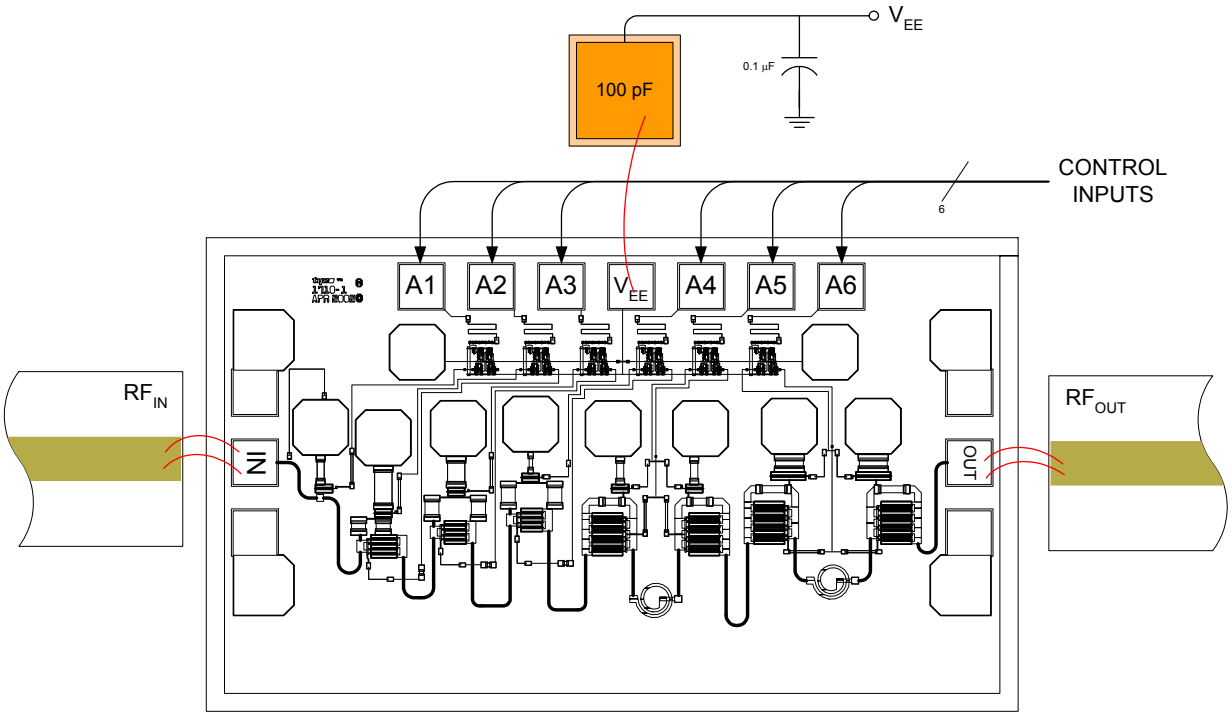

Figure 8. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW test-

Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

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