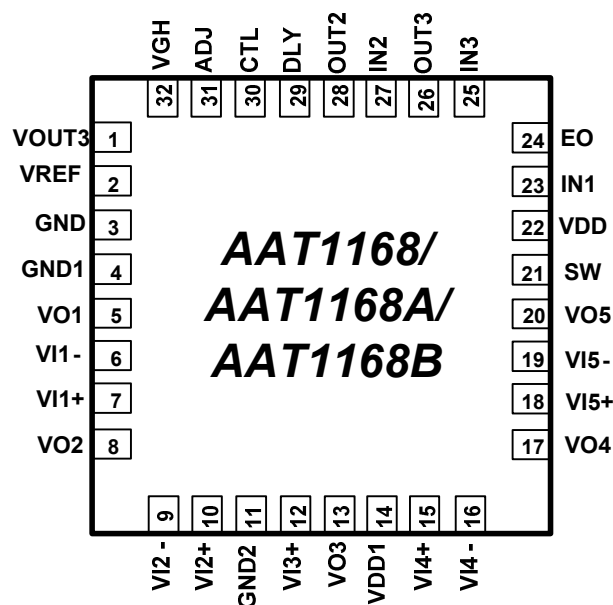


**AAT1168/1168A/1168B**

Product information presented is current as of publication date. Details are subject to change without notice.

**TRIPLE-CHANNEL TFT LCD POWER SOLUTION  
WITH OPERATIONAL AMPLIFIERS****FEATURES**

- Built in 3A, 0.2Ω Switching NMOS
- Positive LDO Driver Up to 28V/5mA
- Negative LDO Driver Down to -14V/5mA
- 1  $V_{COM}$  and 4  $V_{GAMMA}$  Operational Amplifiers
- 28V High Voltage Switch for VGH
- Internal Soft-Start Function
- 1.2MHz Fixed Switching Frequency
- 3 Channels Fault and Thermal Protection
- Low Dissipation Current
- QFN-32 Package Available

**PIN CONFIGURATION****GENERAL DESCRIPTION**

The AAT1168/AAT1168A/AAT1168B is a triple-channel TFT LCD power solution that provides a step-up PWM controller, two LDO drivers (one for positive high voltage and one for negative voltage), five operational amplifiers, and one high voltage switch up to 28V for TFT LCD display.

The PWM controller consists of an on-chip voltage reference, oscillator, error amplifier, current sense circuit, comparator, under-voltage lockout protection and internal soft-start circuit. The thermal and power fault protection prevents internal circuit being damaged by excessive power.

The LDO drivers generate two regulated output voltage set by external resistor dividers. VGH voltage does not activate until DLY voltage exceeds 1.25V.

The AAT1168/AAT1168A/AAT1168B contains 4+1 operational amplifiers. VO1, VO2, VO4, and VO5 are for gamma corrections and VO3 is for  $V_{COM}$ . In the short circuit condition, operational amplifiers are capable of sourcing  $\pm 100\text{mA}$  current for  $V_{GAMMA}$ , and  $\pm 200\text{mA}$  current for  $V_{COM}$ .

With the minimal external components, the AAT1168/A/B offers a simple and economical solution for TFT LCD power.



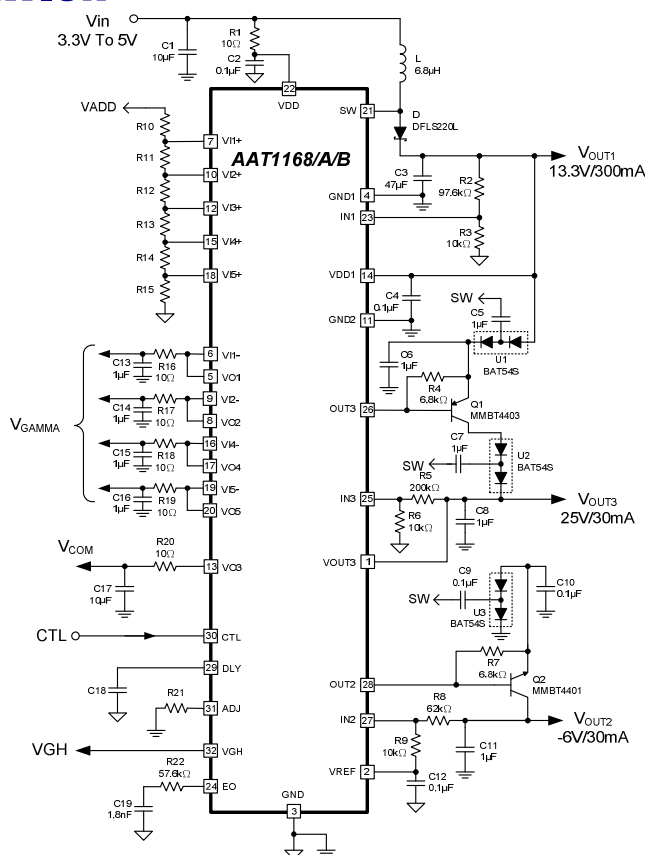
**AAT1168/1168A/1168B**

**ORDERING INFORMATION**

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT1168	AAT1168-Q5-T	Q5:VQFN32-5*5	T: Tape and Reel	-40 °C to +85 °C	AAT1168 XXXXX XXXX	Device Type Lot no.(6~9digits) Date Code (4digits)
AAT1168A	AAT1168A-Q5-T	Q5:VQFN32-5*5	T: Tape and Reel	-40 °C to +85 °C	AAT1168A XXXXX XXXX	Device Type Lot no.(6~9digits) Date Code (4Digits)
AAT1168B	AAT1168B-Q5-T	Q5:VQFN32-5*5	T: Tape and Reel	-40 °C to +85 °C	AAT1168B XXXXX XXXX	Device Type Lot no.(6~9digits) Date Code (4Digits)

NOTE: The product is lead free and halogen free.

**TYPICAL APPLICATION**



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**AAT1168/1168A/1168B****ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
VDD to GND	$V_{DD}$	7	V
VDD1, SW to GND (for AAT1168/AAT1168B)	$V_{H1}$	14.5	V
VDD1, SW to GND (for AAT1168A)	$V_{H1}$	25	V
VOU3, OUT3, VGH to GND (for AAT1168/AAT1168B)	$V_{H2}$	28	V
VOU3, OUT3, VGH to GND (for AAT1168A)	$V_{H2}$	40	V
OUT2 to GND	$V_{H3}$	-14	V
Input Voltage 1 (IN1, IN2, IN3, DLY, CTL)	$V_{I1}$	$V_{DD} + 0.3$	V
Input Voltage 2 (VI1+, VI1-, VI2+, VI2-, VI3+, VI3-, VI4+, VI4-, VI5+, VI5-)	$V_{I2}$	$V_{H1} + 0.3$	V
Output Voltage 1 (EO, $V_{REF}$ )	$V_{O1}$	$V_{DD} + 0.3$	V
Output Voltage 2 (ADJ, VO1, VO2, VO3, VO4, VO5)	$V_{O2}$	$V_{H1} + 0.3$	V
Operating Free-Air Temperature Range	$T_C$	-40 °C to +85 °C	°C
Storage Temperature Range	$T_{STORAGE}$	-45 °C to +125 °C	°C
Maximum Junction Temperature	$T_J$	+125	°C
Package Thermal Resistance	$J_A$	34	°C/W
Package Thermal Resistance	$J_C$	1.1	°C/W
Power Dissipation	$P_d$	1,618	mW

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

**AAT1168/1168A/1168B****ELECTRICAL CHARACTERISTICS**

( $V_{DD} = 2.6V$  to  $5.5V$ ,  $T_C = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified. Typical values are tested at  $25^\circ C$  ambient temperature,  $V_{DD} = 5V$ ,  $V_{DD1} = 10V$ .)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD Input Voltage Range	$V_{DD}$		2.6		5.5	V
VDD1 Input Voltage Range	$V_{DD1}$	AAT1168/AAT1168B	8		14	V
		AAT1168A	8		23	V
VDD Under Voltage Lockout	$V_{UVLO}$	Falling	2.1	2.2	2.3	V
		Rising	2.3	2.4	2.5	V
VDD Operating Current	$I_{VDD}$	$V_{IN1} = 1.5V$ , Not Switching		0.56	0.80	mA
		$V_{IN1} = 1.0V$ , Switching		5.60	10.0	mA
VDD1 Operating Current	$I_{VDD1}$	$V_{VI1+} \sim V_{VI5+} = 4V$		7	10	mA
Thermal Shutdown	$T_{SHDN}$			160		$^\circ C$

**Reference Voltage**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	$V_{REF}$	$I_{VREF} = 100\mu A$	1.231	1.250	1.269	V
Line Regulation	$V_{RI}$	$I_{VREF} = 100\mu A$ , $V_{DD} = 2.6V \sim 5.5V$	-	2	5	mV
Load Regulation	$V_{RO}$	$I_{VREF} = 0 \sim 100\mu A$	-	1	5	mV

**Oscillator**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	$f_{OSC}$		1.05	1.20	1.35	MHz
Maximum Duty Cycle	$D_{MAX}$		84	87	90	%

**AAT1168/1168A/1168B****ELECTRICAL CHARACTERISTICS**

( $V_{DD} = 2.6V$  to  $5.5V$ ,  $T_C = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified. Typical values are tested at  $25^\circ C$  ambient temperature,  $V_{DD} = 5V$ ,  $V_{DD1} = 10V$ .)

**Soft Start & Fault Detect**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Channel 1 Soft Start Time	$t_{SS1}$			14		ms
Channel 2 Soft Start Time	$t_{SS2}$			14		ms
Channel 3 Soft Start Time	$t_{SS3}$			14		ms
Channel 1 to Channel 2 Delay	$t_{D12}$	AAT1168A Only		7		ms
Channel 2 to Channel 3 Delay	$t_{D23}$	AAT1168A Only		7		ms
During Fault Protect Trigger Time	$t_{FP}$	AAT1168/AAT1168B		55		ms
		AAT1168A		165		ms
IN1 Fault Protection Voltage	$V_{F1}$	AAT1168/AAT1168B	1.00	1.05	1.10	V
		AAT1168A	1.13	1.17	1.20	V
IN2 Fault Protection Voltage	$V_{F2}$		0.40	0.45	0.50	V
IN3 Fault Protection Voltage	$V_{F3}$		1.00	1.05	1.10	V

**Error Amplifier (Channel 1)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Feedback Voltage	$V_{IN1}$		1.221	1.233	1.245	V
Input Bias Current	$I_{B1}$	$V_{IN1} = 1V$ to $1.5V$	-40	0	40	nA
Feedback-Voltage Line Regulation	$V_{RI1}$	Level to Produce $V_{EO} = 1.233V$ $2.6V < V_{DD} < 5.5V$		0.05	0.15	%/V
Transconductance	$G_m$	$\Delta I = 5\mu A$		105		$\mu S$
Voltage Gain	$A_V$			1,500		V/V

**AAT1168/1168A/1168B****ELECTRICAL CHARACTERISTICS**

( $V_{DD} = 2.6V$  to  $5.5V$ ,  $T_C = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified. Typical values are tested at  $25^\circ C$  ambient temperature,  $V_{DD} = 5V$ ,  $V_{DD1} = 10V$ .)

**N-MOS Switch (Channel 1)**

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Limit	$I_{LIM}$			3.0		A
On-Resistance	$R_{ON}$	$I_{SW} = 1.0A$		0.2		$\Omega$
Leakage Current	$I_{SWOFF}$	$V_{SW} = 12V$		0.01	20.00	$\mu A$

**Negative Charge Pump (Channel 2)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN2 Threshold Voltage	$V_{IN2}$	$I_{OUT2} = -100\mu A$	235	250	265	mV
IN2 Input Bias Current	$I_{B2}$	$V_{IN2} = -0.25V$ to $0.25V$	-40	0	40	nA
OUT2 Leakage Current	$I_{OFF2}$	$V_{IN2} = 0V$ , $OUT2 = -12V$		-20	-50	$\mu A$
OUT2 Source Current	$I_{OUT2}$	$V_{IN2} = 0.35V$ , $OUT2 = -10V$	1	4		mA

**Positive Charge Pump (Channel 3)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN3 Threshold Voltage	$V_{IN3}$	$I_{OUT3} = 100\mu A$	1.22	1.25	1.28	V
IN3 Input Bias Current	$I_{B3}$	$V_{IN3} = 1V$ to $1.5V$	-40	0	40	nA
OUT3 Leakage Current	$I_{OFF3}$	$V_{IN3} = 1.4V$ , $OUT3 = 28V$		40	80	$\mu A$
OUT3 Sink Current	$I_{OUT3}$	$V_{IN3} = 1.1V$ , $OUT3 = 25V$	1	4		mA

**AAT1168/1168A/1168B****ELECTRICAL CHARACTERISTICS**

( $V_{DD} = 2.6V$  to  $5.5V$ ,  $T_C = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified. Typical values are tested at  $25^\circ C$  ambient temperature,  $V_{DD} = 5V$ ,  $V_{DD1} = 10V$ .)

**High Voltage Switch Controller**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DLY Source Current	$I_{DLY}$		-4	-5	-6	$\mu A$
DLY Threshold Voltage	$V_{DLY}$		1.22	1.25	1.28	V
DLY Discharge $R_{ON}$	$R_{DLY}$			8		$\Omega$
CTL Input Low Voltage	$V_{IL}$				0.5	V
CTL Input High Voltage	$V_{IH}$		2			V
CTL Input Bias Current	$I_{B4}$	$V_{CTL} = 0$ to $V_{DD}$	-40	0	40	nA
Propagation Delay CTL to VGH	$t_{PP}$	OUT3 = 25V		100		ns
VOUT3 to VGH Switch R-on	$R_{ONSC}$	$V_{DLY} = 1.5V$ , $V_{CTL} = V_{DD}$		15	30	$\Omega$
ADJ to VGH Switch R-on	$R_{ONDC}$	$V_{DLY} = 1.5V$ , $V_{CTL} = GND$		30	60	$\Omega$



**AAT1168/1168A/1168B**

**ELECTRICAL CHARACTERISTICS**

( $V_{DD} = 2.6V$  to  $5.5V$ ,  $T_C = -40^\circ C$  to  $85^\circ C$ , unless otherwise specified. Typical values are tested at  $25^\circ C$  ambient temperature,  $V_{DD} = 5V$ ,  $V_{DD1} = 10V$ .)

**$V_{COM}$  and  $V_{GAMMA}$  Buffer**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$V_{OS}$	$V_{V1+} \sim V_{V15+} = 4V$	-	2	12	mV
Input Bias Current	$I_{B5}$	$V_{V1+} \sim V_{V15+} = 4V$	-40	0	40	nA
Output Swing (for AAT1168)	$V_{OL}$	$I_{VO1}, I_{VO2}, I_{VO4}, I_{VO5} = 10mA,$ $V_{V11}, V_{V12}, V_{V14}, V_{V15} = 4V$	-	4.02	4.05	V
		$I_{VO3} = 50mA, V_{V13} = 4V$	-	4.03	4.06	
	$V_{OH}$	$I_{VO1}, I_{VO2}, I_{VO4}, I_{VO5} = -10mA$ $V_{V11}, V_{V12}, V_{V14}, V_{V15} = 4V$	3.95	3.98	-	
		$I_{VO3} = -50mA, V_{V13} = 4V$	3.94	3.97	-	
Short Circuit Current	$I_{SHORT}$	$I_{VO1}, I_{VO2}, I_{VO4}, I_{VO5}$	-	$\pm 100$	-	mA
		$I_{VO3}$	-	$\pm 200$	-	mA
Slew Rate	SR	$V_{V1+}, V_{V13+} = 2V$ to $8V,$ $V_{V13+} \sim V_{V15+} = 8V$ to $2V,$ $20\%$ to $80\%$	-	12	-	V/ $\mu s$
Settling Time	$t_s$	$V_{V1+} \sim V_{V15+} = 3.5V$ to $4.5V, 90\%$	-	5	-	$\mu s$



**AAT1168/1168A/1168B****PIN DESCRIPTION**

<b>PIN NO. QFN-32</b>	<b>NAME</b>	<b>I/O</b>	<b>DESCRIPTION</b>
1	VOUT3	-	Channel 3 Output Voltage (gate high voltage input)
2	VREF	O	Internal Reference Voltage Output
3	GND	-	Ground
4	GND1	-	SW MOS Ground
5	VO1	O	Operational Amplifier 1 Output
6	VI1-	I	Operational Amplifier 1 Negative Input
7	VI1+	I	Operational Amplifier 1 Positive Input
8	VO2	O	Operational Amplifier 2 Output
9	VI2-	I	Operational Amplifier 2 Negative Input
10	VI2+	I	Operational Amplifier 2 Positive Input
11	GND2	-	Ground for Operational Amplifiers
12	VI3+	I	V <sub>COM</sub> Operational Amplifier Positive Input
13	VO3	I	V <sub>COM</sub> Operational Amplifier Output
14	VDD1	-	High Voltage Power Supply Input
15	VI4+	I	Operational Amplifier 4 Positive Input
16	VI4-	I	Operational Amplifier 4 Negative Input
17	VO4	O	Operational Amplifier 4 Output
18	VI5+	I	Operational Amplifier 5 Positive Input
19	VI5-	I	Operational Amplifier 5 Negative Input
20	VO5	O	Operational Amplifier 5 Output
21	SW	-	Main PWM Switching Pin
22	VDD	-	Power Supply Input
23	IN1	I	Main PWM Feedback Pin
24	EO	O	Main PWM Error Amplifier Output
25	IN3	I	Positive Charge Pump Feedback Pin
26	OUT3	O	Positive Charge Pump Output
27	IN2	I	Negative Charge Pump Feedback Pin

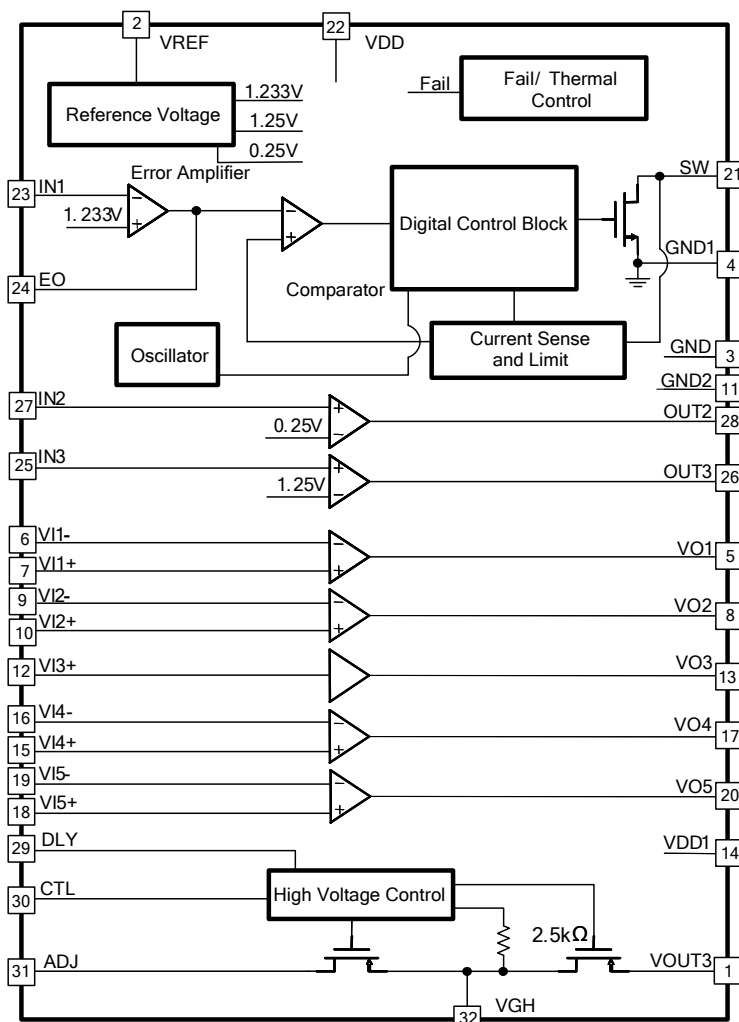


**AAT1168/1168A/1168B**

PIN NO. QFN-32	NAME	I/O	DESCRIPTION
28	OUT2	O	Negative Charge Pump Output
29	DLY	I	High Voltage Switch Delay Control
30	CTL	I	High Voltage Switch Control Pin
31	ADJ	O	Gate High Voltage Fall Time Setting Pin
32	VGH	O	Switching Gate High Voltage for TFT

## FUNCTION BLOCK DIAGRAM

### AAT1168



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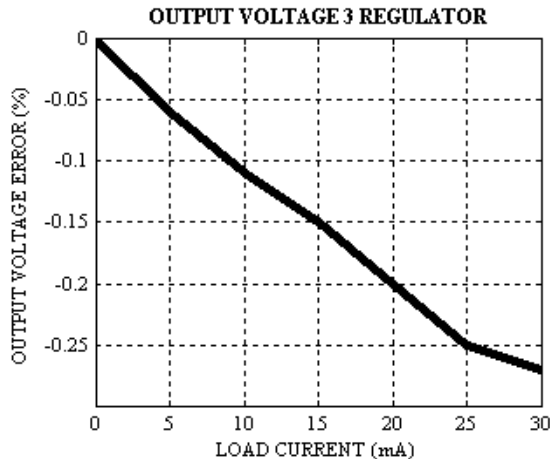
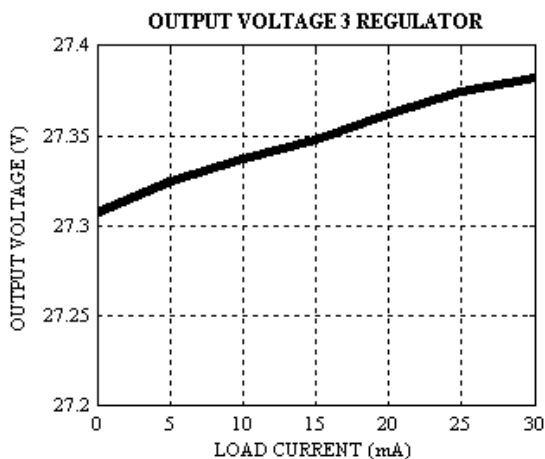
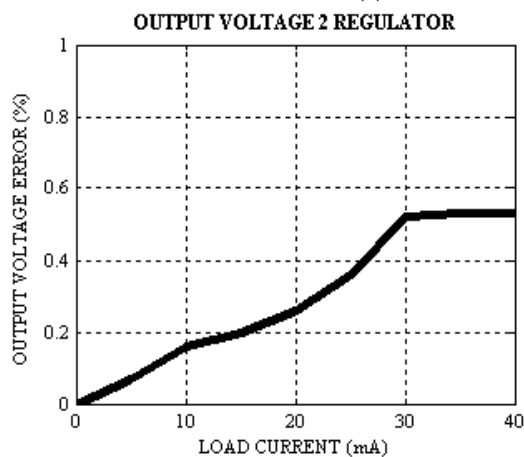
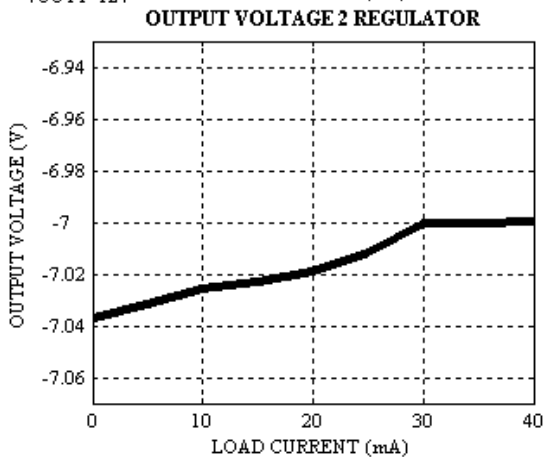
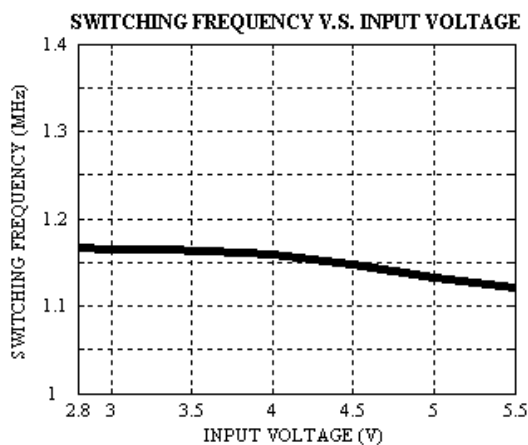
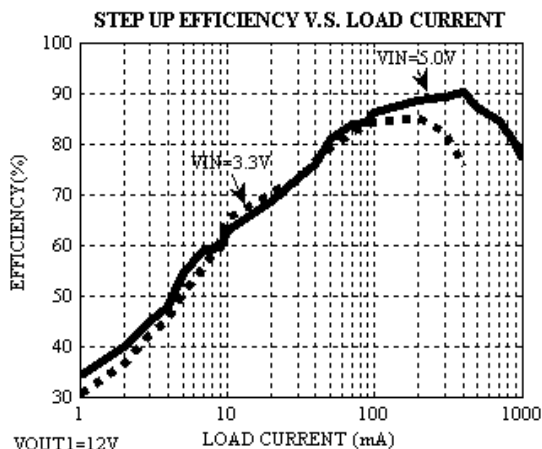




AAT1168/1168A/1168B

# TYPICAL OPERATING CHARACTERISTICS

( $V_{IN} = 5V$ ,  $V_{OUT1} = 12V$ ,  $V_{OUT2} = -7V$ ,  $V_{OUT3} = 27V$ ,  $T_C = +25^\circ C$ , unless otherwise noted.)



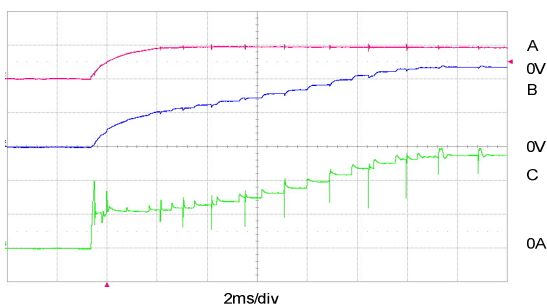


AAT1168/1168A/1168B

TYPICAL OPERATING CHARACTERISTICS

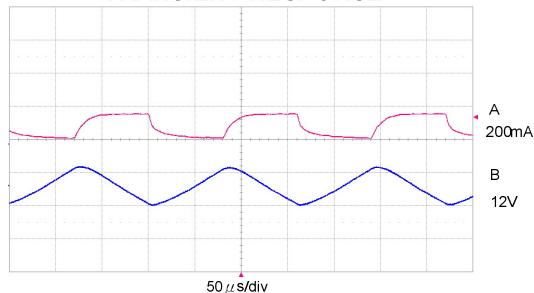
(VIN = 5V, VOUT1 = 12V, VOUT2 = -7V, VOUT3 = 27V, TC = +25°C, unless otherwise noted.)

STEP UP REGULATOR SOFT-START (HEAVY LOAD)



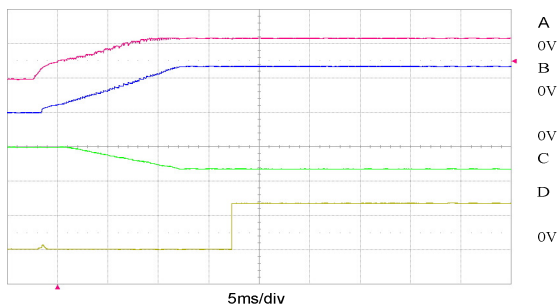
A:VIN,5V/div
B:VOUT1,5V/div
C:INDUCTOR CURRENT,1A/div

STEP UP REGULATOR PULSED LOAD TRANSIENT RESPONSE



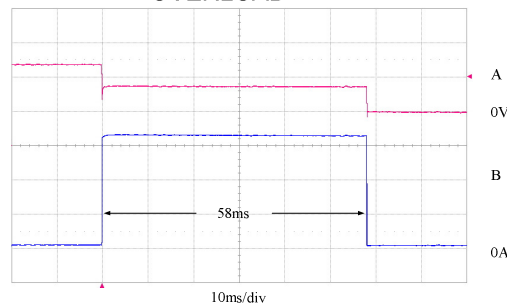
A:LOAD CURRENT,100mA/div
B:VOUT1,200mV/div,AC-COUPLED

POWER ON SEQUENCE



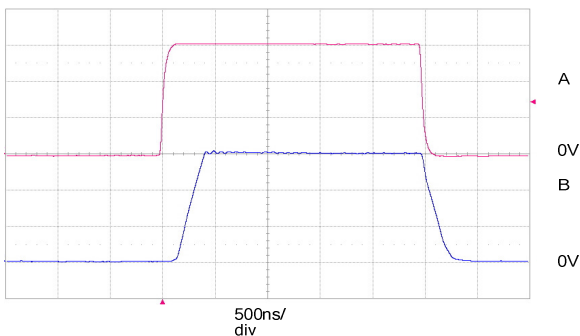
A:VOUT1,10V/div
B:VOUT3,20V/div
C:VOUT2,10V/div
D:VOUT3,20V/div

TIME DELAY LATCH RESPONSE TO OVERLOAD



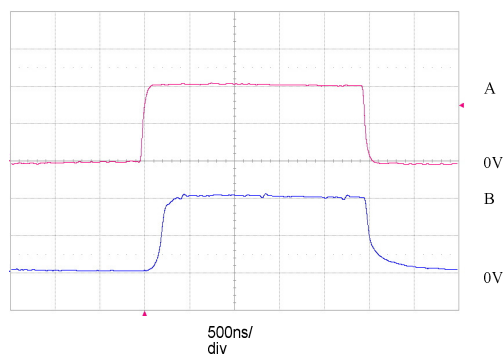
A:VOUT1,5V/div
B:INDUCTOR CURRENT,1A/div

OPERATIONAL-AMPLIFIER LARGE SIGNAL STEP RESPONSE



A:INPUT SIGNAL,2V/div
B:OUTPUT SIGNAL,2V/div
VSUP=6V

OPERATIONAL-AMPLIFIER SMALL SIGNAL STEP RESPONSE



A:INPUT SIGNAL,200mV/div
B:OUTPUT SIGNAL,200mV/div



**AAT1168/1168A/1168B**

**DESIGN PROCEDURE**

**Boost Converter Design**

**Setting the Output Voltage and Selecting the Lead Compensation Capacitor**

The output voltage of boost converter is set by the resistor divider from the output ( $V_{OUT1}$ ) to GND with the center tap connected to the IN1. Where  $V_{IN1}$ , the boost converter feedback regulation voltage is 1.233V. Choose  $R_2$  (Figure 2) between 5.1k $\Omega$  to 51k $\Omega$  and calculate  $R_1$  to satisfy the following equation.

$$R_1 = R_2 \left( \frac{V_{OUT1}}{V_{IN1}} - 1 \right)$$

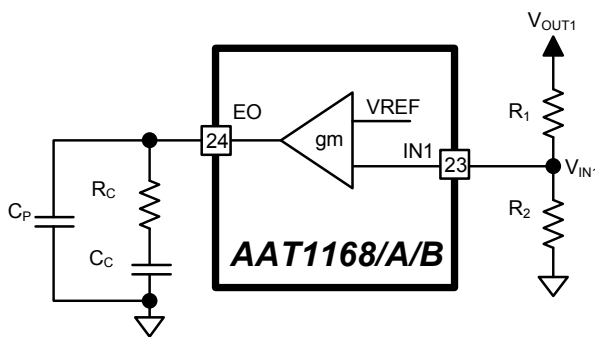


Figure 2. Feedback Circuit

**Inductor Selection**

The minimum inductance value is selected to make sure that the system operates in continuous conduction mode (CCM) for high efficiency and to prevent EMI. The equation of inductor used a parameter  $\kappa$ , which is the ratio of the inductor peak to peak ripple current to the input DC current. The best trade-off between voltage ripple of transient output current and permanent output current has a  $\kappa$  between 0.4 and 0.5.

$$L \geq \frac{\eta V_O D(1-D)^2}{\kappa I_O f_s}$$

$$D = 1 - \frac{V_{IN}}{V_O}$$

$$\kappa = \frac{I_{Lpeak}}{I_{IN}}$$

$\eta$ : Boost converter efficiency

$\kappa$ : The ratio of the inductor peak to peak ripple current to the input DC current

$V_{IN}$ : Input voltage

$V_O$ : Output voltage

$I_O$ : Output load current

$f_s$ : Switching frequency

$D$ : Duty cycle

$I_{LPEAK}$ : Inductor peak to peak ripple current

$I_{IN}$ : Input DC current

The AAT1168 SW current limit ( $I_{LIM}$ ) and inductor saturation current rating ( $I_{LSAT}$ ) should exceed  $I_{L(peak)}$ , and the inductor's DC current rating should exceed  $I_{IN}$ . For the best efficiency, choose an inductor with less DC series resistance ( $r_L$ ).

$$I_{LIM} \text{ and } I_{LSAT} > I_{L(peak)}$$

$$I_{LDC} > I_{IN}$$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} D}{2L f_s}$$

$$I_{IN} = \frac{I_O}{\eta(1-D)}$$

$$P_{DCR} \approx \left( \frac{I_O}{\eta(1-D)} \right)^2 r_L$$

$I_{LDC}$ : DC current rating of inductor

$P_{DCR}$ : Power loss of inductor series resistance

Table 1. Inductor Data List

C6-K1.8L	$r_L$	DC CURRENT RATING
3.9 $\mu$ H	41 m $\Omega$	2.5A
6.8 $\mu$ H	68 m $\Omega$	2.2A
10 $\mu$ H	81 m $\Omega$	1.8A
MITSUMI Product-Max Height: 1.9mm		

Example 1: In the typical application circuit (Figure 1) the output load current is 300mA with 13.3V output



**AAT1168/1168A/1168B**

voltage and input voltage of 5V. Choose a  $\kappa$  of 0.465 and efficiency of 90%.

$$L \geq \frac{0.9 * 13.3}{0.465 * 0.3 * 1.1^6} 0.624(0.376)^2 \approx 6.8 \mu\text{H}$$

$$I_{IN} = \frac{I_O}{\eta(1-D)} = 0.89\text{A}$$

$$I_{L(\text{peak})} = I_{IN} + \frac{V_{IND}}{2Lf_s} = 1.095\text{A}$$

$$P_{DCR} = 0.043\text{W or } 1\% \text{ power loss}$$

**Schottky Diode Selection**

Schottky has to be able to dissipate power. The dissipated power is the forward voltage and input DC current. To achieve the best efficiency, choose a Schottky diode with less recovery capacitor (CT) for fast recovery time and low forward voltage (VF).

For boost converter, the reverse voltage rating ( $V_R$ ) should be higher than the maximum output voltage, and current rating should exceed the input DC current.

$$P_{DIODE} = P_{DSW} + P_{DCOM}$$

$$P_{DSW} = (1-D)V_F Q_R f_s$$

$$Q_R = V_R C_T$$

$$P_{DCOM} = V_F I_O / (1-D)$$

$P_{DIODE}$  : Total power loss of diode for boost converter

$P_{DSW}$  : Switching loss of diode for boost converter

$P_{DCOM}$  : Conduction loss of diode for boost converter

**Table 2. Schottky Data List**

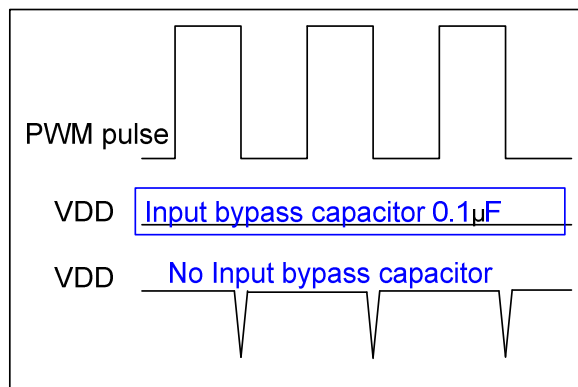
SMA	$V_F$	$V_R$	$C_T$
B220A	0.24V	14V	150pF
B240A	0.24V	28V	150pF
DIODES Product, Max-Height: 2.3mm			

For example,

$$P_{DIODE} = P_{DSW} + P_{DCOM} = 0.203\text{W or } 5.1\% \text{ power loss.}$$

**Input Capacitor Selection**

The input capacitors have two important functions in PWM controller. First, an input capacitor provides the power for soft start procedure and supply the current for the gate-driving circuit. A 10 $\mu$ F ceramic capacitor is used in typical circuit. Second, an input bypass capacitor reduces the current peaks, the input voltage drop, and noise injection into the IC. A low ESR ceramics capacitor 0.1 $\mu$ F is used in typical circuit. To ensure the low noise supply at  $V_{DD}$ ,  $V_{DD}$  is decoupled from input capacitor using an RC low pass filter.



**Figure 3. Input Bypass Capacitor Affects the  $V_{DD}$  Drop**

**Output Capacitor**

The output capacitor maintains the DC output voltage. A Low ESR ( $r_C$ ) ceramic capacitor can reduce the output ripple and power loss. There are two parameters which can affect the output voltage ripple: 1. the voltage drops when the inductor current flows through the ESR of output capacitor; 2. charging and discharging of the output capacitor also affect the output voltage ripple.

$$V_{RIPPLE} = V_{RIPPLE}(C_{OUT}) + V_{RIPPLE}(ESR)$$

$$V_{RIPPLE}(C_{OUT}) \approx \frac{I_O D}{f_s C_{OUT}}$$

$$V_{RIPPLE}(ESR) \approx I_{L(\text{peak})} r_C$$



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$$P_{ESR} = (I_{Lpeak})^2 \cdot r_C$$

ESR: Equivalent Series Resistance

Example 2:  $C_{OUT} = 38\mu F$ ,  $r_C = 20m\Omega$

$$V_{RIPPLE}(C_{OUT}) = 4mV$$

$$V_{RIPPLE}(ESR) = 22mV$$

$$V_{RIPPLE} = 26mV$$

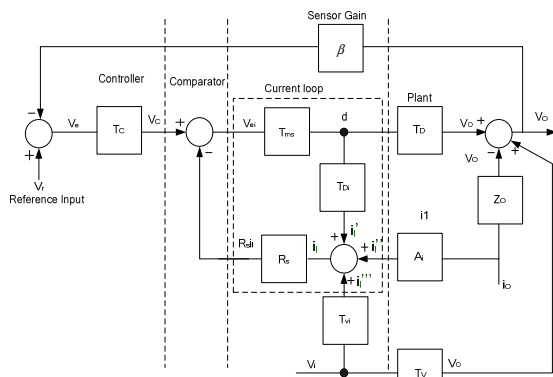
$$P_{ESR} = 0.023W \text{ or } 0.6\% \text{ power loss}$$

**Boost Converter Power loss**

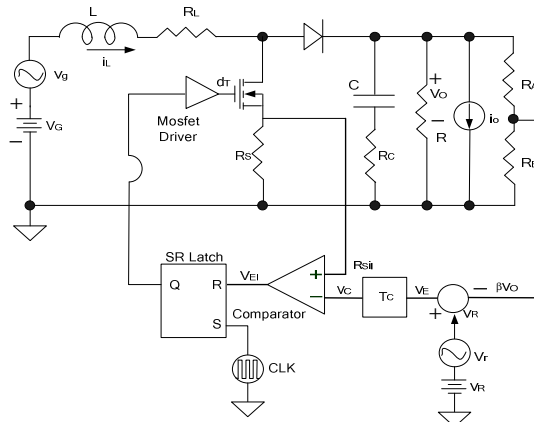
The largest portions of power loss in the boost converter are the internal power MOSFET, the inductor, the Schottky diode, and the output capacitor. If the boost converter has 90% efficiency, there is approximately 3.3% power loss in the internal MOSFET, 1% power loss in the inductor, 5.1% power loss in the Schottky diode, and 0.6% power loss in the output capacitor.

**Loop Compensation Design**

The voltage-loop gain with current loop closed sets the stability of steady state response and dynamic performance of transient response. The loop compensation design is as follows:



**Figure 4. Closed-current Loop for Boost with PCM**



**Figure 5. Block Diagram of Boost Converter with Peak Current Mode (PCM)**

**Power Stage Transfer Functions**

The duty to output voltage transfer function  $T_p$  is:

$$T_p(s) = \frac{V_O}{d} = T_{p0} \frac{(s + w_{esr})(s - w_{z2})}{s^2 + 2\xi w_n s + w_n^2}$$

Where  $T_{p0} = V_O \frac{-r_C}{(1-D)(R_L + r_C)}$ ,  $w_{esr} = \frac{1}{Cr_C}$

And

$$w_{z2} = \frac{R_L(1-D)^2 - r}{L}, w_n = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_C)}}$$

$$\xi = \frac{C[r(R_L + r_C) + R_L r_C(1-D)^2] + L}{2\sqrt{LC(R_L + r_C)[r + (1-D)^2 R_L]}}$$

$$r = r_L + Dr_{DS} + (1-D)R_F$$

$r_L$  is the inductor equivalent series resistance,  $r_C$  is capacitor ESR,  $R_L$  is the converter load resistance,  $C$  is output filter capacitor,  $r_{DS}$  is the transistor turn on resistance, and  $R_F$  is the diode forward resistance.

The duty to inductor current transfer function  $T_{pi}$  is:

$$T_{pi}(s) = \frac{i_L}{d} = T_{pi0} \frac{s + w_{zi}}{s^2 + 2\xi w_n s + w_n^2}$$

Where  $T_{pi0} = \frac{V_O(R_L + 2r_C)}{L(R_L + r_C)}$ ,  $w_{zi} = \frac{1}{C(R_L / 2 + r_C)}$





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**Current Sampling Transfer Function**

Error voltage to duty transfer function  $F_m$  is:

$$F_m(s) = \frac{d}{v_{ei}} = \frac{2f_s^2 (s^2 + 2\xi\omega_n s + \omega_n^2)}{T_{pi0} R_{CS} s (s + w_{zi}) (s + w_{sh})}$$

Where  $w_{sh} = \frac{3w_s}{\pi} \left( \frac{1-\alpha}{1+\alpha} \right)$ ,  $\alpha = \frac{M_2 - M_a}{M_1 + M_a}$

$w_s = 2\pi f_s$

Therefore,  $F_m$  depends on duty to inductor current transfer function  $T_{pi}$ , and  $f_s$  is the clock switching frequency;  $R_{CS}$  is the current-sense amplifier transresistance.

For the boost converter,  $M_1 = V_{IN}/L$  and  $M_2 = (V_O - V_{IN})/L$ .

For AAT1168,  $R_{CS} = 0.24 \text{ V/A}$ ,  $M_a$  is slope compensation,  $M_a = 0.8 \times 10^6$ .

The closed-current loop transfer function  $T_{icl}$  is:

$$T_{icl}(s) = \frac{12f_s^2}{R_{CS} T_{pi0}} \times \frac{(s^2 + 2\xi\omega_n s + \omega_n^2)}{(s + w_{zi})(s^2 + w_{sh}s + 12f_s^2)}$$

**The Voltage-Loop Gain with Current Loop Closed**

The control to output voltage transfer function  $T_d$  is:

$$T_d(s) = \frac{V_O(s)}{V_C(s)} = T_{icl}(s) T_p(s)$$

The voltage-loop gain with current loop closed is:

$$L_{vi}(s) = \beta T_C(s) T_d(s) \\ = \beta g_m R_C \frac{s + w_c}{s} \frac{12f_s^2 T_{pi0}}{R_{CS} T_{pi0}} \times \frac{(s + w_{zi})(s - w_{z2})}{(s + w_{zi})(s^2 + sw_{sh} + 12f_s^2)}$$

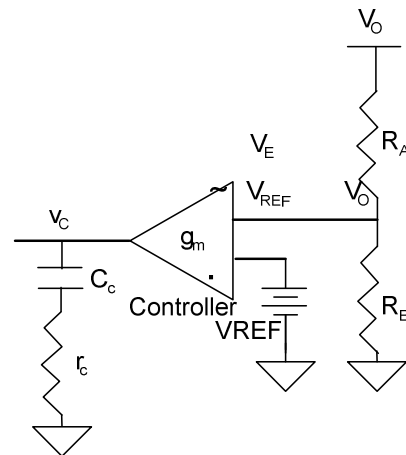
Where  $\beta = \frac{V_{FB}}{V_O}$

The compensator transfer function

$$T_C(s) = \frac{V_C}{v_{fb}} = g_m R_C \frac{s + w_c}{s}$$

Where

$$w_c = \frac{1}{R_C C_C}$$



**Figure 6. Voltage Loop Compensator**

Compensator design guide:

1. Crossover frequency  $f_{ci} < \frac{1}{2} f_s$
2. Gain margin > 10dB
3. Phase margin > 45°
4. The  $|L_{vi}(s)| = 1$  at crossover frequency, Therefore, the compensator resistance,  $R_C$  is determined by:

$$R_C = \frac{V_O}{V_{FB}} \frac{2\pi f_{ci} C_C R_{CS}}{g_m k} \left[ \frac{(R_L + 2r_c)}{(1-D)R_L - \frac{r}{(1-D)}} \right]$$



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**Table 3 K factor Table**

C	Best Corner Frequency	K factor
21.533μF	23.740 kHz	4.692
25.079μF	21.842 kHz	5.083
32.587μF	20.095 kHz	6.042
36.312μF	15.649 kHz	5.230
38.469μF	13.247 kHz	4.703

5. The output filter capacitor is chosen so  $C R_L$  pole cancels  $R_C C_C$  zero

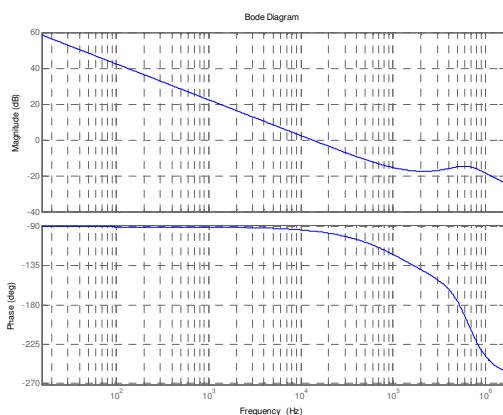
$$\epsilon R_C C_C = C \left( \frac{R_L}{2} + r_C \right), \text{ and}$$

$$C_C = \frac{C}{\epsilon R_C} \left( \frac{R_L}{2} + r_C \right)$$

$$\epsilon = (1 \sim 3)$$

Example 3:

$V_{IN} = 5V$ ,  $V_O = 13.3V$ ,  $I_O = 300mA$ ,  $f_s = 1,190kHz$ ,  
 $V_{FB} = 1.233V$ ,  $L = 6.65\mu H$ ,  $G_m = 85\mu S$ ,  
 $r_L = 76.689 m\Omega$   
 $r_C = 9.13m\Omega$ ,  $R_F = 0.7667\Omega$ ,  $C_C = 1.95nF$ ,  
 $R_C = 7.6k\Omega$ ,  $C = 38.5\mu F$ ,  $\epsilon = 3$ ,  $R_{CS} = 0.23V/A$ .



**Figure 7. Bode Plot of Loop Gain Using Matlab® Simulation**

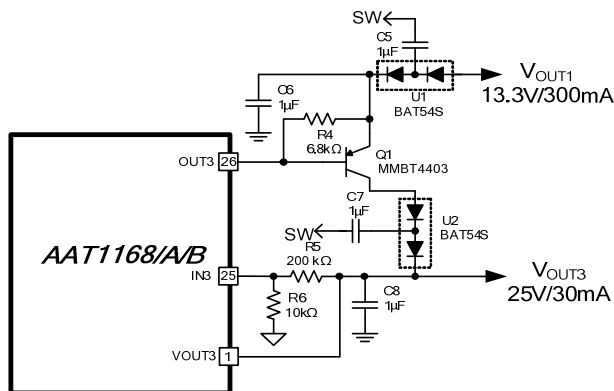
### Positive and Negative LDO driver Output Voltage Selection

The output voltage of positive LDO driver is set by a resistive divider from the output (Vout3) to GND with the center tap connected to the IN3, where  $V_{IN3}$ , the positive LDO driver feedback regulation voltage, is 1.25V. Choose  $R_6$  (Figure 8) between 10k  $\Omega$  and 51k  $\Omega$ . And calculate  $R_5$  with the following equation.

$$R_5 = R_6 \left( \frac{V_{out3}}{V_{IN3}} - 1 \right)$$

The output voltage of negative LDO driver is set by a resistive divider from the output (VGL) to VREF with the center tap connected to the IN2, where  $V_{IN2}$ , the negative LDO driver feedback regulation voltage, is 0.25V. Choose  $R_9$  (Figure 9) between 10k  $\Omega$  and 51k  $\Omega$  and calculate  $R_8$  with the following equation.

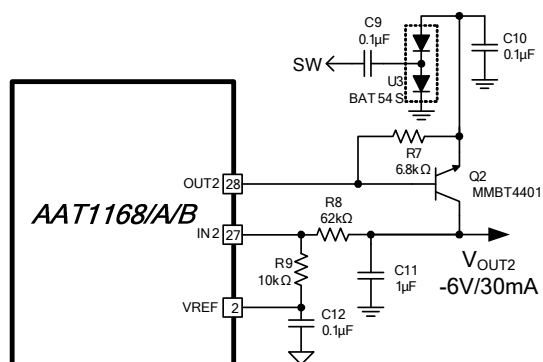
$$R_8 = R_9 \left( \frac{V_{IN2} - V_{GL}}{V_{REF} - V_{IN2}} \right)$$



**Figure 8. The Positive LDO Driver**



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**Figure 9. The Negative LDO Driver**

Example 4:

For system design

$V_{OUT3} = 25V$ ,  $R_5 = 200k\Omega$ ,  $R_6 = 10k\Omega$ ,  
 $V_{OUT2} = -6V$ ,  $R_8 = 62k\Omega$ ,  $R_9 = 10k\Omega$

**Flying Capacitors**

Increasing the flying capacitor ( $C_5$ ,  $C_7$ ,  $C_9$ ) values can lower output voltage ripples. The 1µF ceramic capacitors works well in positive LDO driver. A 0.1µF ceramic capacitor works well in negative LDO driver.

**LDO Driver Diode**

To achieve high efficiency, a Schottky diode should be used. BAT54S (Figure 8 and 9) has fast recovery time and low forward voltage for best efficiency.

**LDO Driver Base-Emitter Resistors**

For AAT1168, the minimum drive current for positive and negative LDO driver are 1mA, thus the minimum base-emitter resistance can be calculated by the following equation:

$$R_{4(min)} \geq V_{BE(max)} / ((I_{OUT3(min)} - I_C) / h_{fe(min)})$$

$$R_{7(min)} \geq V_{BE(max)} / ((I_{OUT2(min)} - I_C) / h_{fe(min)})$$

**Table 4 Pass Transistor Specifications**

	MMBT4401	MMBT4403
$V_{BE(max)}$	0.65V	0.5V
$h_{fe(min)}$	130	90
DIODES Product, Case: SOT23		

Example 5:

Output current of  $V_{OUT3}$  and  $V_{OUT2}$  are 30mA, the minimum base-emitter resistor can be calculated as

$$R_{4(min)} \geq 0.5 / ((1mA - 30mA) / 90) \geq 750\Omega$$

$$R_{7(min)} \geq 0.65 / ((1mA - 30mA) / 130) \geq 845\Omega$$

The minimum value can be used, however, the larger value has the advantage of reducing quiescent current. So we choose 6.8kΩ to be  $R_4$ .

**Charge Pump Output Capacitor**

Using low ESR ceramic capacitor to reduce the output voltage ripple is recommended. With ceramic capacitor, output voltage ripple is dominated by the capacitance value. The minimum capacitance value can be calculated by the following equation:

$$C_{out} \geq \frac{I_{load}}{2V_{ripple}f_s}$$

Example 6:

The output voltage ripple of  $V_{OUT3}$  and  $V_{GL}$  is under 1%, the minimum capacitance value can be calculated as

$$C_{out}(V_{OUT3}) \geq \frac{30mA}{\eta \times 250mV \times 1.19MHz} \approx 0.1\mu F$$

$$C_{out}(V_{GL}) \geq \frac{30mA}{\eta \times 60mV \times 1.19MHz} \approx 0.33\mu F$$

$\eta$ : Efficiency, about 60% at charge pump circuit



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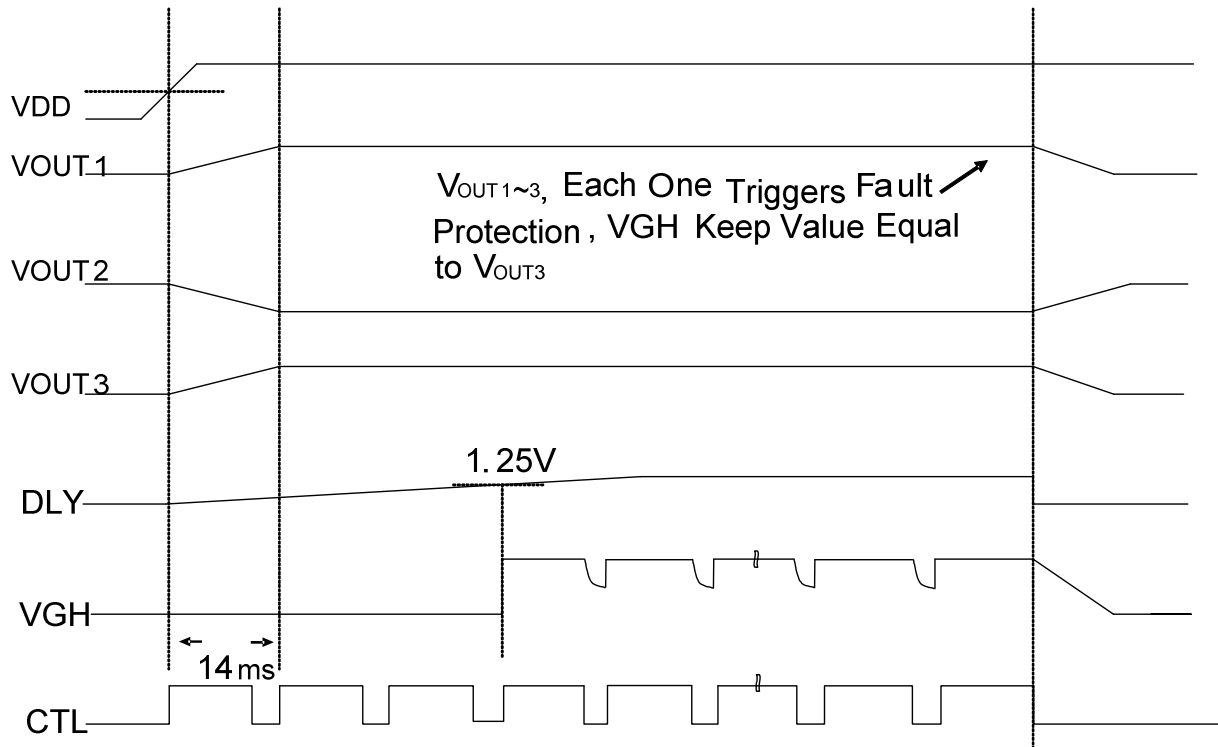
**Operational Amplifier**

The AAT1168 have five amplifiers independent. The operational amplifiers are usually used to drive  $V_{COM}$  and the gamma correction divider string for TFT-LCD. The output resistors and capacitors of amplifiers are as low pass filter and compensator for unity GAIN stable.

**Table 5. Recommended Components**

DESIGNATION	DESCRIPTION
L	6.8 $\mu$ H, 1.8A, MITSUMI C6-K1.8L 6R8
U1, U2, U3	200mA 30V Schottky barrier diode (SOT-23), DIODES BAT54S
D	2A 20V rectifier diode DIODES DFLS220L
C3	10 $\mu$ F, 25V X5R ceramic capacitor
C5, C6, C7	1 $\mu$ F, 25V X5R ceramic capacitor
C2, C4, C9, C10, C12	0.1 $\mu$ F, 50V X5R ceramic capacitor

**Soft Start Waveform**



**AAT1168/1168A/1168B****LAYOUT CONSIDERATION****Layout Guide**

The system's performances including switching noise, transient response, and PWM feedback loop stability are greatly affected by the PC board layout and grounding. There are some general guidelines for layout:

**Inductor**

Always try to use a low EMI inductor with a ferrite core.

**Filter Capacitors**

Place low ESR ceramics filter capacitors (between 0.1 $\mu$ F and 0.22 $\mu$ F) close to VDD and VREF pins. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. The ground connection of the VDD and VREF bypass capacitor should be connected to the analog ground pin (GND) with a wide trace.

**Output Capacitors**

Place output capacitors as close as possible to the IC. Minimize the length and maximize the width of traces to get the best transient response and reduce the ripple noise. We choose 10 $\mu$ F ceramics capacitor to reduce the ripple voltage, and use 0.1 $\mu$ F ceramics capacitor to reduce the ripple noise.

**Feedback**

If external compensation components are needed for stability, they should also be placed close to the IC. Take care to avoid the feedback voltage-divider resistors' trace near the SW. Minimize feedback track lengths to avoid the digital signal noise of TFT control board.

**Ground Plane**

The grounds of the IC, input capacitors, and output capacitors should be connected close to a ground plane. It would be a good design rule to have a ground

plane on the PCB. This will reduce noise and ground loop errors as well as absorb more of the EMI radiated by the inductor. For boards with more than two layers, a ground plane can be used to separate the power plane and the signal plane for improved performance.

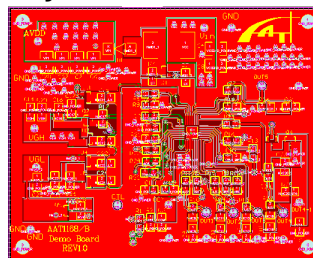
**PC Board Layout**

Figure 11. TOP Layer

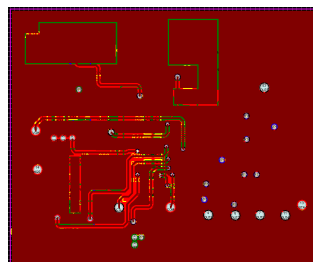


Figure 12. Midlayer1 (Ground Plane)

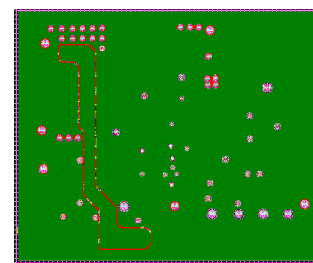


Figure 13. Midlayer2 (Power Plane)

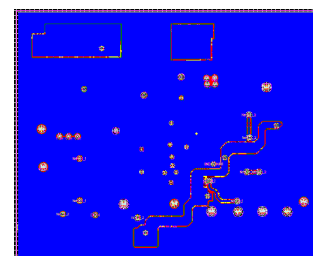


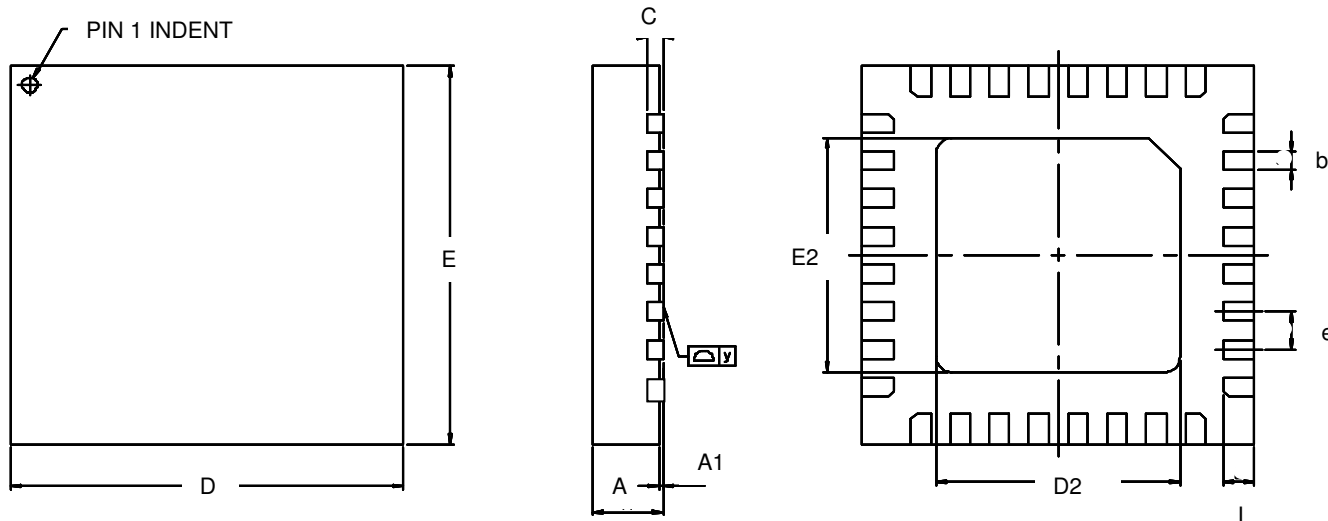
Figure 14. Bottom Layer



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**PACKAGE DIMENSION**

**VQFN32**



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN	TYP	MAX
A	0.8	0.9	1.0
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
C	-----	0.2	-----
D	4.9	5.0	5.1
D2	3.05	3.10	3.15
E	4.9	5.0	5.1
E2	3.05	3.10	3.15
e	-----	0.5	-----
L	0.35	0.40	0.45
y	0.000	-----	0.075